Industrial Policy Committee

Technology Harmonisation Advisory Group

Data Systems and On Board Computers
Roadmap
Issue *4* rev. 2Draft

TEC-EDD
Giorgio Magistrati

18 October 2016

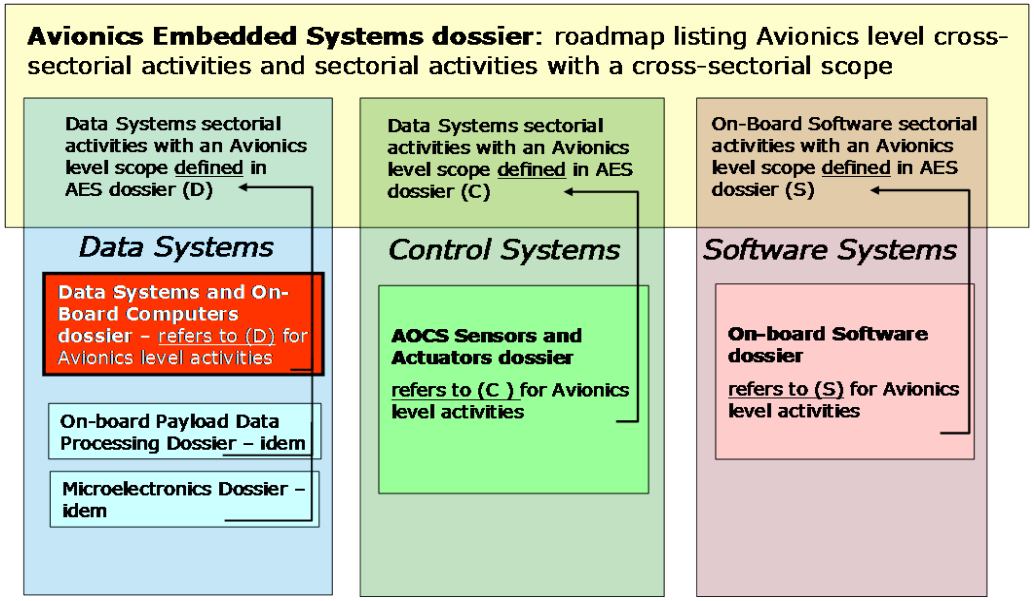
Contents

Technology Overview

1. ***Data Systems and On-board Computers*** *encompass a vast range of functional blocks that include* ***Telecommand and Telemetry Modules, On-Board computers, Data Storage and Mass memories, Remote Terminal Units, Communication protocols, Interfaces and Busses****.*
2. *These elements are common to all projects and are subject to a demanding set of evolving requirements from Science, Exploration, Earth Observation, Telecom missions, Navigation, Launchers and intrinsically linked to software technology, including validation techniques.*
3. *In addition to the classical evolution induced objectives, such as* ***increasing processing power, reducing mass, volume and power budgets****, additional* ***driving requirements*** *are identified during the definition phase of new programs.*
4. *Such requirements are not only related to the implementation of* ***functional services linked to on-board communication standards*** *but also to* ***new architectural and development paradigms for the system and application software.***

Technology Overview

IPC-THAG



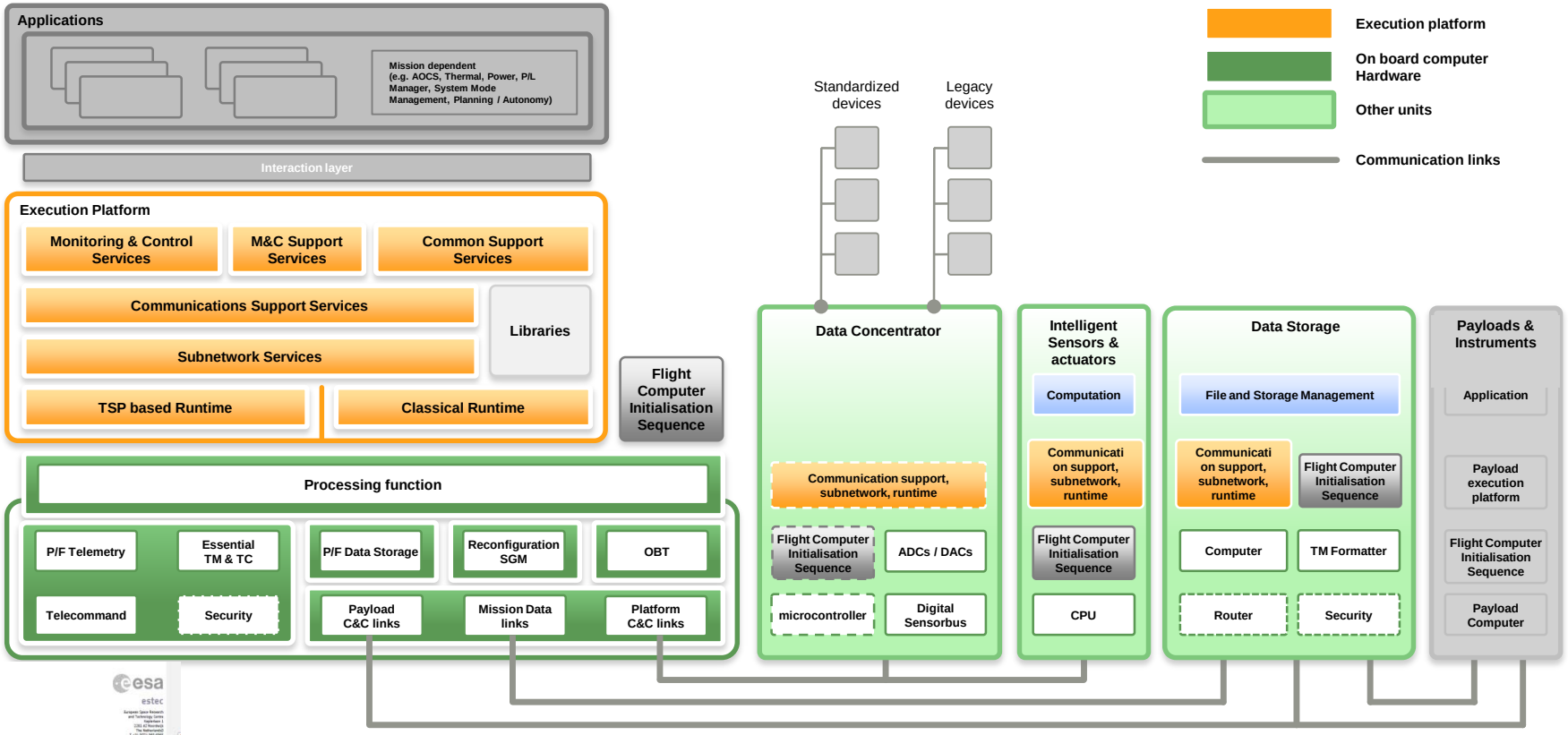
TD	TECHNOLOGY DOMAIN	TSD	TECHNOLOGY SUBDOMAIN
1	On-Board Data Systems	A	Payload Data Processing
		B	On Board Data Management
		C	Microelectronics for digital and analogue applications

ESA Technology tree

1. ***On-board Computers*** *(or Spacecraft Management Unit SMU or Command & Data Handling Management unit CDMU)*
2. ***RTU/RIUs*** *(Remote Terminal /Interface Units proving a data concentrator function)*
3. ***Platform Solid State Mass Memories*** *(optionally hosted inside the OBC)*
4. ***TM/TC units*** *(usually hosted inside the OBC) +* ***Security****,*
5. ***Interfaces, Busses and comm' protocols*** *(to connect units/sensors/actuators together but also internal busses as inter-processor links inside an OBC)*

Technology Overview

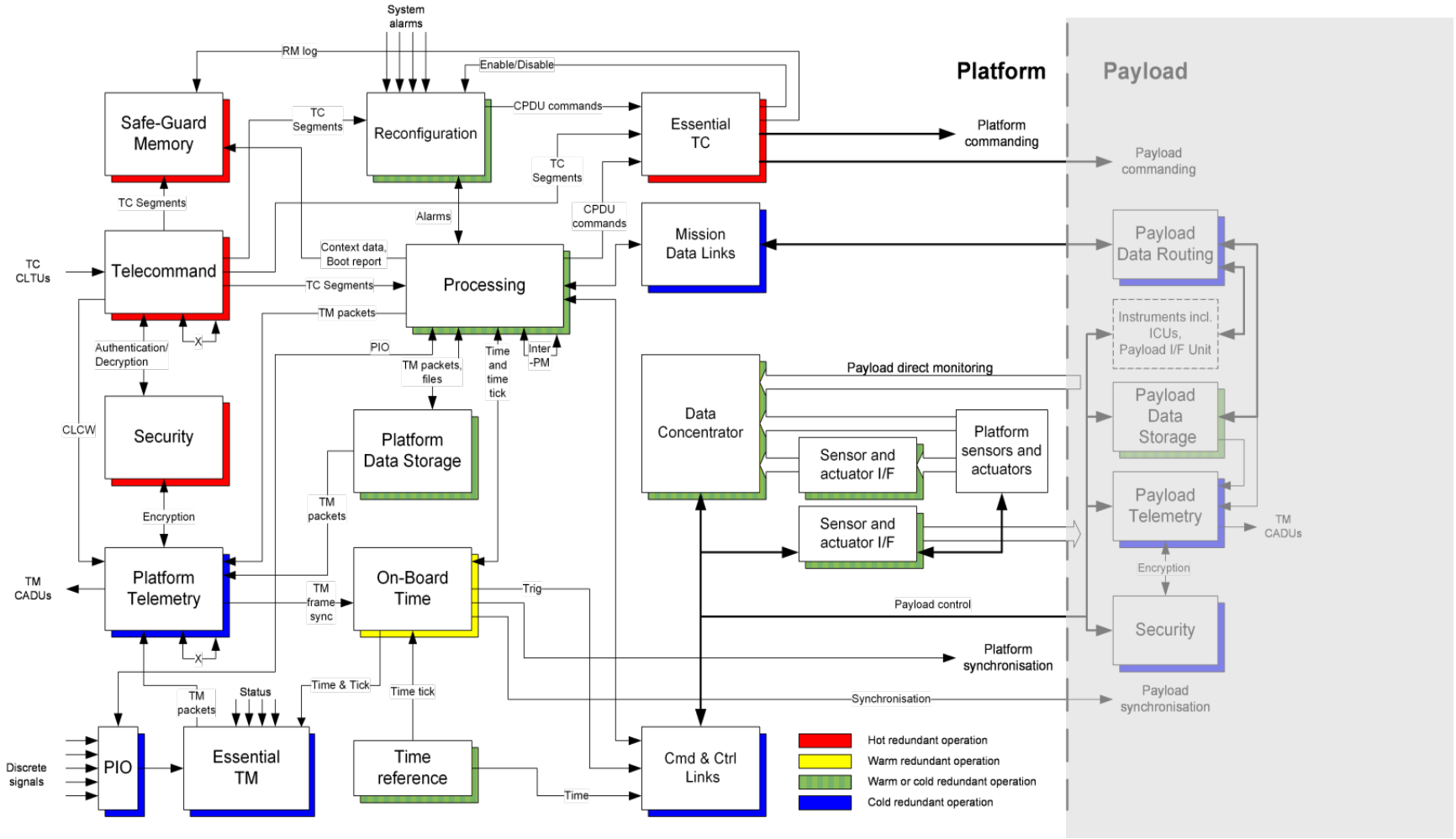
IPC-THAG



SAVOIR Reference Architecture and Building Blocks

Technology Overview

IPC-THAG

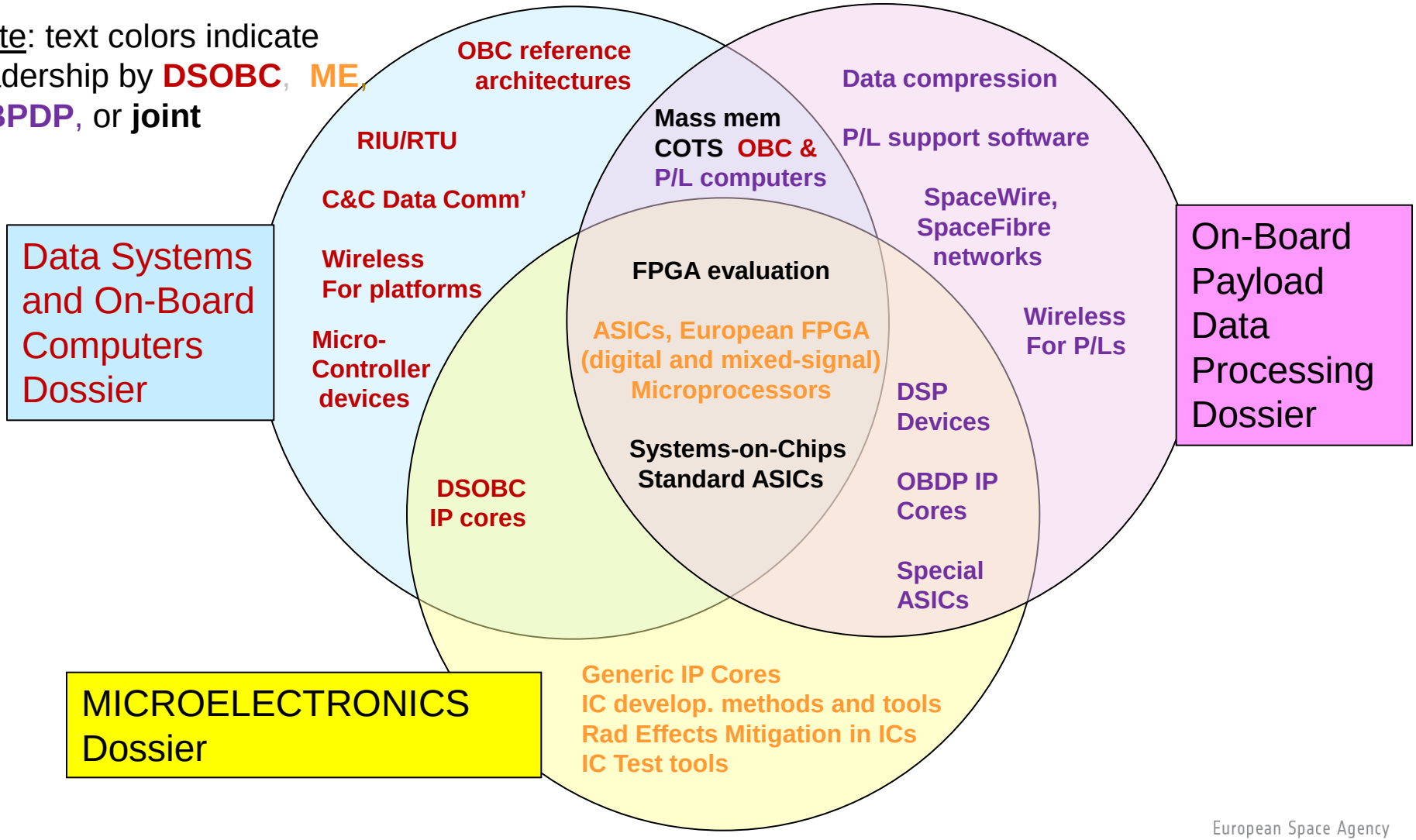


SAVOIR Functional Reference Architecture

Technology Overview: synergies among the three Data Systems dossiers

IPC-THAG

Note: text colors indicate leadership by **DSOBC**, **ME**, **OBPDP**, or **joint**



Mission Needs and Market Perspectives

The **Data System, and the On-Board Computer as main actor** of a P/F Data System, is the entity responsible for the command and monitoring of the S/C. It implements the S/C management and the mission management functions an extension of the ground control and operation centre. **Consequently every modern Spacecraft and Launcher are equipped with a Data Systems and an On–Board Computer**.

Satellite missions can be classified in two categories for what concerns the P/F data systems:

- **Recurring data systems** (Telecom, Earth Observations and the majority of Science Missions) where the emphasis is on schedule and cost reduction,
- **New data systems as Exploration**, **Space Robotics or dedicated science missions that require specific designs** (e.g. Fault Tolerant Computer / High Available Computer for descent module) and very high performance of the platform to support the payload.

Reference for Prioritisation

According to the implementation of the previous (2011) roadmap :
***33ESA activities** are "funded" or "partially funded" for a budget of about **20.2 M€**.* *

*The total amount of fourteen **additional ESA activities** that were not part of the 2011 Roadmap, amounted to ~ **7.1 M€**.*

***Total of 47 ESA activities approved since 2011 for a budget of 27.3 M€ (**20.2 M€ + 7.1 M€)*

So, the yearly reference (total budget of all relevant activities approved since the previous Roadmap divided by the number of years (6 years, as of December 2015):

Yearly reference budget = 4550 k€

ROADMAP
General Development Approach

IPC-THAG

The following lines of actions (already proposed in the previous Harmonization cycle) will be maintained and pursued:

Aim A: Computer Architectures

3 running activities, 2 activities going to start in 4Q2016, 10 new activities in the area of Data Systems and On-Board Computer architectures targeting new architectures, cost reduction, integration of new functionalities and development of reference designs

Aim B: Building Blocks

9 running activities, 2 activities going to start in 4Q2016, 13 new activities Microcontrollers (Rad-tolerant and Rad-hard), OBC mass Memory, RTUs/RIUs, microRTU, Interface Controller (wireless) Asic, CFDP controller, LVDS transceivers, others

ROADMAP
General Development Approach

IPC-THAG

Aim C: Cots Based Computers

1 running activity, 3 new activities

Qualification of a dynamic Latch-up protection circuit, characterization of COTS components (and Lots procurement)

Aim E: Interfaces and Busses

10 running activities, 1 activity going to start, 10 new activities related to Command & Control Interfaces – P/F interfaces (CAN/CANOpen, SpW, SpacePower link, TTEthernet, Wireless, SPI)

Aim F: Security

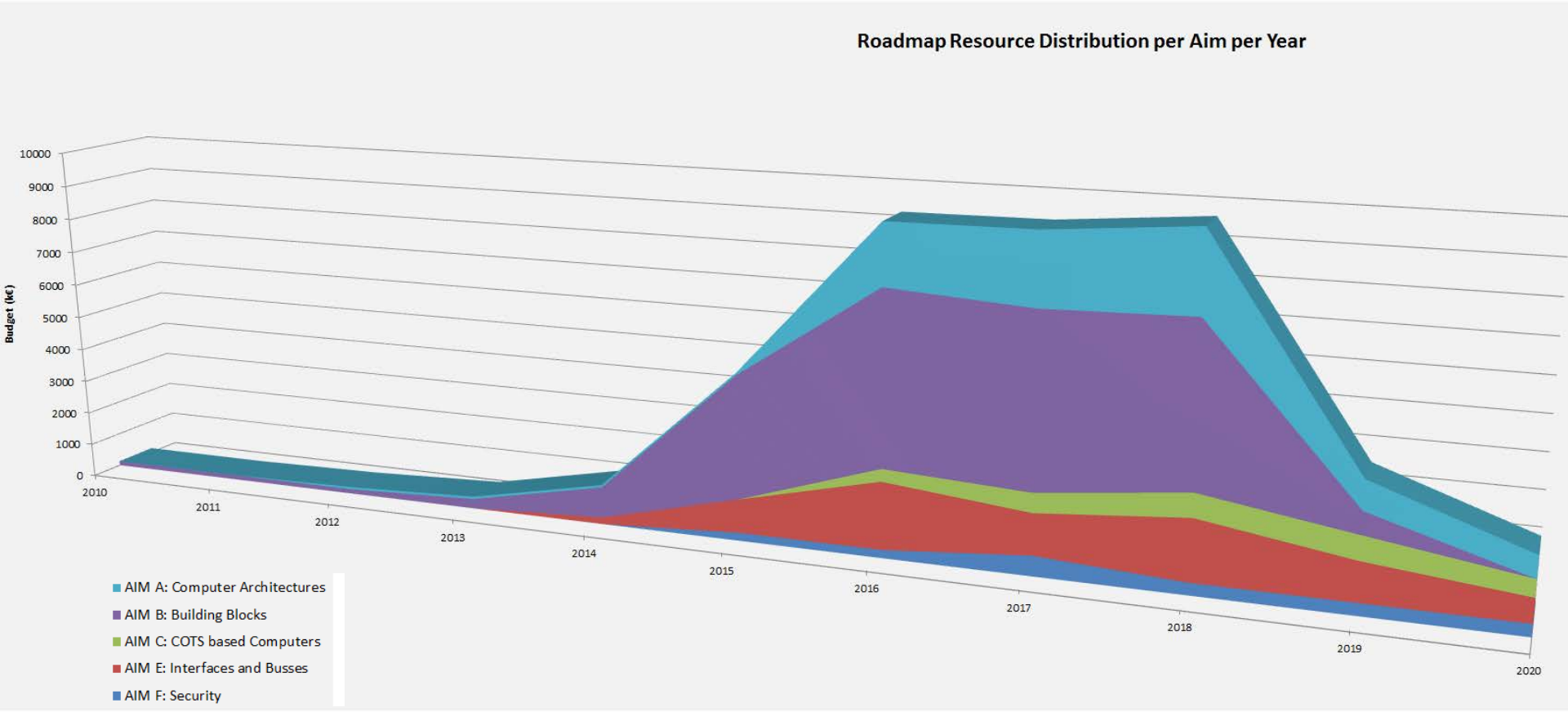
1 running activity, 3 new activities:

Crypto Processor and Space Data Link standard

Aim D: On Board Communications *is moved to the Avionics Embedded Dossier for its cross-sectorial content (HW, SW and System aspects)*

ROADMAP
Proposed development approach: Resource Distribution

IPC-THAG



ROADMAP
AIM-A Computer architectures

IPC-THAG

The R&D activities developed so for the Data Systems and On-board Computers have been very successful by adopting a systematic approach to solve the previous issues that can be summarised as follow:

1. **Specification of data handling functions**: In coordination with the main stakeholders, the key functions needed by the data handling system have been identified. The ADCSS conferences and the SAVOIR related activities have allowed to define and produce products specifications
2. **Miniaturisation of generic functions** thanks to availability of SoCs, new ICs and FPGA technologies.
3. The **introduction of new paradigms**: **reduction of variants** : the data handling number of boxes and related interfaces are streamlined as much as possible to reduce their assembly, verification and integration test, **use of COTS**, **use of Reference Designs**
4. The **pre-development of products** as reference designs, devices, boards, new interfaces and possibly units ready-to-be (re-)used

ROADMAP
AIM-A Computer architectures

IPC-THAG

During the day-2 of the ADCSS2015 conference (session on Avionics Technology trends) the tomorrow's needs identified by Primes have been presented:

- **Cost reductio**n (in all the elements: HW, SW,AIT and Operations),
- **Increase of processing capabilities** (multicore, higher clock frequency),
- **Increased efficiency of integration process for large constellations**,
- **Secured software partitioning**
- **Interfaces Standardization**,
- **Satellite Data Communication Network** (new solutions cost oriented and with higher data rate in addition to legacy solutions)

A good synergy between expectations from Primes and European Equipment suppliers and the ESA view has been recognized and the on-going harmonization cycle will be the ideal mechanism to ensure that the roadmap of ESA will address the needs risen by the space community.

ROADMAP
AIM-B Building Blocks : Microcontroller

IPC-THAG

Software based data acquisition/processing and simple control applications are widely used in many spacecraft subsystems. They allow implementing software based control architectures that provide a **higher flexibility and autonomous capability versus pure hardware implementations**.

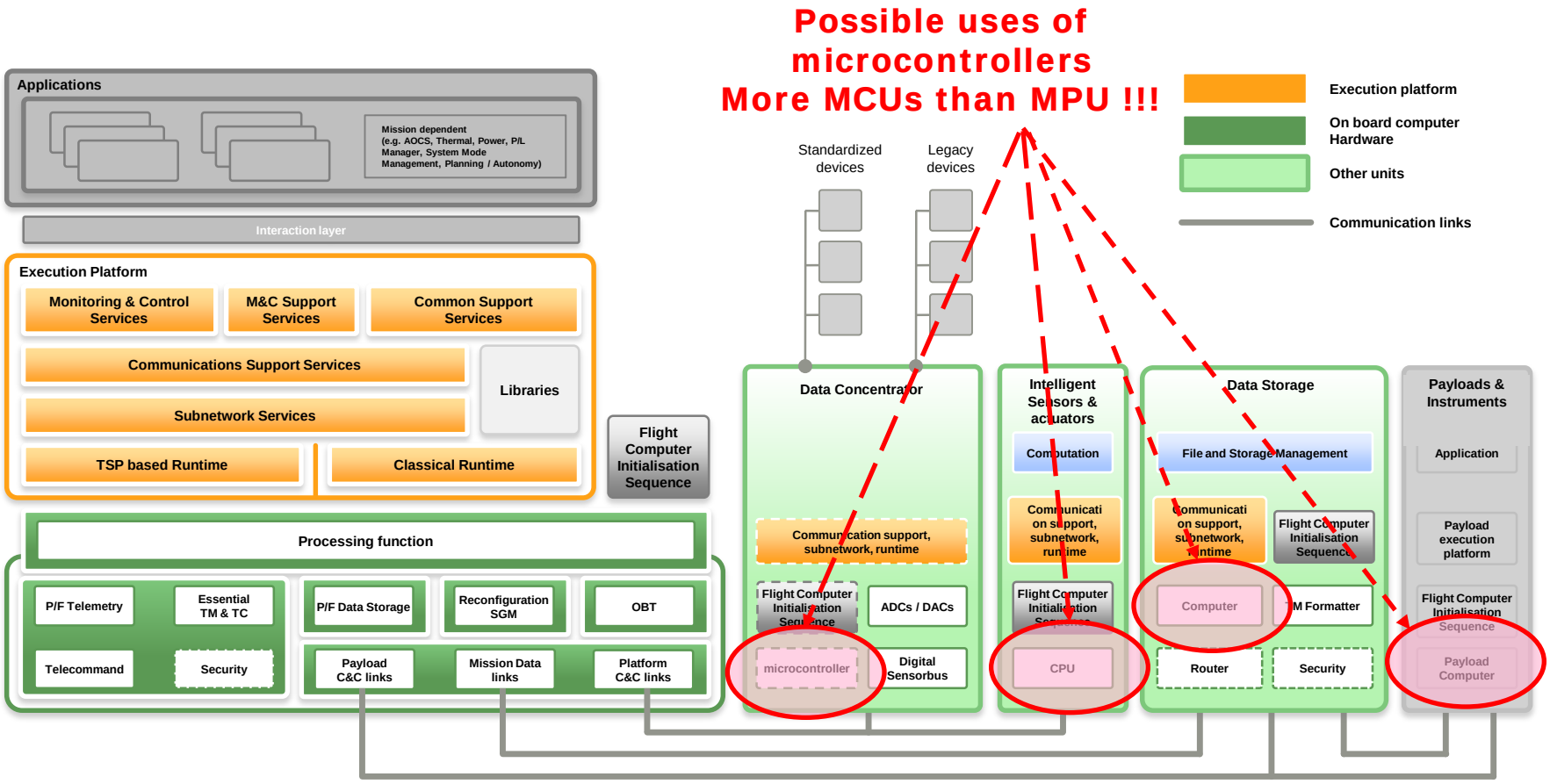
For this type of applications, where limited performances are requested to the processor, general purpose microprocessors (MPU) are usually considered not compatible due to high power consumption, high pin count packages, need of external memories and peripherals.

Ideal features of a microcontroller (MCU) to match the needs:

- relatively low price,
- low power consumption,
- limited number of pins,
- Internal RAM(/nvRAM)
- I/O peripherals for control and data acquisition (serial I/Fs, GPIO's, PWM, ADC, DAC etc.).

ROADMAP
AIM-B Building Blocks : Microcontrollers, where to use them ?

IPC-THAG



SAVOIR Reference Architecture and Building Blocks

ROADMAP
AIM-B Building Blocks : Microcontroller

IPC-THAG

Low-end microcontrollers are attractive in many applications such as:

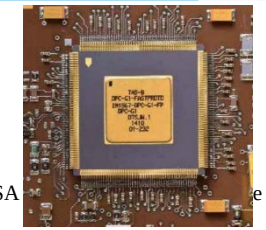
- propulsion system control
- sensor bus control
- robotics applications control
- simple motor control
- mechanism control
- power control
- particle detector instrumentation
- radiation environment monitoring
- thermal control
- antenna pointing control
- AOCS/GNC (Gyro, IMU, ...)
- RTU/RIU control
- Simple instrument control
- Wireless networking
- ...

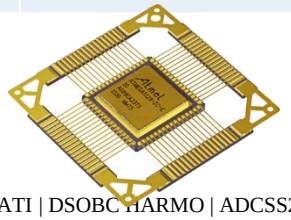
ROADMAP
AIM-B Building Blocks : MicroController

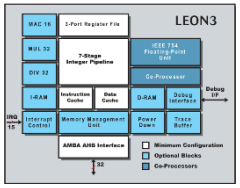
IPC-THAG

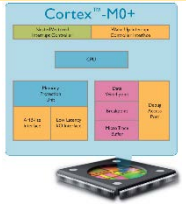
Current available/planned space-grade microcontrollers-Ics in Europe:

Device	Company	Architecture	Core bit width	Clock (MHz)	Status	RHBD
GR716	Cobham Gaisler	SPARCv8	32	50	In devel.	RadHard
UT32M0R500	Cobham Aeroflex	ARM Cortex-M0+	32	50	In devel.	RadHard
DPC	TAS ETCA	QUAD-MSP430	16	60	FM parts avail	RadHard
CCASIC	Curtiss-Wright	SPARCv8	32	80	In early devel.	RadHard
CLP	SABCA	HBRISC	32	?	In devel.	RadHard
AtmegaS128/ S64M1	ATMEL	AVR	8	8	FM parts avail/samples avail	RadTol
SAM3XE	ATMEL	ARM Cortex-M3	32	80MHz/100Mips	Under Test	RadTol
SAMV71RT	ATMEL	ARM Cortex-M7	32	300MHz/600Mips	Under Test	RadTol
Kitsune	TI	ARM Cortex-M0+	32	30	In devel.	RadTol
SAMRH71	ATMEL	ARM Cortex-M7	32	100MHz/200Mips	In devel.	RadHard









ROADMAP
AIM-B Building Blocks : Microcontroller

IPC-THAG

Current available/planned space-grade microcontroller soft cores in Europe:

Soft Core	Company	Architecture	ISA	Status	Rad Hard Design
V8uC SoC	Sitael	SPARCv8-LEON2	32	Y	Y
PicoSkyFT CPU	Skylabs	RISC8/16	8/16	Y	Y
PicoSkyFT TMR CPU	Skylabs	RISC8/16	8/16	Y	Y
Cortex M0+ CPU	ARM	ARMv6-M	16/32	Y	N
Cortex M1 CPU	ARM	ARMv6-M	16/32	Y	N
Cortex M3 CPU	ARM	ARMv7-M	16/32	Y	N

[1] ARMv6-M Licensing schemes force use of Cortex M0 and M3 on ASIC designs and restrict use of Cortex M1 on FPGA only. Cortex M1 is available through Microsemi DirectCore IP service.

ROADMAP
AIM-C Use of COTS

IPC-THAG

In term of pure processing power capabilities the majority of the mission needs can be served by space qualified products but a small percentage of applications asks for **more performances**. This was the case of the Video Processing Unit of the GAIA mission.

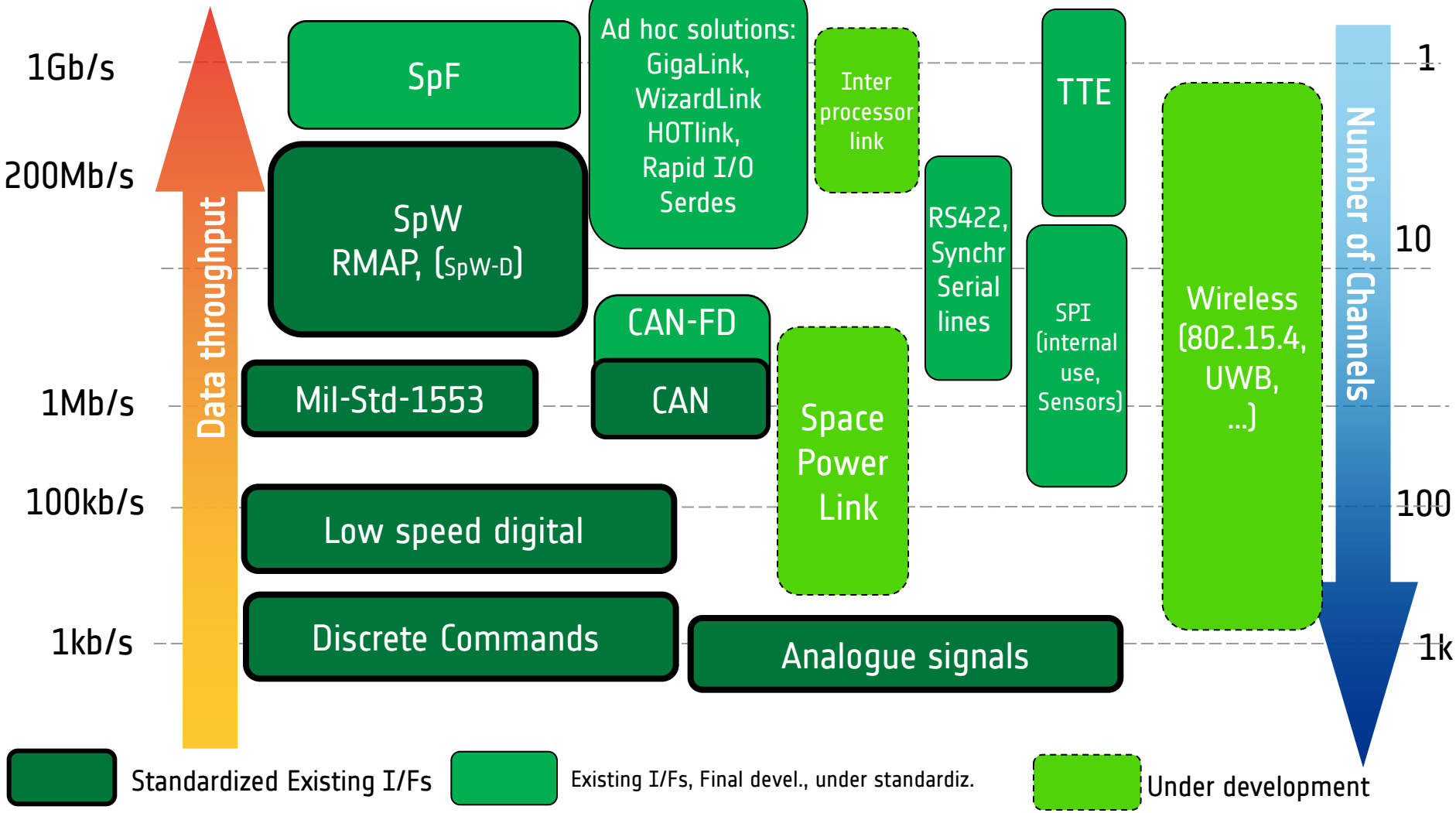
COTS can provide **new functionalities and/or integration of more functionalities** in a single component.

Use of COTS parts or COTS technologies is now also strongly pushed by the need **to reduce the cost** of the Data Systems and OBCs especially for applications with reduced requirements in terms of reliability (e.g. cubesats, nanosat). Mega-constellations programmes are reducing the target price for avionics, consequently COTS technologies and parts are considered interesting solutions provided that **adequate selection and "validation" processes are defined and performed.**

An activity to explore **new technologies, processes, and packages targeting a cost reduction** compared to processors/ICs currently used on telecommunication missions is going to start.

ROADMAP
AIM-E Interfaces&Busses

IPC-THAG



ROADMAP
AIM-E Interfaces&Busses
CAN in SPACE Workshop #2

IPC-THAG

After the success of the 1st CAN in Space WS organized in Estec in Feb 2016 we are pleased to announce the **CAN in SPACE WS#2 !**

SCOPE

Space avionics systems are witnessing a change from highly centralized intelligence to distributed autonomous functions, thanks to the availability of high capacity FPGAs and microcontrollers that offload tasks alternatively concentrated in the on-board computer.

The glue of this change are the command and control buses, and a similar process led in the late 80s to the development and successive adoption of CAN as an automotive and industrial automation bus.

1.WHEN: 14-16 June 2017

2.WHERE: **SITAEL S.p.A**. - Mola di Bari (ITALY)

MAIN TOPICS

- CAN implementations
- CAN device design
- CAN system design
- CAN diagnostic and tools
- CAN higher-layer protocols
- CAN-related research studies
- CAN applications in space or ground support equipment
- CAN applications in space industry

EVENT PAGE

http://bit.ly/can space

EARLY BIRD BOOKING !

UNTIL 10th Dec. , 2016

Closing remarks

IPC-THAG

- We are in an interesting period for the **OBC architecture**: cost reduction, integration/miniaturization of functions (GNSS, AOCS processing, …), high processing performances, availability of multicore processors are modifying the architecture of an OBC/SMU
- All the changes and variants of an OBC architecture should be implemented and specified in **SAVOIR docs**,
- Adequate effort for **COTS** characterization has to be spent, the ever increasing cost of DSM technology inevitably leads the space industry to use more COTS parts or use non-European fabs. It is essential that ESA explores ways and methods to accommodate this trend, the risk is that European space industry will be increasingly non-competitive with the rest of the world.
- **Building blocks** (in primis the microcontroller) and reference designs are fundamental for the development of new data systems architectures,
- **Interfaces**:
  - To progress in the consolidation of the existing ones (e.g. verification aspects for SpW, PHY for CAN,…)
  - To define/standardize protocols for Space applications (e.g. SpW-D, TTEthernet, SPI …)
  - To develop solutions for specific needs (Space Power link, Interprocessor link,…)

Closing remarks

IPC-THAG

Thanks to all of you for your contribution and passion !

Closing remarks

IPC-THAG

1. Back-up slides

Implementation of previous Roadmap

General Roadmap Statistics

The Roadmap has 53 activities, for a total of 29405 k€.

- ***Roadmap Activities Distribution per Programme***

  - ESA: 53 activities for a budget of 29405 k€
  - National: No National Activities

Distribution of Roadmap Activities per Programme

Distribution of Roadmap Budget per Programme

- ***Roadmap Activities Status when this Roadmap was Approved***

  Out of the 53 activities for the total Roadmap budget of 28905 k€:
  - 24 Roadmap Activities for a budget of 14135 k€ had been already approved before Harmonisation.
  - 29 Roadmap Activities for a budget of 14770 k€ had not been approved before Harmonisation or no funding status defined.

- ***Roadmap ESA Activities Status when this Roadmap was Approved***

  Out of the 53 Roadmap ESA activities for the total Roadmap budget of 29405 k€:
  - 25 Roadmap Activities for a budget of 14635 k€ had been already approved before Harmonisation or no status defined.
  - 28 Roadmap Activities for a budget of 14770 k€ had not been approved before Harmonisation or no funding status defined.

Implementation of previous Roadmap

Implementation of the Roadmaps

- ***General Roadmap Implementation***

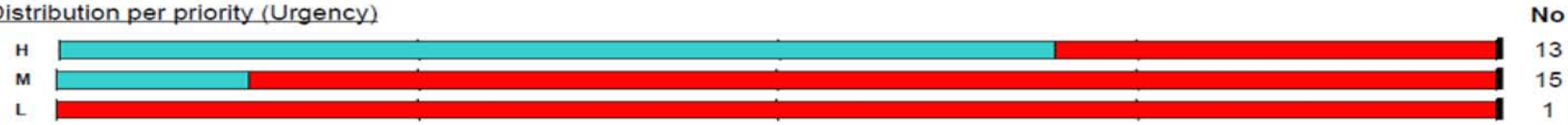
Activities

Budget

- 4 RM activities have not started as planned. Planned RM completion date: 2016.

- ***Roadmap Implementation per Priority***

Distribution per priority (Urgency)



Distribution per priority (Criticality)

- ***Funding of the ESA Activities***

Among the 53 ESA activities (29405 k€) part of this Roadmap
- 33 are "Partially Funded" or "Fully Funded" for an approximate budget of 20155 k€.
- 29 (15270 k€) had not yet been approved before Harmonisation or no funding status defined, of which 11 have been approved since and are "Partially Funded" or "Fully Funded" for an approximate budget of 6420k€.

Implementation of previous Roadmap – additional activities

IPC-THAG

Title	Description	Budget (k€)	Prog.	Ref.	Status	TRL level		Date	
						Start	End	Start	End
HIPNOS - High Performance Avionics Solution for Avanced and Complex GNC Systems	Architectural study for advanced GNC systems integrated in OBC/CDMU	150	GSP		On going	NA	NA	2015	2016
Failure Rate Prediction Models for Semiconductor Memories, NPI	Study and validation of prediction models for memories	90	NPI		On going	NA	NA	2015	2017
Avionics Product Line Building Blocks (Modular RTU TAS-B) , GSTP	Design and Development of a modular RTU	3158	GSTP6.2		On going	3	6	2015	2016
Development of an EIU	Design and Development of a RTU for Sci applications	750	CTP		On going	3	5	2015	2017
Development of miniaturized Unit based on ETM	Essential Telemetry module	40	TRP		completed	3	5	2014	2015
CAN Bus interface for TT&C	Development of CANBUS I/F for a TT&C unit	150	GSTP		On going	3	5	2015	2017
SPI Protocol(s) for Space	Prototyping of SPI protocol for space (specification and demonstrator)	400	TRP		On going	NA	NA	2015	2016
SpacePowerLink Development	Development of the IPs for Space Power Link	600	TRP+EO+Sci		On going	2	3	2015	2017
iSAFT PVS with Time Triggered Ethernet	Extension of PVS capabilities to include TTE I/F	249	G-TF		On going	NA	NA	2015	2016
Generation of a test bed for the validation of the TTEthernet technology	Definition and implementation of a test bed for TTE building blocks	800	GSTP		On going	NA	NA	2015	2017
SATA controller into a Space CPU	Evaluation of a SATA controller for space applications	200	LET-SME		completed	3	4	2013	2015
Extension of PVS with EGSE functionality	Extension of PVS according to realistic EGSE requirements and validation of PVS EGSE in a real environment.	90	G-TF		Completed	NA	NA	2014	2015
Protocol Validation system Evolution to EGSE requirements, Phase 1+2) G-TF	Extension of PVS with support for CAN/CANOpen and SpW with error injection EGSE functionalities, as well as CFDP protocol support.	240	G-TF		On going	NA	NA	2014	2015
Ethernet PHY transceiver characterization	Characterization of commercial physical transceiver for Ethernet	200	TRP		On going	3	5	2015	2016

Implementation of previous Roadmap

Few new activities have started but all of them are falling in the AIMs defined by the previous harmonization dossier:

1. Architectures (HIPNOS - High Performance Avionics Solution for Advanced and Complex GNC Systems)
2. Interfaces (e.g. SPI protocol(s) for Space, characterization of PHY for Ethernet, extension of Protocol Validation System capabilities, ...)
3. Building blocks (TAS-B Modular RTU, Development of an EIU, ...)

Mission Needs and Market Perspectives

IPC-THAG

Virtually all satellite and launcher is equipped with command and data processing and the market breakdown between “On-board payload data processing” and “data systems and on board computers” is not easy because the same firms and technical expertise are involved in both fields. For market estimate purposes we can take as **approximate share 60% as contribution of payload data processing and 40% for data systems and on board computers**, although these values can vary a lot depending on the typology of the mission and spacecraft.

Accounting for the uncertainties of the current constellation projects, the most likely scenario (Euroconsult Data) is that in the next 10 years 1.400 appx commercial and institutional satellites will be produced valuated €200b (€20b per year). **The command and data processing electronics installed in these 1.400 appx satellites will generate an industrial turnover of approximately €2,5b per year worldwide.**

Assuming the European market share will remain the same in the next decade compared to the past 5 years, **the European satellites will generate industrial activity reaching approximately €850M yearly average, related to development and manufacturing of command and data processing electronics units**. The average cost of electronic components in command and data processing units is about 35% of the sales price of these units, leading to electronic parts procurement for ~ 300M€/year by EU companies.