Triple Core Lock Step (TCLS) ARM FOR SPACE

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ARM Ltd

A semiconductor IP company headquartered in Cambridge, UK

- Key supplier of IP blocks enabling scalable, efficient system-on-chip solutions
- Product portfolio:
  - Diverse components, including **CPUs and GPUs** designed for specific tasks
  - **Interconnect System IP** delivering coherency and the quality of service required for lowest memory bandwidth
  - **Physical IP** for a highly optimized processor implementation
  - **Software** increasing system efficiency with optimized software solutions

TCLS ARM for Space

Introduction

- Collaborative project funded by European Commission H2020 Space program
- Start in Feb'15 – 2-yr duration

Partners

AIRBUS DEFENCE & SPACE (Project Leader)

ARM Atmel DOLPHIN INTEGRATION

Public Website

http://www.tcls-arm-for-space.eu/

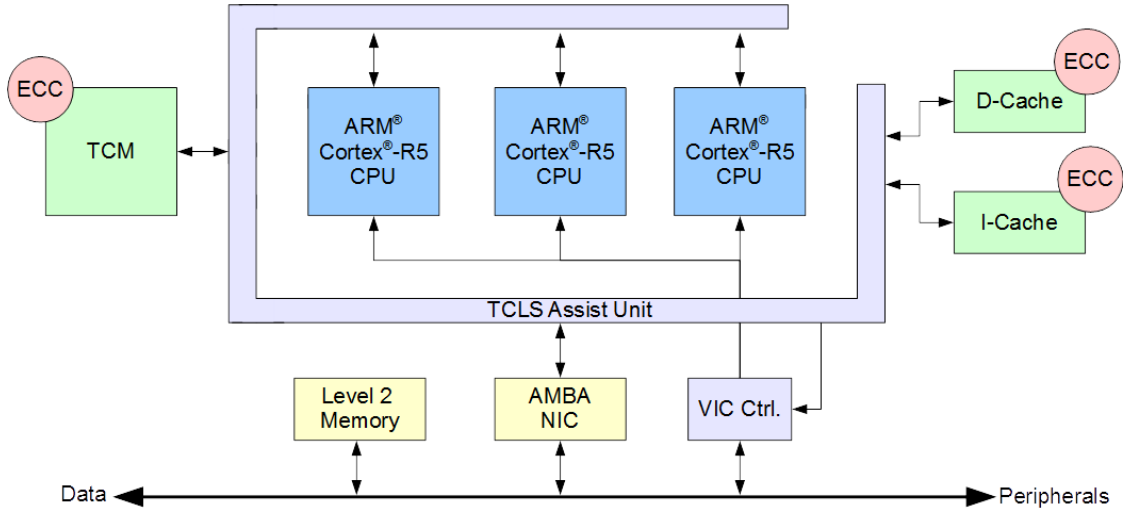
Project Objectives

- Investigate the feasibility of a **fail functional ARM CPU** using the triple core lockstep (TCLS) principle
- Target **radiation-tolerant space** and **safety-critical terrestrial** applications
- Assess the fail functional design using radiation-tolerant STM65nm technology

ARM's Objectives

- Understand **fail functional** design requirements and principles under heavy SEU scenarios
- Design the **TCLS Cortex-R5** sub-system
- Capture trade-offs of TCLS in comparison to single core and dual-core Lockstep (DCLS) solutions

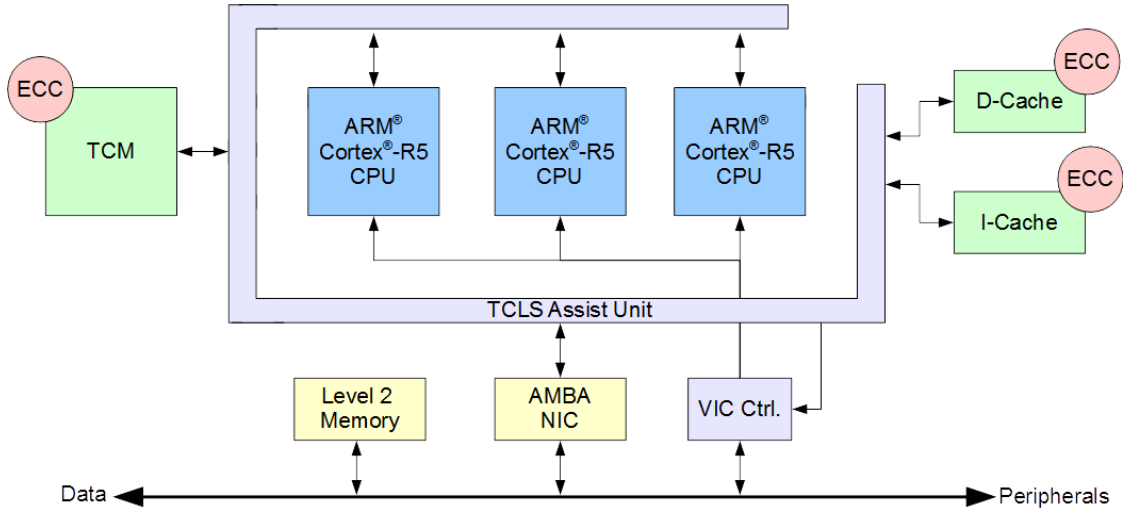
TCLS in a Nutshell



Concept

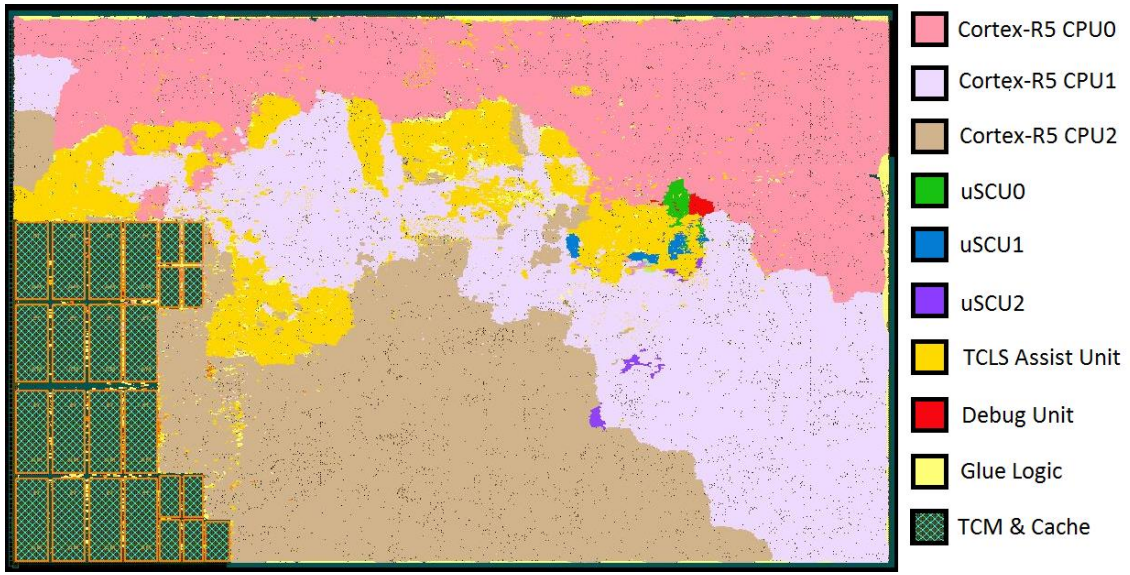
- Three ARM CPUs execute in lockstep
- Shared ICache, DCache & memory
- **Fail functional capable** – Resynchronize upon divergence
- Support for demand scrubbing, count correctable errors
- On-line testing, Error injection feature supported

ARM Triple Core Lock-Step (TCLS) Processor



- **3 ARM CPUs** (e.g., Cortex-R5) to be implemented using **commercial process technology**
  - Original and optimized CPU design – No modifications to the RTL
  - Open to be used with any other ARM CPU, including performance-oriented A-class
  - Shared memory
- **TCLS Assist Unit** to be implemented using **rad-hard process technology (for space-use)**
  - Coordinates the CPUs
  - Detects errors (correctable and un-correctable) & prevent them from propagating to memory (majority-voting)
  - Re-synchronizes CPUs after correctable errors & CPU scrubbing

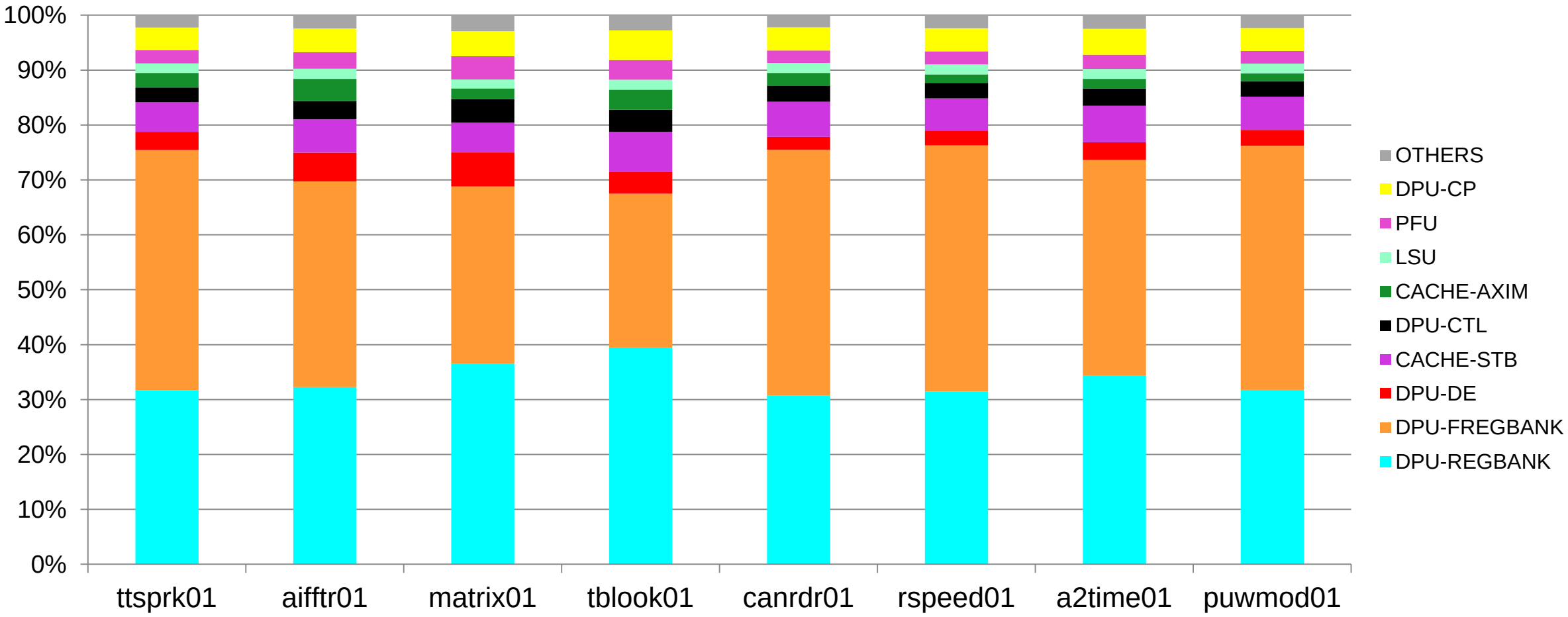
Preliminary Results @ 32 nm CMOS LP Process Tech



- Performance (not optimized yet):
  - @ 450 MHz → ~750 DMIPS
- Area:
  - < 36% overhead w.r.t. DCLS (64 KB caches and TCM)
  - TCLS Assist Unit: < 7% overhead → Smaller with greater CPUs (e.g., Cortex-A)
- CPU Re-synchronization / Scrubbing:
  - < 5 us (SAVE_ISR: 1,171 clock cycles & RESTORE_ISR: 1,180 clock cycles)
  - Current commercial solution take about 1 ms!!

Soft-Error Rate (SER)

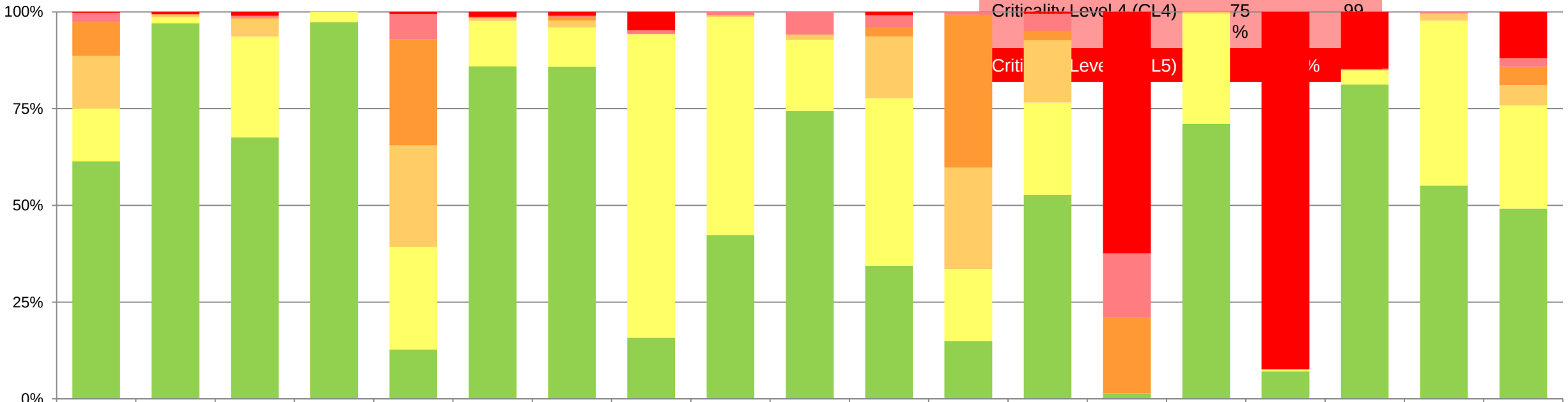
Failure Rate: 5.4%



Unit Criticality Analysis

Detailed reports available!

	SER		
Criticality Level 0 (CL0)	0%		
Criticality Level 1 (CL1)	1%	→	24 %
Criticality Level 2 (CL2)	25 %	→	49 %
Criticality Level 3 (CL3)	50 %	→	74 %
Criticality Level 4 (CL4)	75 %	→	99 %
Criticality Level 5 (CL5)	100 %		



	PFU	MPU	LSU	CACHE-LOGIC	CACHE-STB	DCACHE	ICACHE	CACHE-AXIM	DPU-BR	DPU-CPSR	DPU-CTL	DPU-DE	DPU-LDST	DPU-REGBANK	DPU-FPU	DPU-FREGBANK	DPU-CP	DPU-DP	CPU TOTAL
CL5	2	6	16	0	4	8	5	89	0	0	11	0	1	608	0	1045	114	0	1909
CL4	25	0	5	0	44	0	1	17	2	26	38	4	9	160	0	0	3	5	339
CL3	90	3	5	0	187	2	5	1	0	0	29	236	5	192	0	0	0	0	755
CL2	140	6	73	0	178	4	9	2	1	6	194	157	33	0	7	0	0	22	832
CL1	140	16	402	5	181	71	50	1468	124	81	527	111	49	0	475	6	29	499	4234
CL0	632	1034	1044	184	87	519	424	296	93	329	419	89	108	14	1181	80	631	646	7810

Questions ???

Drop by our poster at the exhibition centre for more details

ARM