# Industrial Policy Committee

## Technology Harmonisation Advisory Group

## MICROELECTRONICS:
## ASIC AND FPGA

### Issue 4 rev. 2Draft

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# Technology Overview

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**Avionics Embedded Systems dossier**: roadmap listing Avionics level cross-sectorial activities and sectorial activities with a cross-sectorial scope

| Data Systems sectorial activities with an Avionics level scope defined in AES dossier (D) | Data Systems sectorial activities with an Avionics level scope defined in AES dossier (C) | On-Board Software sectorial activities with an Avionics level scope defined in AES dossier (S) |
|---|---|---|
| *Data Systems* | *Control Systems* | *Software Systems* |
| **On-board Computers and Data Systems dossier** – refers to (D) for Avionics level activities | **AOCS Sensors and Actuators dossier** refers to (C ) for Avionics level activities | **On-board Software dossier** refers to (S) for Avionics level activities |
| Payload Data Processing Dossier – idem | | |
| Microelectronics Dossier – idem | | |

# Technology Overview: Areas covered in "Microelectronics: ASIC & FPGA dossier"

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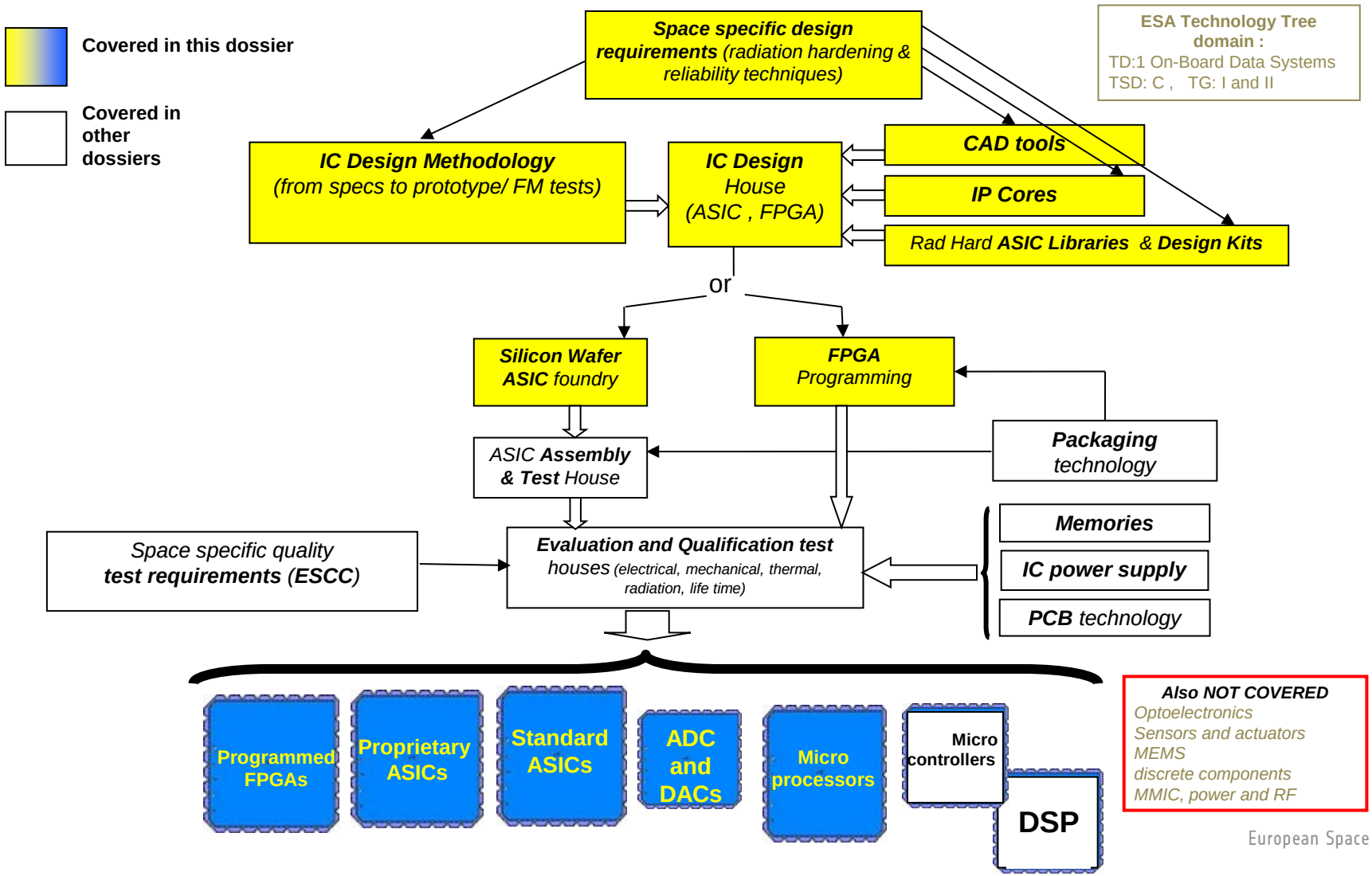


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# Technology Overview: Synergies among the three Data Systems Dossiers

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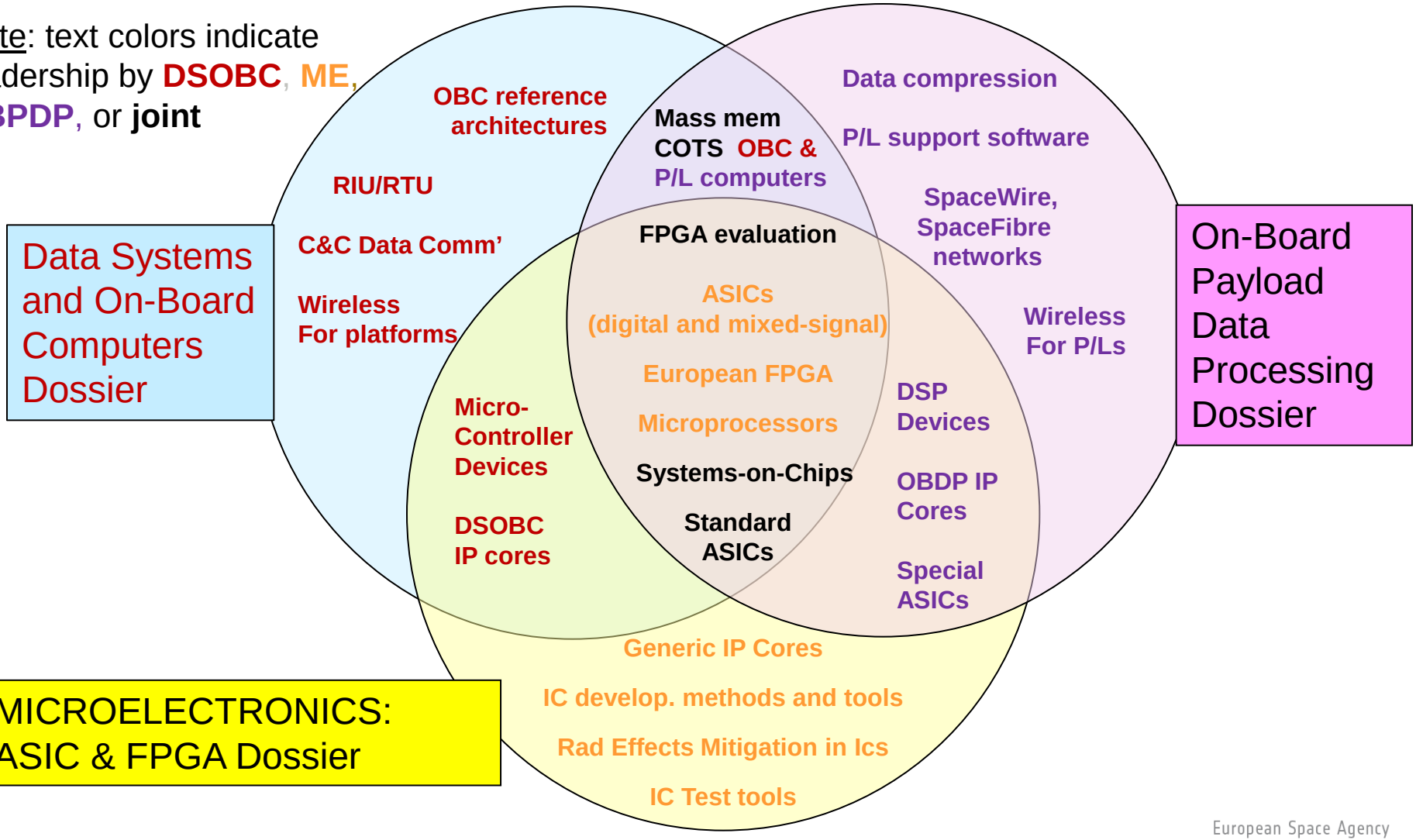
Note: text colors indicate leadership by **DSOBC**, **ME**, **OBPDP**, or **joint**

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# MISSION NEEDS / MARKET PERSPECTIVES
## European strategic interest

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- availability of European space ASIC and FPGA technology in general, at competitive prices

- miniaturisation and speed/power optimization
  - make advances in the performances and functional capabilities of our satellites (e.g. DSM ASIC for next generation Telecom payloads)
  - maintain and increase competitiveness of European satellite equipment manufactures
  - minimize the dependency on export restrictions and overhead (e.g. US ITAR parts)

- trend: manufacturing in Asia, with cheaper labour costs and national incentives for foreign capital investment facilitates a better and more sustainable business model

  - European strategic interest that all ASIC/FPGA capabilities (design houses, manufacturing and test) remain secured and sustainable in Europe.
  - While in parallel there is a European strategy to work with Asian Fabs

# MISSION NEEDS / MARKET PERSPECTIVES
## FPGA

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- steady increase in the use of FPGAs versus more or less constant use rate of new and existing catalogue ASICs and ASSPs.
  - IP Core-based SOC design is also experimenting an increase

- FPGAs used in space is dominated by US one-time-programmable technologies

- Rad hard reprogrammable FPGAs received a slow uptake by the space community.
  - Reasonable parts costs shall be a major requirement in the European FPGA development
  - The upcoming family of European BRAVE FPGAs offers potential for a much wider acceptance, as well as the new Microsemi FLASH-based reprogrammable parts.

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# Reference for Prioritization

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*According to the implementation of the **previous (2011) roadmap** :*

- ***33 ESA activities** are "funded" or "partially funded" for a budget of about **24M€**.*
  *

- ***37 additional ESA activities** that were not part of the 2011 Roadmap, amounted to ~ **24.5 M€**.*

***Total of 70 ESA activities approved since 2011 for a budget of 48.5 M€***

*So, the yearly reference (total budget of all relevant activities approved since the previous Roadmap divided by the number of years (6 years, as of December 2015):*

## *Yearly reference budget = 8M€*

# ROADMAP Aims (1/2)

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**Aim A: Digital ASIC technologies**

- European deep submicron technologies 65nm and 28nm or beyond, evaluation of radiation effects in these technologies.

**Aim B: ASIC/FPGA Design methodology and IP Cores**

- fault injection tools, HW-SW SoC co-design, various digital and A/MS new IP Cores, tools to optimise design of systems combining FPGA and Microprocessors, multi-core multithreading , timing predictability, fast simulation with Virtual Platforms and ESL, etc.

**Aim C: Analogue and mixed-signal ASICs, ADC/DAC**

- multiple ADC and DAC ASSP developments and standard standalone devices; A/MS design kits and ASIC platforms like IMEC-DARE, Atmel-ATMX150RHA, or IMST/XFAB

**Aim D: FPGA**

- new European reprogrammable BRAVE FPGA family (65nm, 28nm or beyond), tools to optimise radiation behaviour reprogrammable FPGAs

# ROADMAP Aims (2/2)

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**Aim E: Microprocessors, Standard and proprietary ASICs**

- Maintaining, improving, developing , evaluating or qualifying Microprocessors , “Standard ASICs” (or ASSPs) and other proprietary ASICs (with potential for reuse)

**Aim F: ASIC/FPGA Evaluation , Qualification, packaging, memories**

**Aim G: Read-Out ASICs for Imagers and Radiation Sensors**

- new AIM in the 2016 dossier. activities for maintaining, improving, developing , evaluating or qualifying microelectronic technologies needed for imagers, radiation sensors, namely read-out ASICs.

# ROADMAP
# Proposed development approach: Resource Distribution

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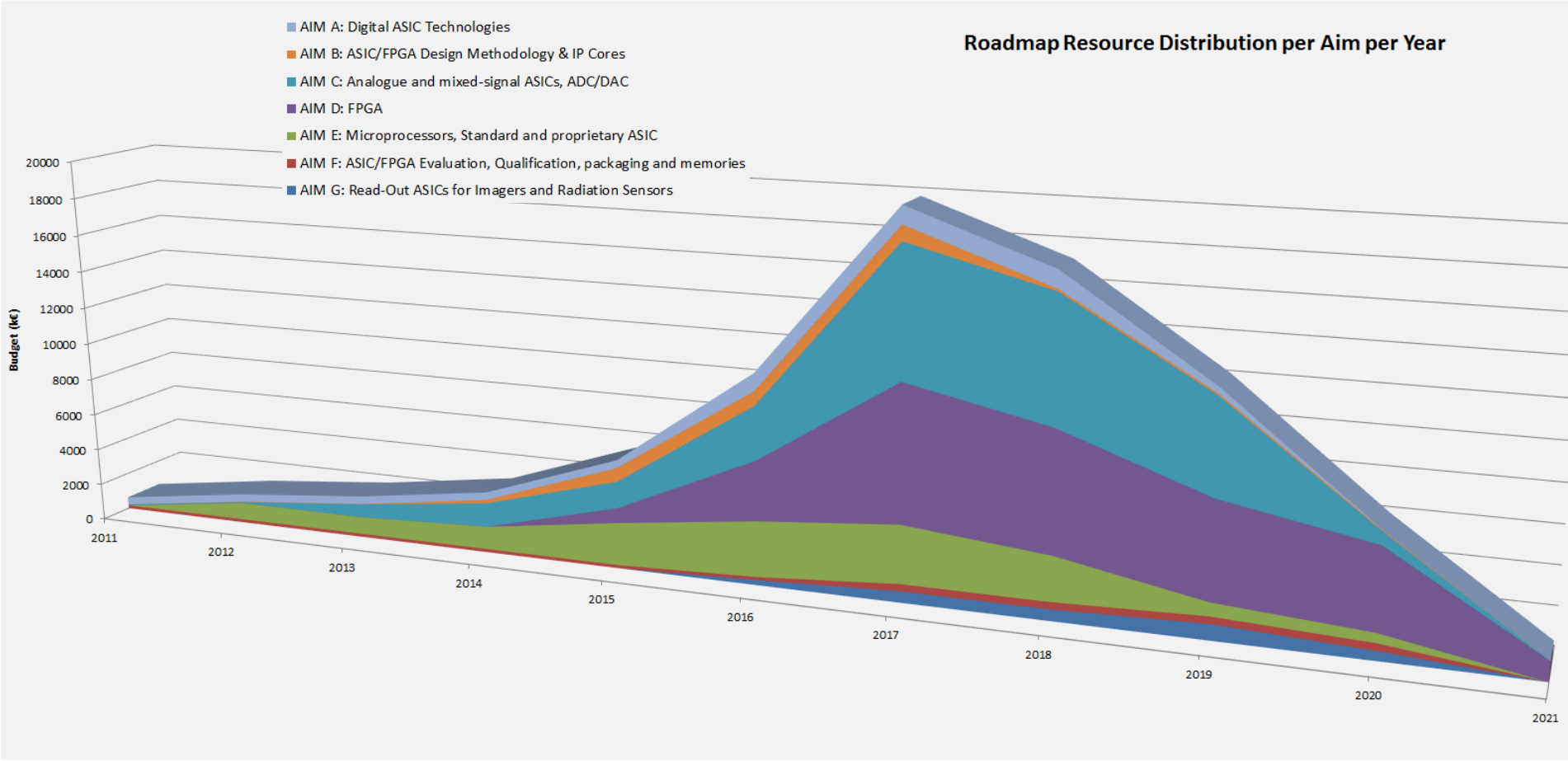


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# Overview of 2016 Roadmap ASIC & FPGA activities

esa
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**1- Standard ASICs & processors (DIGITAL and Mixed-Signal)**
**21 running activities**

**2 - ASIC technology**
**6 running activities**

**3 - IP Cores, FPGA, IC design and test tools & methodology**
**14 running activities**

**46 new activities** being proposed in “Microelectronics: ASIC & FPGA” harmonization dossier 2016 (many in synch with “CTB/ECI5” roadmaps).

There are also many ASIC/FPGA/IP Core/uC/DSP activities in OBPayloadDS and DSOBComputer dossiers

# European DSM processes & libraries for space microchips: 65nm and below

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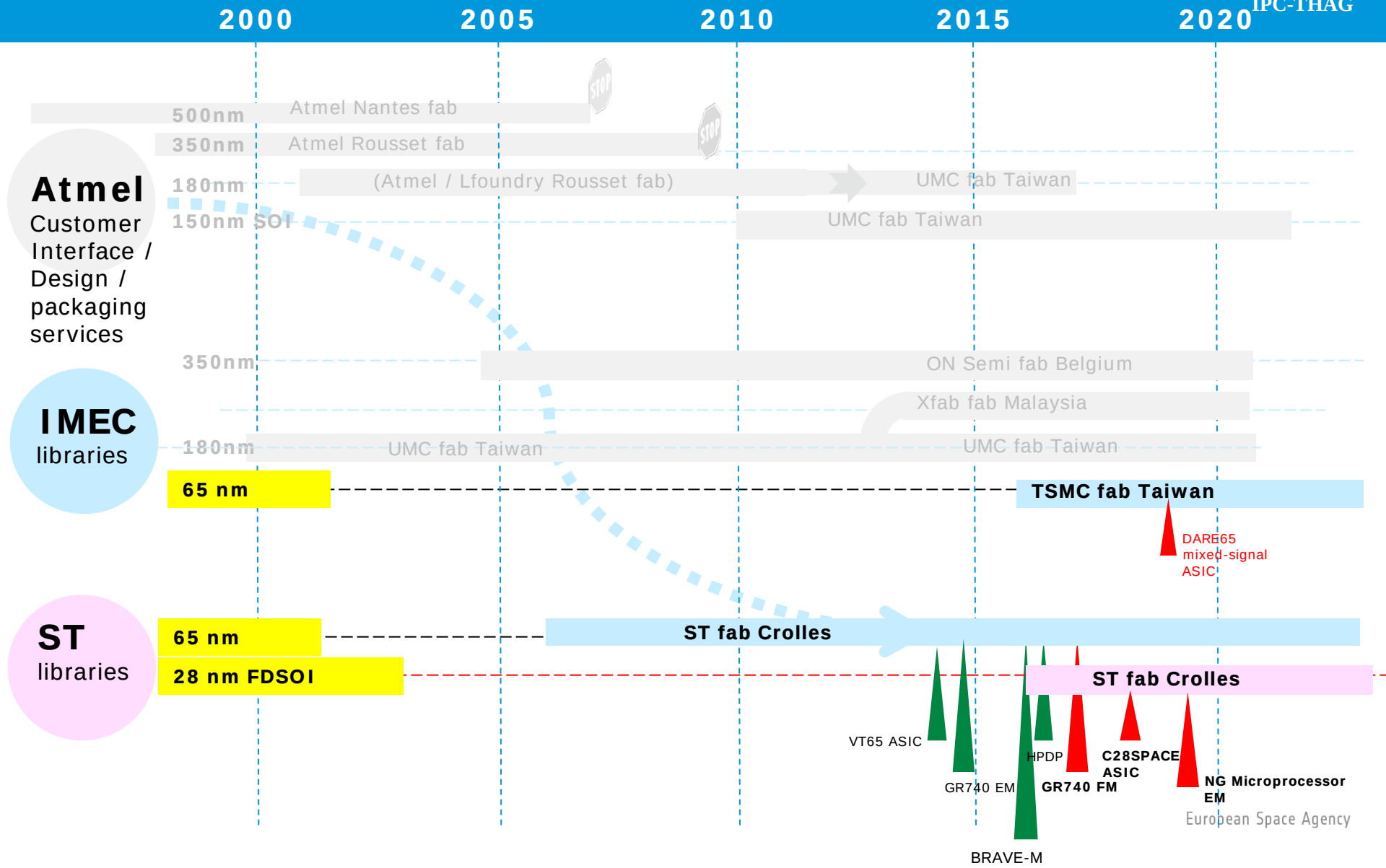

# recent examples of European DSM chips

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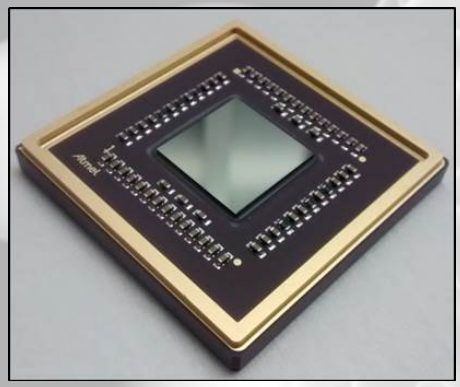
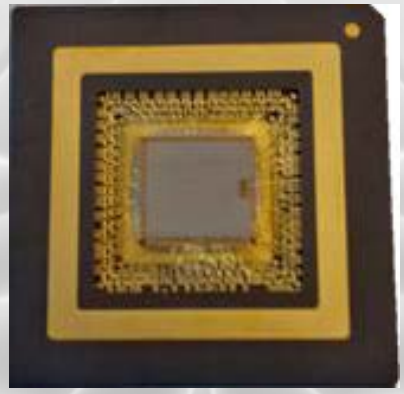
## brains processing the DATA inside our satellites

2015



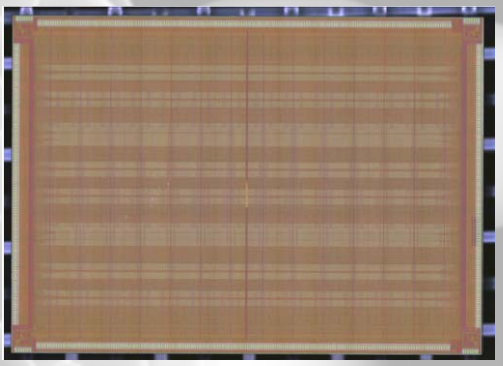
"VT65"
Telecom payload processor
200 $mm^2$
1752 pins
TAS/ST/Atmel/E2V/CNES

2015



"NGMP/GR740"
General Purpose Microprocessor
70 $mm^2$
625 pins
Cobham Gaisler/ST/E2V/ESA

2016



"BRAVE FPGA"
General Purpose
Reprogrammable
170 $mm^2$
625 pins
NanoXplore/ST/ESA/CNES

**All manufactured with 65nm rad-hard microchip technology provided by STMicroelectronics & partners**

# European DSM processes & libraries for space microchips: 65nm and below

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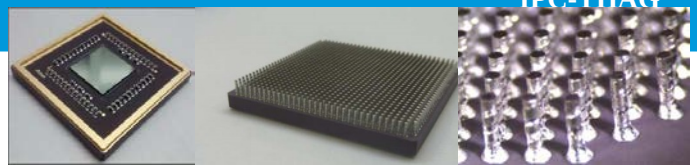

## ASICs

| Accomplished | |
|---|---|
| STMicroelectronics mature design kit/libraries (**C65SPACE**) | 7M€ ESA & CNES<br>8 yrs |
| first users and products (VT65, NGMP, BRAVE-M) | |

| On-going | |
|---|---|
| Space Flip-Chip packaging | 1.8M€ |
| HPDP ASIC | 480K€ |
| DDR IP | 900K€ |
| IMEC development of mixed-signal DARE65 | 3M€<br>2016-2019 |

| Next | Support Needed ! |
|---|---|
| **C65SPACE** ESCC* Qualification (wire bonding and flip chip) | 1.5M€ |
| Development and evaluation of **C28SPACE** (28nm) | 1M€ |
| **DARE65** Analogue IPs (GSTP+TRP) | 3.5M€ |

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* European Space Components Coordination, https://spacecomponents.org/

# European DSM processes & libraries for space microchips: 65nm and below

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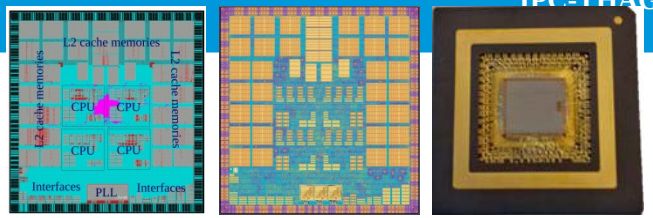


## Micro-processors

| Accomplished | |
|---|---|
| **GR740** Engineering Model (4xLEON4 + peripherals) component manufactured end 2015 with ST C65SPACE | 2.6M€<br>11 yrs |
| Software benchmarks, multi-thread, time-predictability | 1.4M€<br>5 yrs |

| On-going | |
|---|---|
| Finish GR740 validation | |
| HW optimisation for performance, time-predictability | |
| SW environment tools optimisation for performance, time-predictability, debugging | |

| Next | Support Needed ! |
|---|---|
| **GR740** Flight Model & ESCC Qualification | 2M€ |
| High Performance Space Microprocessor: **GR740-HP** (Eng. Model) | 1.5M€ |
| Qualification of new/complementary GR740 SW tools & Operating System | 1M€ |

# European DSM processes & libraries for space microchips: 65nm and below

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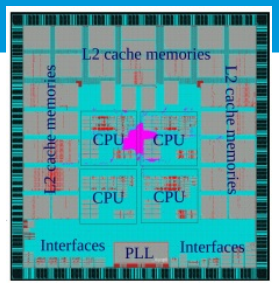
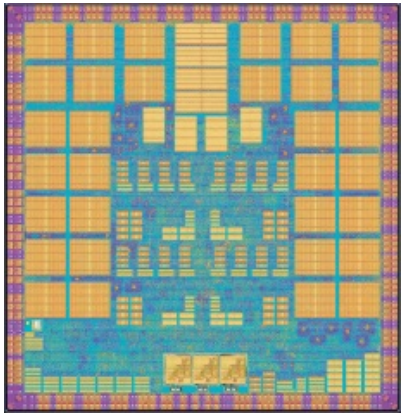
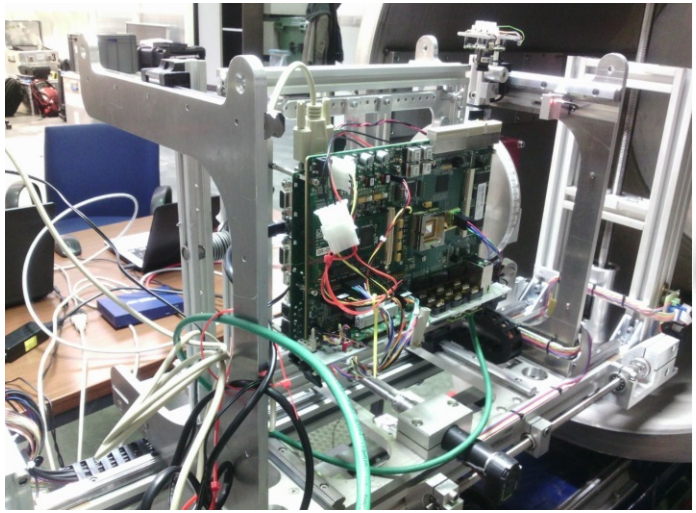
## GR740 4xLEON4 Micro-processor

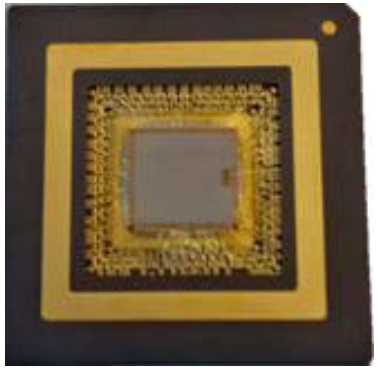



GR740 Evaluation boards



GR740 SEE tests June 2016



# BRAVE NG-MEDIUM Bring Up

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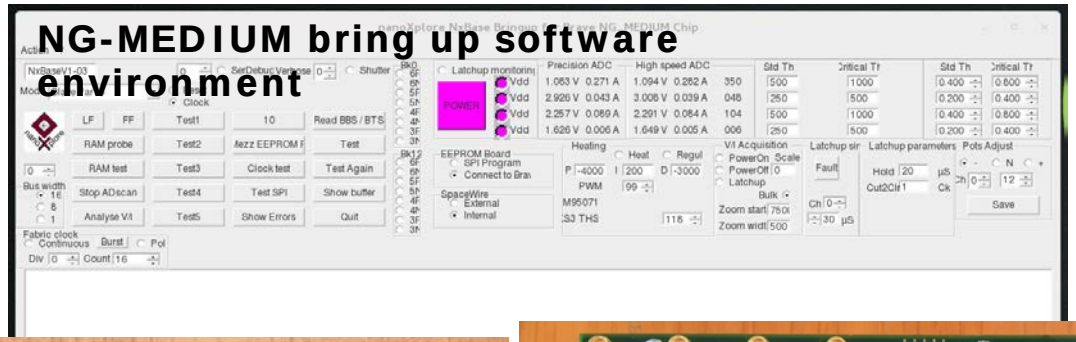



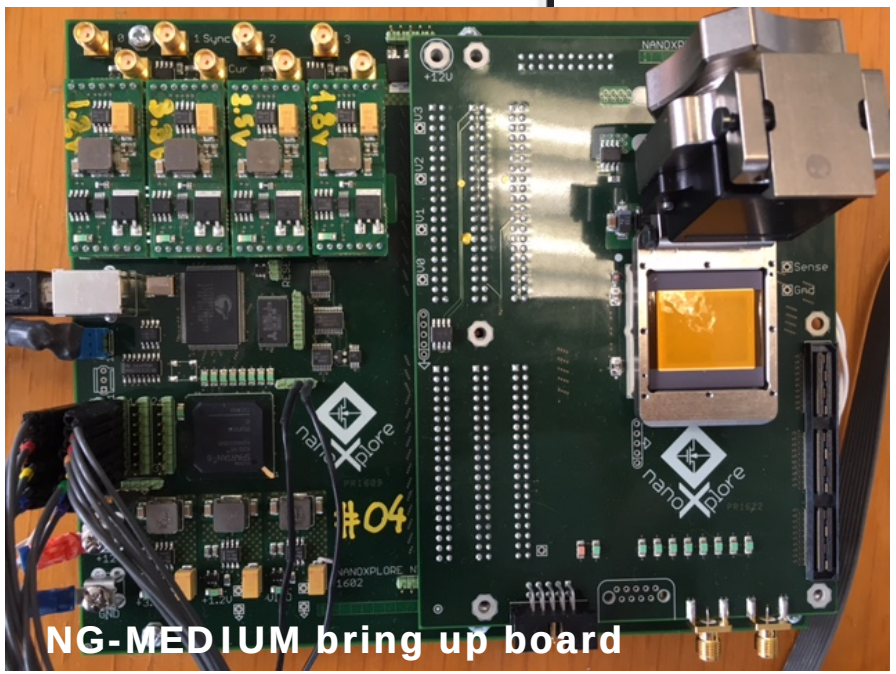


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# CONCLUSIONS on European space DSM

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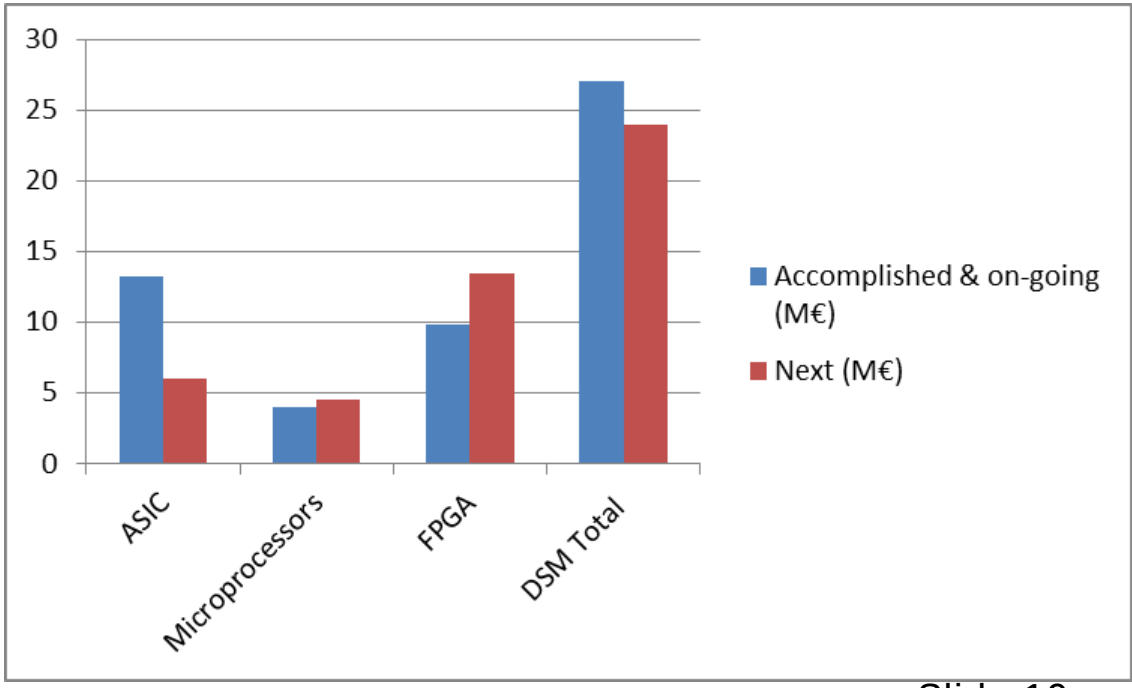
- Deep Submicron (65nm and smaller) ASICs, FPGAs and Microprocessors enable higher performance, miniaturization and less power consumption than older microchip technologies

- First microchips have been manufactured: VT65, GR740, BRAVE-M…

- Urgent new investments needed to finish and qualify 1st products and tools, to develop next generations and more mixed-signal DSM ASIC capability

| | Accomplished & on-going (M€) | Next (M€) |
|---|---|---|
| ASIC | 13.2 | 6.0 |
| Microprocessors | 4.0 | 4.5 |
| FPGA | 9.8 | 13.5 |
| **DSM Total** | **26.8** | **24.0** |



# Closing remarks on ASIC & FPGA Roadmaps

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- *ASICs and FPGAs are key for all missions*
- *ME dossier has been updated to reflect inputs from industry and delegations, and better coordination between dossiers*
- *New roadmap has been compiled and consolidated*
- *More FPGAs and fewer ASICs, as gate capacity and performance increases and because differences in price (NREs and per part) and development time*
- *European space ASICs vendors with European rad-hard libraries and IP, some manufacturing in Asia (fabless) , but*
  - *Many silicon fabs still in Europe, strong in niche, specialized, mixed-signal*
  - *huge dependence on US (ITAR) space FPGAs (all manufactured in Asia).*
  - *Many European ASIC/FPGA design groups and test houses with space know-how*
- *European supply chain fragmented and international ownership makes space quality control difficult*
- *Technology changes call for updates and tailoring of old quality standards*
- *Space complex general use ICs difficult/expensive to develop and maintain, market sustainable only by parallel commercial (non-space) high volumes, and* ***institutional (Agencies and EC ) support***

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***-> important to coordinate and harmonise efforts and priorities***

# More info

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**ESA Microelectronics section activity:**

http://www.esa.int/TEC/Microelectronics

**Technology harmonisation dossiers will be available here:**

http://www.esa.int/Our_Activities/Space_Engineering_Technology/About_strategy_and_harmonisation

https://tec-polaris.esa.int/pls/adm/webloginext.login

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# BACK UP SLIDES

# Microprocessors: better performance thanks to DSM technology

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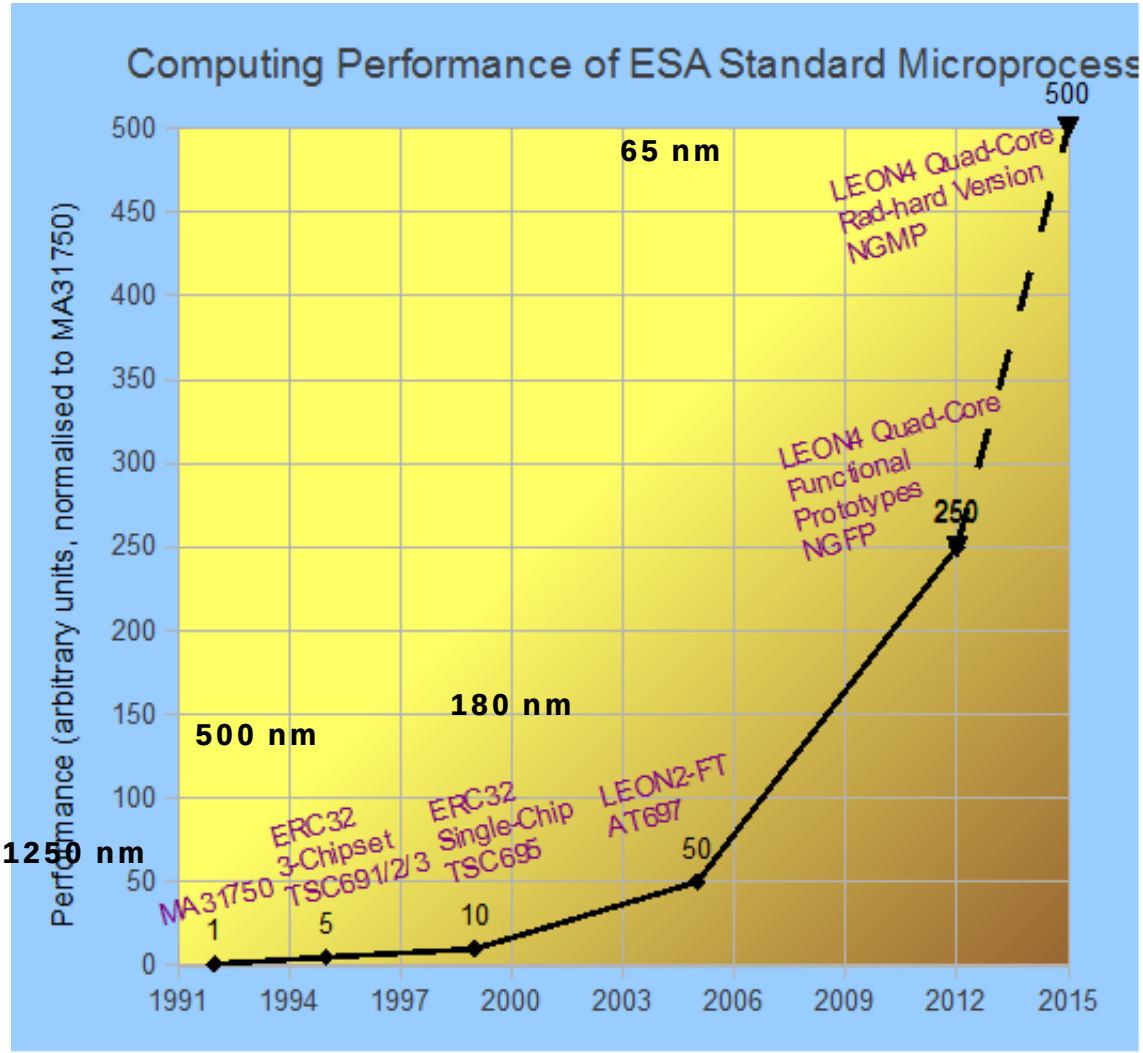


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# FPGAs: better performance and functional capacity thanks to DSM technology

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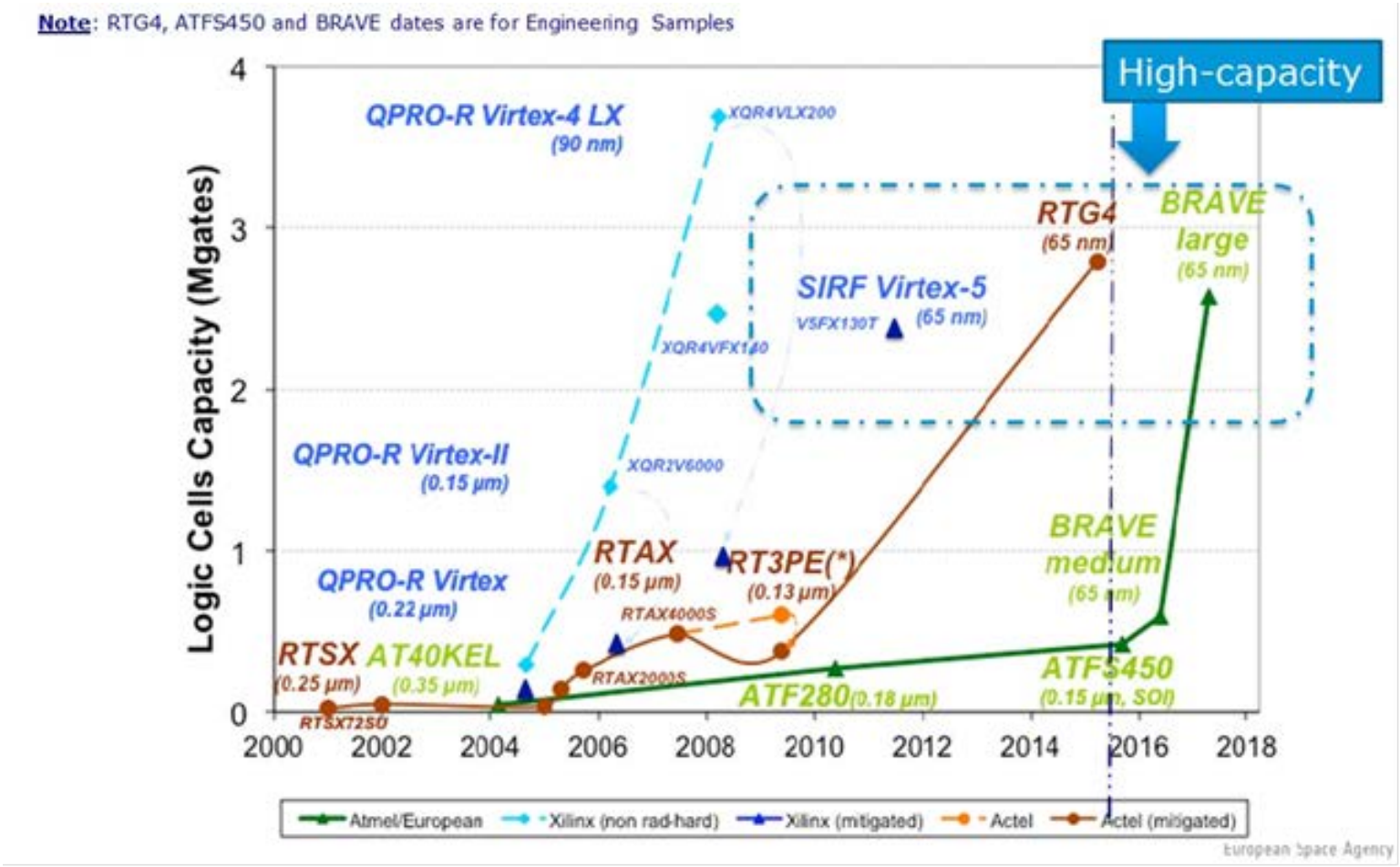

# Space ASIC Technology Observatory ( draft 2 – Jan 13th 2016)

DIGITAL