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Industrial Policy Committee

Technology Harmonisation Advisory Group

On-Board Payload Data Processing Roadmap
Issue 4.2

TEC-EDP*

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Contents

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1. Technology Overview
2. Mission Needs, Market Perspectives, Applications
3. Strategic Interest and Development Aims
4. Overview on Tech Development Lines / Roadmap
5. Summary / Closing Remarks

Technology Overview

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- **OBPDP is a key element of the overall data flow**
- Needs to cope with **increased raw data rate and data volumes**, while a **downlink bottleneck remains**
- Includes **data pre-processing, transport, storage, intelligent selection, compression, encryption**
- OBPDP is an **enabling technology for scientific and commercial successes**. It is also a **significant technology driver** for other areas.

OBPDP covers the development and application of technology related to:

Data processing architectures for P/L

Payload computers

Reconfigurable processing modules

DAQ I/O modules

Processing & compression algorithms

Encryption for P/L data

Payload mass memories

Digital Signal Processors & boards

High speed links & on-board networks

Payload support software

Wireless technologies for P/L apps

Technology Overview: Synergies among the three Data Systems Dossiers

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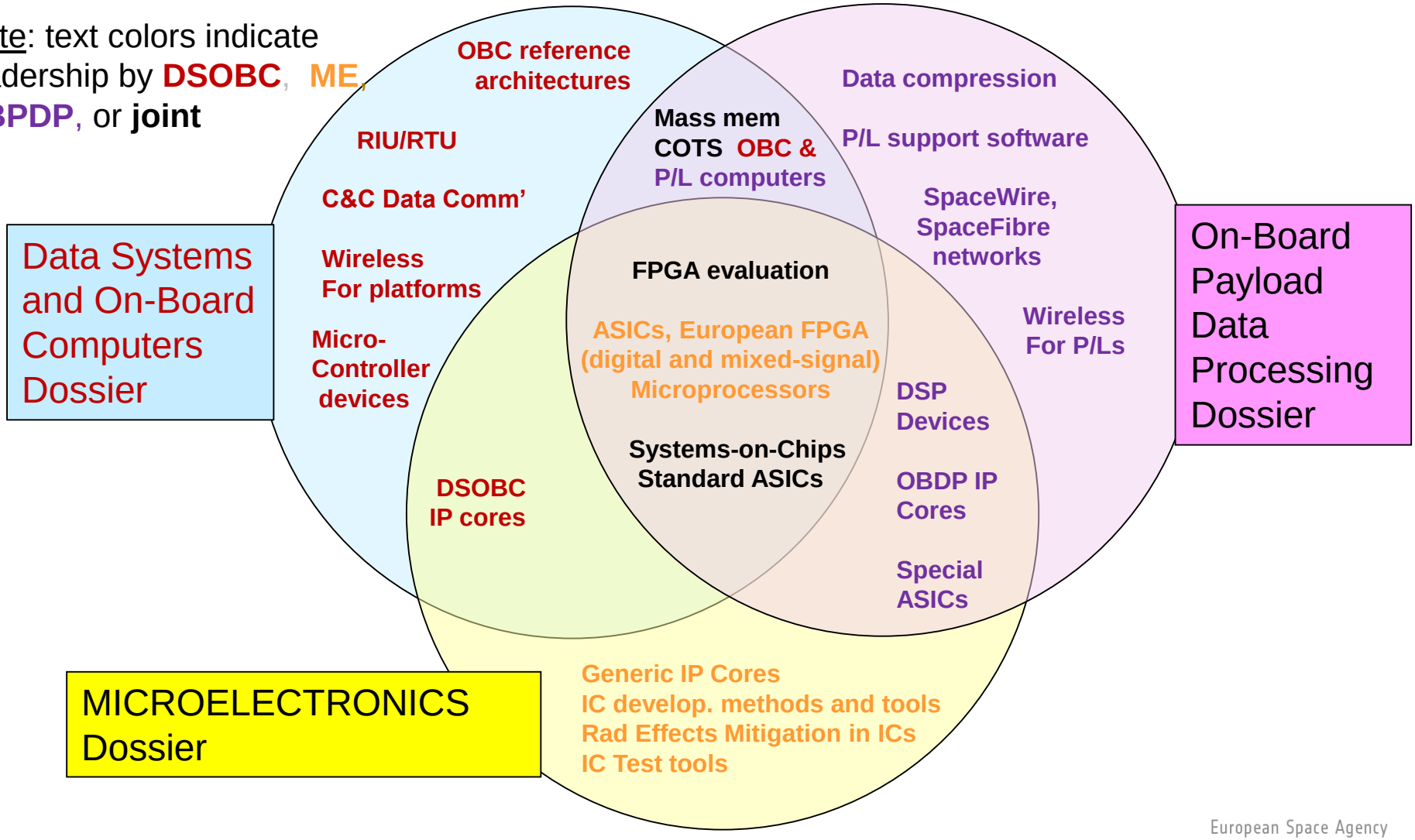
Note: text colors indicate leadership by **DSOBC**, **ME**, **OBPDP**, or **joint**



MISSION NEEDS/MARKET PERSPECTIVES
Application to missions

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	Technology	Science &Robotic Exploration	Earth Observation Missions	Manned Spaceflight &Launchers	Telecom Applications	Navigation
1	Rad-hard High Performance Digital Signal Processors	++	+	+	+	+
2	High Speed and Very High Speed Links & Networks	+	++	+	++	+
3	Mass memories for payload applications	++	++	o	o	
4	App.- Specific solutions based on ASIC/FPGA technology	+	+	+	++	++
5	Data compression algorithms, S/W, IP cores, chips	+	+	+	o	
6	Specific multi/manycore GPP/DSP/NoC based proc.	+	+	o	o	+
7	Scalable and integrated payload computers	+	+		o	o
8	High performance COTS based computers	+	+	o	o	
9	General purpose processors with high performance co-processors	+	+	o		++
10	Reconfigurable processing modules for payloads	+	++		o	o
11	Reconfigurable array data processor chips	o	+		++	
12	High speed encryption for payload applications		+	+	o	o
13	Wireless technologies for payload applications	+	o	o	o	

++ enabling technology useful for a wide range of applications
+ useful for a wide range of applications
o useful for some applications
[ ] application area is not a driver for this technology

MISSION NEEDS/MARKET PERSPECTIVES
Application to missions

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- **Science and robotic exploration -** missions need to manage the usual bandwidth bottleneck which drives on-board autonomy and processing needs; for high data rate instruments (spectrometers, imagers…) high performance acquisition chains and efficient memories and networks (2,3) as well as reliable high processing performance devices (1,6,9,10) are required, meeting key mass and power constraints
- **Earth observation** - the evolution in sensor resolution and dynamic range has led to a dramatic increase of sensor bandwidth and data volume, creating significant bottlenecks in downlink capacity, and a need of very high on-board data processing capabilities (1,2,3,4,6,8,9,10) for data pre-/post-processing and compression (5,12)
- **For manned spaceflight & launcher** safety is a key requirement, and implies the need for reliable processing platforms , links, processors (1,2,4,8,12) and IP (5).
- **For Telecommunications**, a desired key feature for future platforms is the capability to reconfigure the payload functionality and therefore allow the use of new coding standards which can be enabled by suitable processors (1,2,4,8,10,11).
- **For Navigation,** application specific ASIC/FPGA solutions and algorithms, fast and reliable processors and networks are among the key needs (1,2,4,6, 12)

MISSION NEEDS/MARKET PERSPECTIVES
European strategic interest

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- **Development of advanced digital processing technology and architectures** forming the basis for future high performance Payload Data Processing
- Definition of scalable and powerful architectures based on **high performance networks**.
- Support the **standardisation of interfaces and communication protocols**.
- Development of **key network devices (including internal network) and IP** for SpaceWire and SpaceFibre links.
- **Ensure the timely availability of key components** with adequate performances (processors / DSPs, FPGAs, ASICs, ADC/DAC, HSSL) with an appropriate TRL at competitive cost and **strive to close technology gaps** that affect European competitiveness.
- **Support company initiatives to offer key components** for Payload Data Systems in Europe.
- **Make ESA-supported IP and chip developments accessible to European Industry**, and maintain and enlarge the IP-core service for ESA projects.
- **Address and support payload processing dedicated software development** in parallel, for example for pre-/post-processing, optimise download data volume, payload operations, …
- **Support the development of tools** required to validate instantiations of the reference architecture for specific mission needs.
- Advance the **standardisation of data compression algorithms and techniques** optimised for space application.

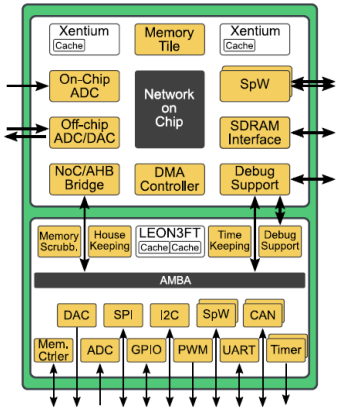
ROADMAP
Aims

- Aim A: DSP Device and Processing Modules
- Aim B: On-board Networks
- Aim C: Solid State Mass Memory Modules
- Aim D: I/O and Data Acquisition Modules
- Aim E: Data Compression and Processing Techniques and Systems
- Aim F: Reconfigurable Processing Modules
- Aim G: Payload Support Software
- Aim H: Wireless Technologies for Payload Applications

  - The developments aims (A) to (F) are the same as in the previous roadmap in 2011.
  - New aims for payload support software (G) and wireless technologies (H) were introduced to better accommodate other developments
  - Sequence of Aims does not reflect a prioritization

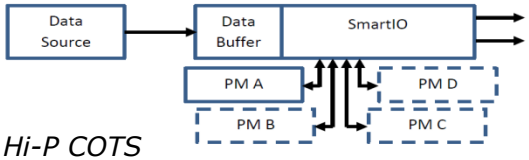
Aim A: DSP Device and Processing Modules

- **Next Generation High Performance Floating Point DSP** - Requirements consolidation, IP prototyping, license procurement, ASIC development, ASIC qualification and board / SDE developments
- **DSP IP core developments** – completion of Xentium® fixed & floating point IP core for ESA IP portfolio
- **Scalable Sensor Data Processor (GR732)** - development completion, flight batch manufacturing, board developments, and SDE / library upgrade



SSDP ASIC

- **XPP** - flight model development
- **High Performance COTS based computers** – COTS processor / DSP assessments and evaluation; Hi-P CBC II module development



Hi-P COTS based computer Mk. I

ROADMAP
Aim B

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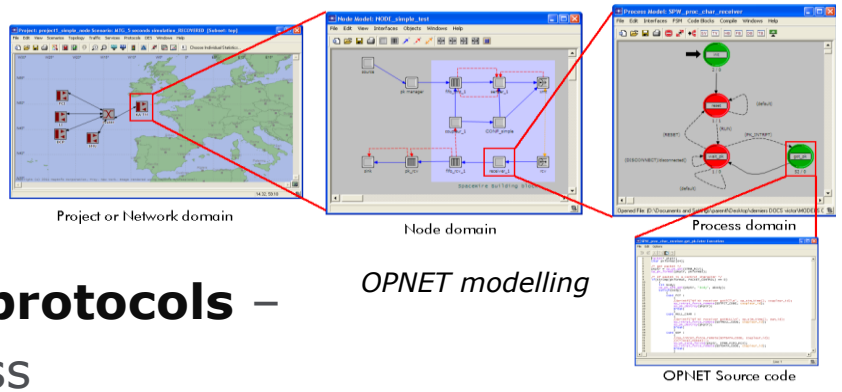
Aim B: On-board Networks



OPNET modelling

- **SpaceWire and SpaceFibre network model** developments
- **Development / upgrades of SpW protocols** – including NDCP, TDS, SpW-D2, N-Mass
- **Development of new SpW IP cores** that support the upgrades / protocols
- **SpaceFibre network terminal chip** – IP development / prototyping, ASIC development, qualification – high priority
- **SpaceFibre routing switch** - IP development / prototyping, ASIC development, qualification – high priority
- **SpaceFibre multilane and optical link developments** – development, prototyping, optical link H/W standardization

ROADMAP
Aim C & D

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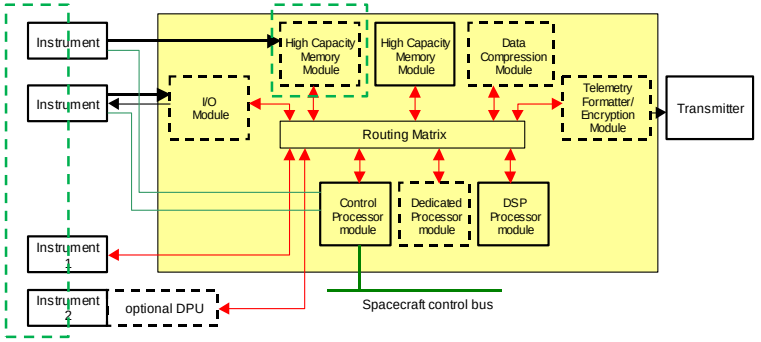
Aim C: Solid State Mass Memory Modules

- **Future very high speed mass memory** – technology studies and breadboarding activities

P/L architectue incl. MM and DAQ / Frontends



Aim D: I/O and Data Acquisition Modules

- **High speed multilane SpFi frontend –** board development for EO/TC
- **Visual monitoring camera** development
- **Highly integrated video acquisition chain** development
- **Secure / high datarate telemetry encoders** – development of building blocks addressing industry needs

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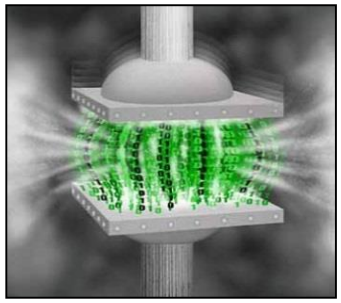
Aim E: Data Compression and Processing Techniques and Systems



- **Future on-board Processing algorithms** – study on processing and information extraction
- **Data compression algorithm development** – lossless and lossy algorithms including hyperspectral compression and compressive sensing studies
- **Processing modules** – SAR data compression, correlator and control unit
- **Combined compression / encryption** – secure implementation of CCSDS 122 standard

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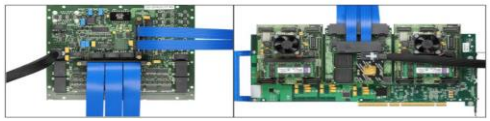
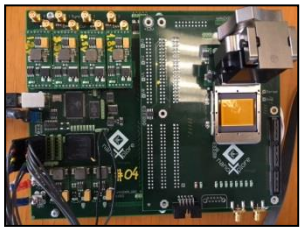


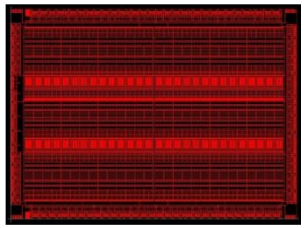
DRPM

Aim F: Reconfigurable Processing Modules

- **Reconfigurable Payload Processor** – requirements study, development and evaluation
- **FDIR techniques** for reconfigurable processors
- **Telecommunication processor** – flexible reconfigurable board for telecom applications

=> Priority to European FPGAs
where they meet the requirements





BRAVE FPGA

ROADMAP
Aim G & H

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Aim G: Payload Support Software

Autonomous operations example: planetary rovers

- **Smart On-board Data Pre-processing** – incl. data fusion and selection
- **Autonomous Operations Planning** – on-board operations planning based on priorities, requirements, resources
- **DSP Software Libraries** for new DSP ASICs and IP cores

Aim H: Wireless Technologies for Payload Applications

- **Low Energy Wireless Imaging System** – wireless camera prototype
- **System level studies** – impact assessment of using wireless on S/C
- **Wireless Sensor / Instrument links** – prototyping of link technologies for payload applications (complementary to DSOBC activities)

ROADMAP
Proposed development approach: Resource Distribution

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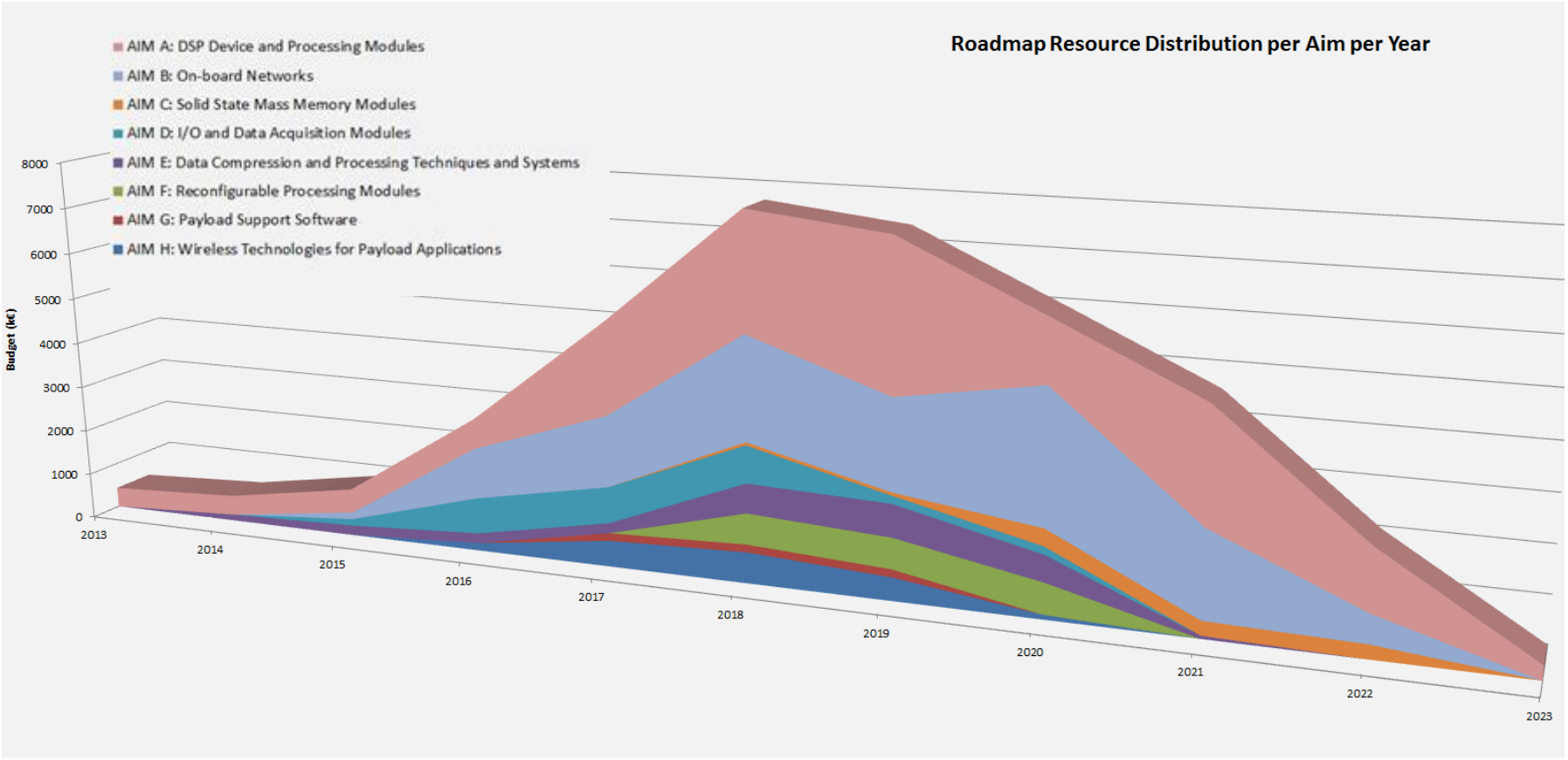

The **NEW yearly reference budget based on the 2011-2015 timeframe expenditures** is (15.3 M€ + 7.2 M€) / 6 years ≈ **3,751k€**

Summary – OBPDP

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- *OBPDP dossier has been updated to reflect inputs from industry and delegations, and improved alignment of dossiers*
- *New aims have been introduced to cover work done previously and address new challenges (wireless, P/L support SW)*
- *Links between dossiers have been clarified (OBPDP and ME / OBPDP and DSOBC)*
- *Activity Roadmap was adjusted taking into account THAG feedback and latest industry inputs on SAVOIR, DSP, and others*

- *New roadmap has been compiled and consolidated; 42 new activities are proposed for 2016-2023 timeframe; new total roadmap budget is 38.6 M€ (2011: was 22 M€);* ***new reference budget is 30 M€ / 3.75 M€ per year***

Closing remarks – OBPDP

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- *Top priority is to ensure adoption of SpaceFibre without delay in European avionics and P/L architecture designs*
  - ***Completion of standard, development of chips*** *is highest priority*
- *New high priority / high urgency electronic parts supporting OBPDP applications are essential:*
  - ***Need significant funding for pre-development*** *and* ***development & qualification*** *of* ***DSM chips*** *(SpFi, DSP SoC …)*
  - ***Need for both High Performance DSP ASICs & boards and reconfigurable FPGA & modules*** *in support of future OBPDP hardware – developments need to start / be supported*
  - ***European Industry Competitiveness and non-Dependence*** *rely on* ***European component sources***
  - *Component cost = 35% of OBPDP turnover:* ***ensure availability of suitable European components !***
- *OBPDP implementation will be performed in close collaboration with related domains*

Backup VG: TEC-ED funding needs for component qualification

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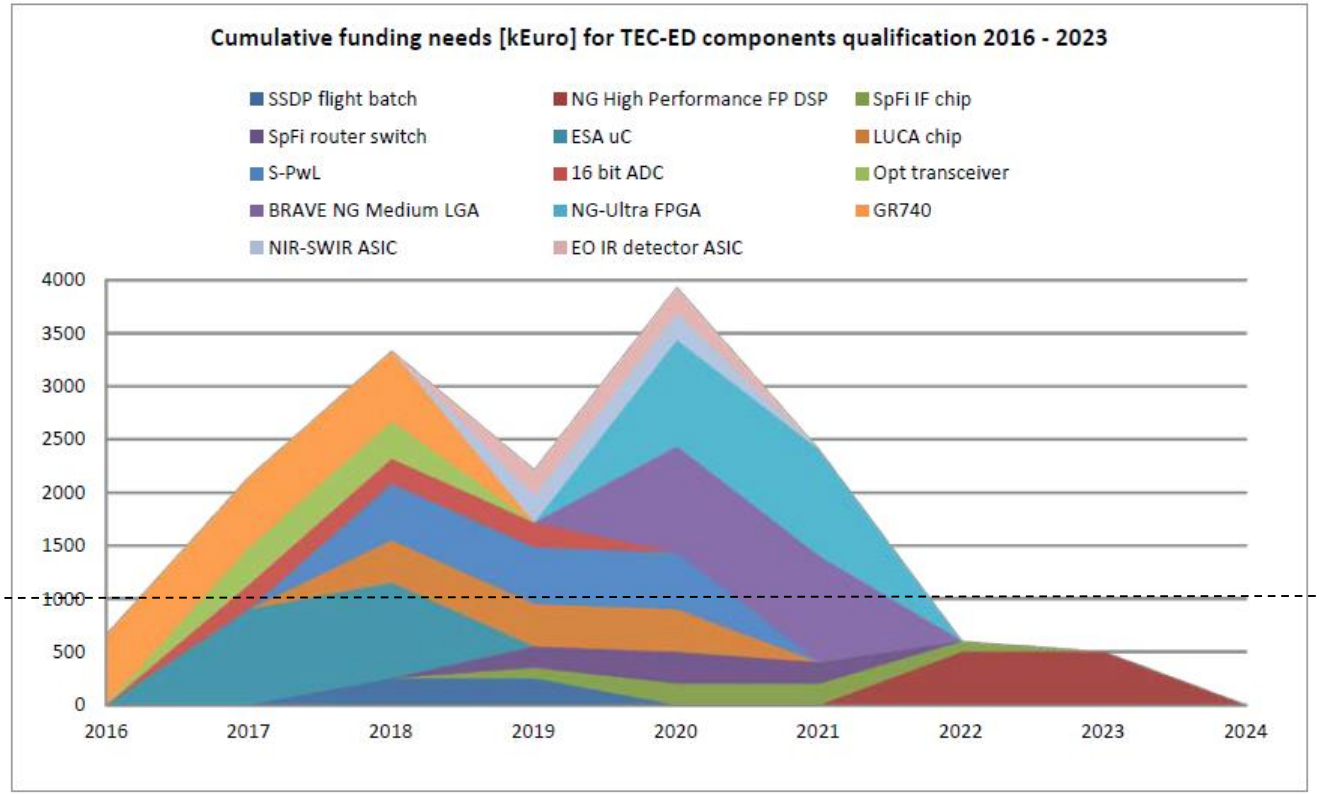
The problem:

The **accumulated** TEC-ED (**ME, DSOBC, OBPDP** combined**)** need for funding component qualification/ evaluation (only ASICs; no packages, ASIC process technologies etc.) is ca. **2.5 Meuro annually** for the next 5 years.

The **reported expectations for the next ECI program** is only **~1 Meuro per year**

=> **If not changed, dramatic underfunding must be expected**, with consequences for European component/equipment/asso -ciated industry



Data taken from latest DSOBC / ME / OBPDP roadmaps