
# *Modeling of Irradiation Effects in sub-N7 CMOS Logic Devices Using Layout-Based Design*

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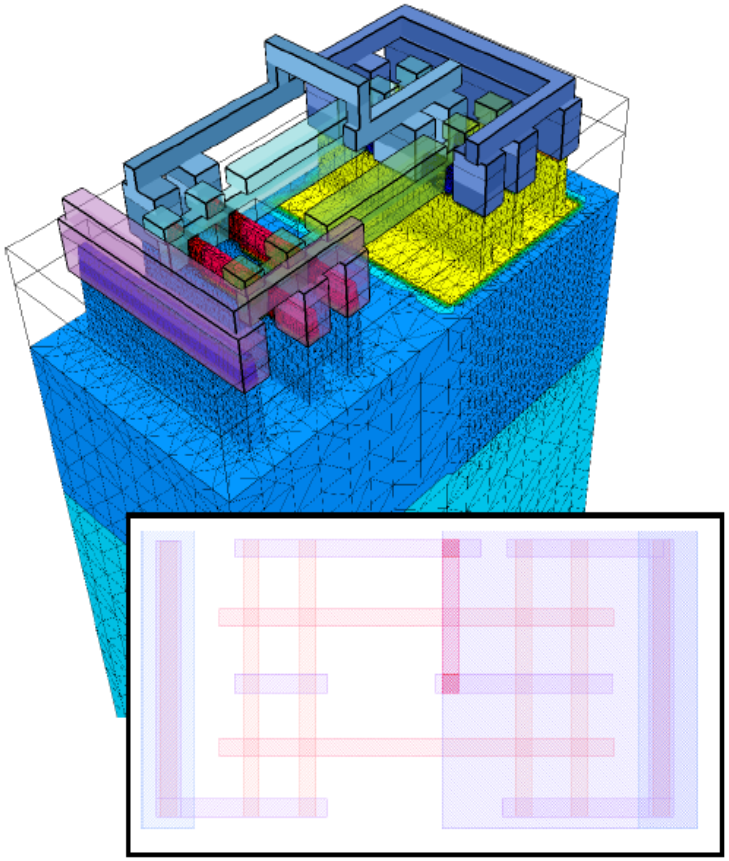
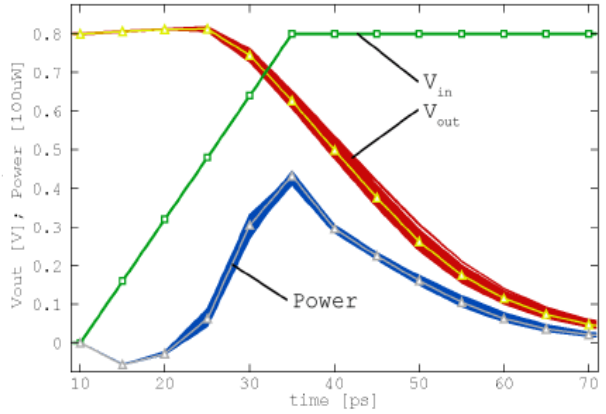
*Pete Truscott (Kallisto Consultancy)*

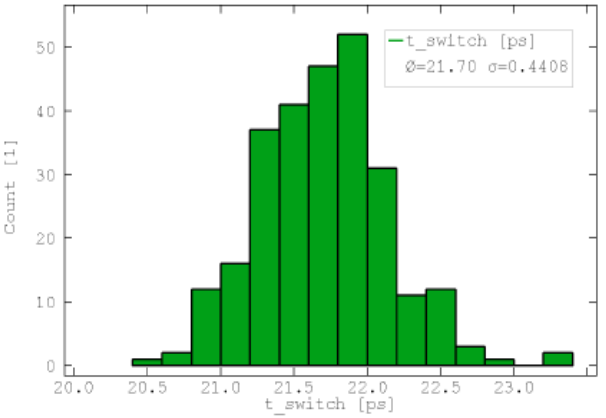
# Model Suite for full Logic Cells

## TCAD based analysis of a full NAND Gate:

## Power, Performance, Area, Variability, and Reliability





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# GTS Framework – Minimos NT

MINIMOS-NT

## Semiconductor device simulator

- General-purpose semiconductor device simulator
- Planar and non-planar CMOS
- Power electronics based on wide band gap materials

## Non-volatile memory

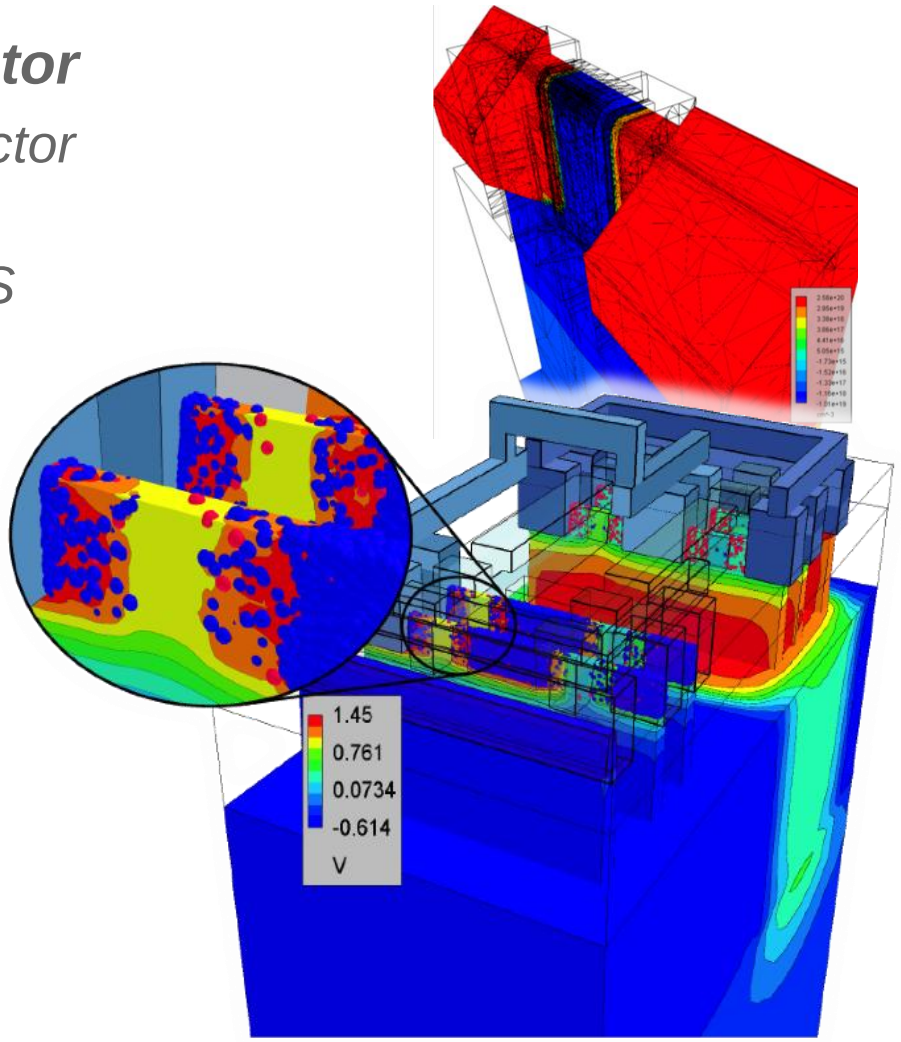
- Mixed-mode simulation
- Discrete traps and dopants

## Variability time zero:

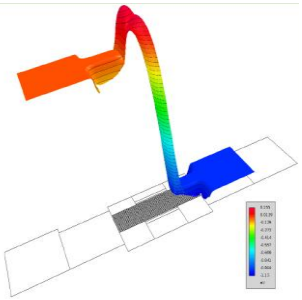
RDD, MGR, LER

## Statistical reliability:

BTI, HCD



# Effects in Emergent Devices

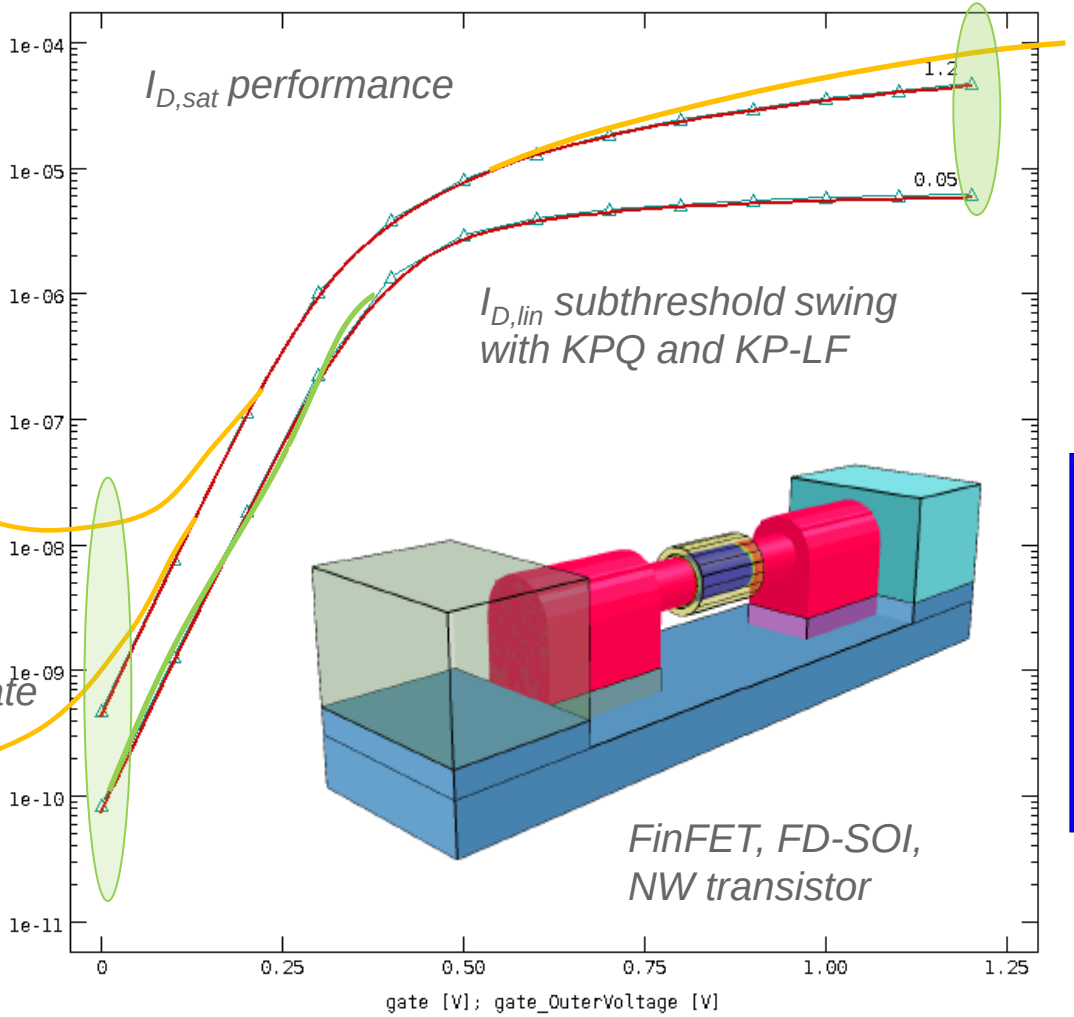


Non-local QTBM tunneling model

BTB tunneling

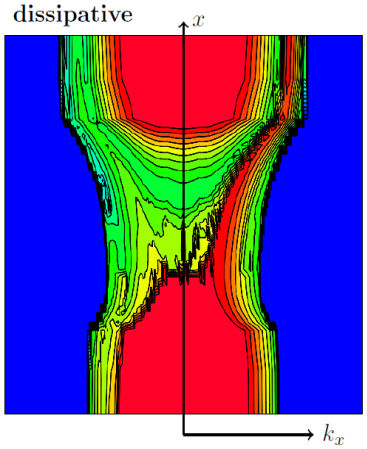
Direct tunneling SD barrier & Gate barrier

**Off-current $I_{off}$ incl. leakage**




**On-current $I_{on}$ ballistic effects**

PS-Transport solving SB-BTE




and scattering

FinFET, FD-SOI, NW transistor



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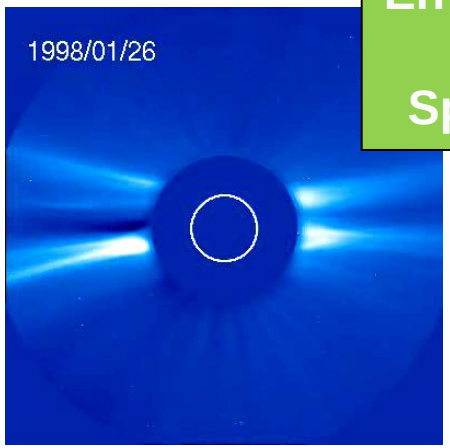
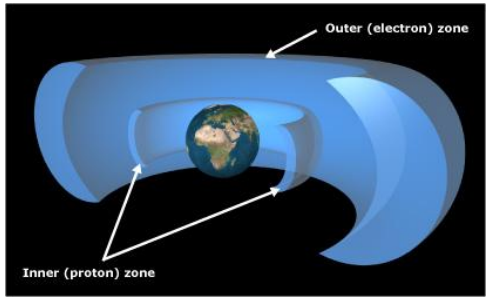
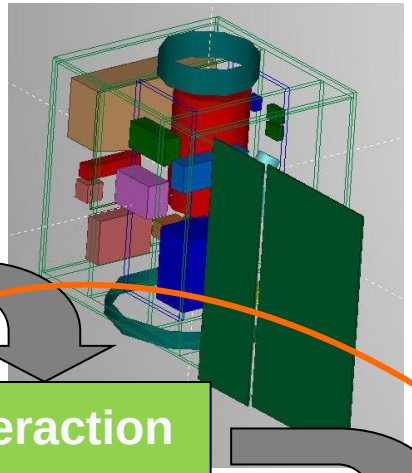
# Radiation Effects Prediction Process

External Environment

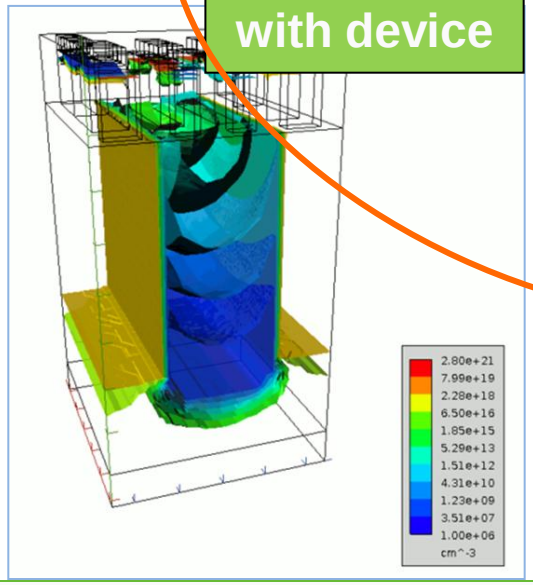


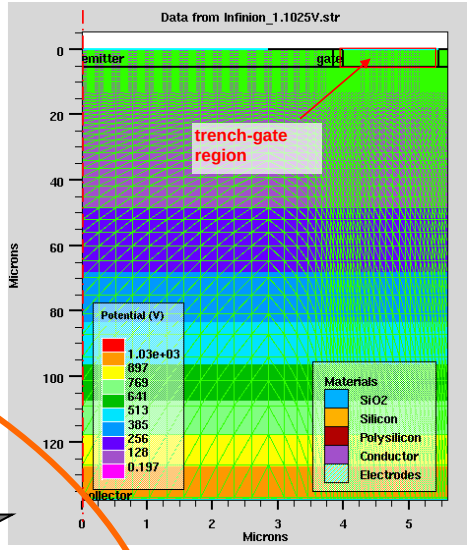




Environment inside Spacecraft



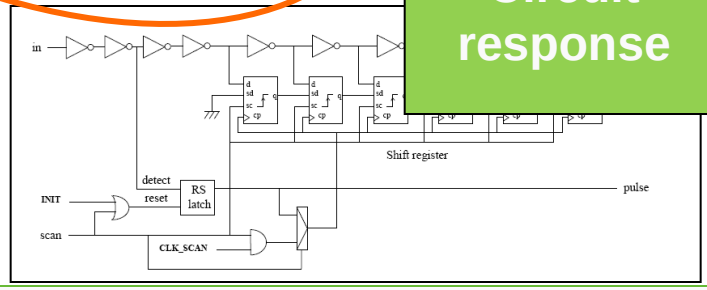
Interaction processes with device




Q Collection & device response

Circuit response



# Deep Sub-Micron CMOS Radiation Effects (DESMICREX)

*Sponsored by ESA to*

- *develop simulation environment for modelling DSM CMOS radiation effects*
- *Identify example DSM CMOS technology and implement in test vehicles*

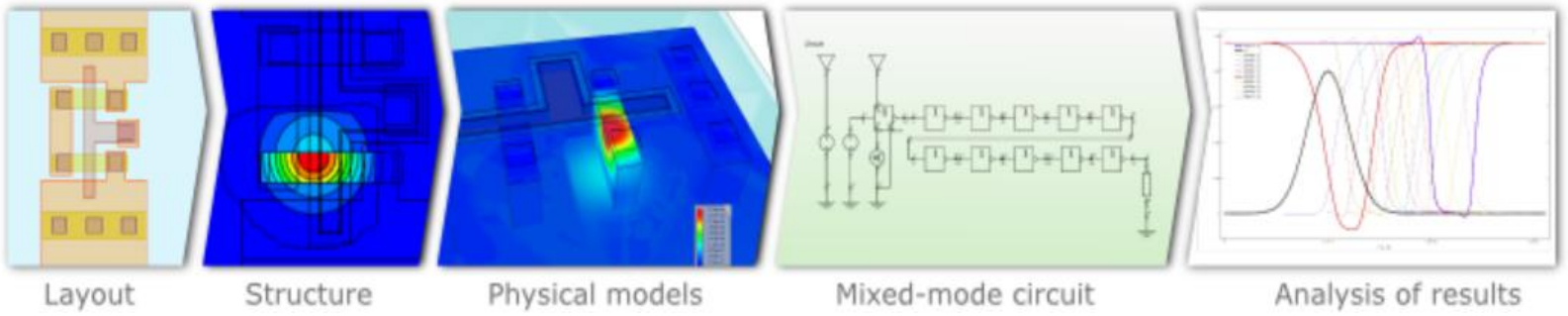
*Simulation environment based on Geant4/GRAS operating within GTS Framework with MINIMOS-NT*

*Significant strides made:*

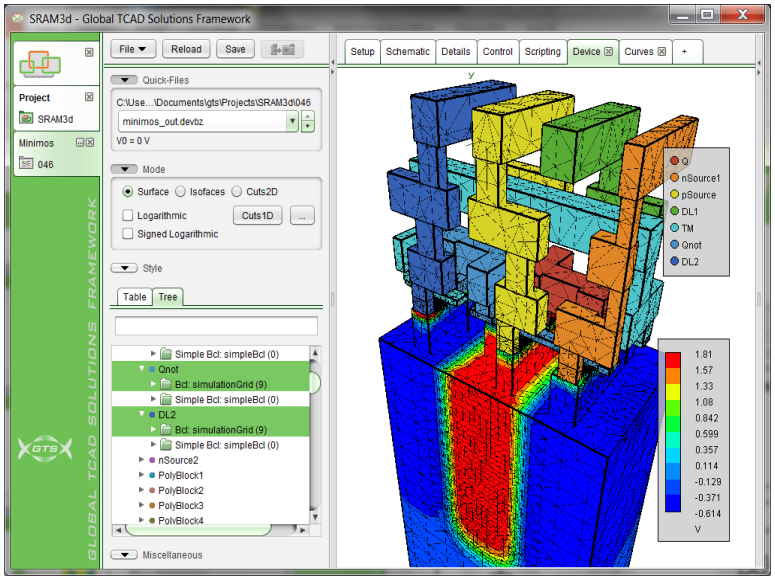
- *Version of GRAS which can read-in standard format microelectronics structures and simulate ion tracks*
- *Cost-effective multi-platform/multi-CPU TCAD Framework to treat mixed-mode MINIMOS-NT +BSIM4*

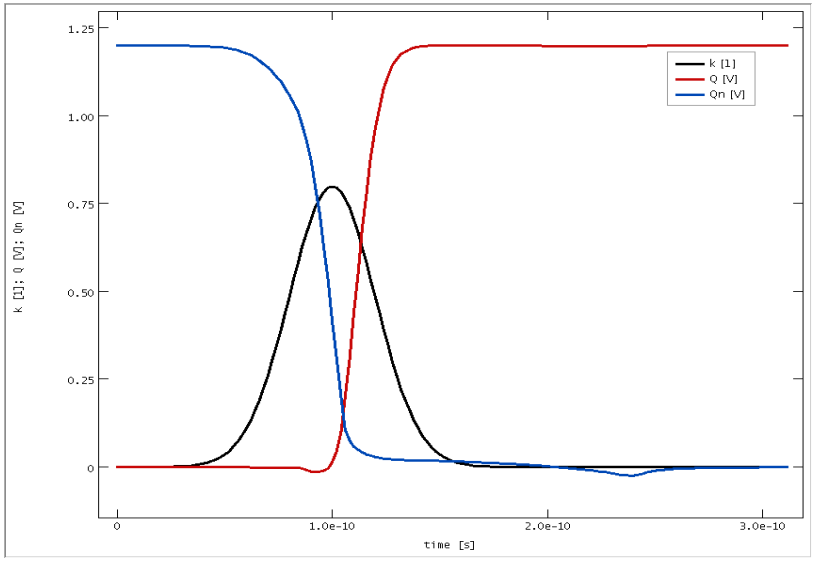
*No follow up development on Geant4/GRAS integration*

# Tool Flow for Irradiation Simulation




*Simulation of a single event transient (SET) on an inverter chain*
*(From **device layout** to **circuit simulation**, all set up in less than **1 hour**)*




*Simulation of a single event up-set (SEU) on a 90nm 6T-SRAM*



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# *Modeling of Radiation Effects in Flash Memories*

*Transnational project started 2016 and funded by*

- *Austrian Research Promotion Agency FFG*
- *Chinese Academy of Science*

*Partners*

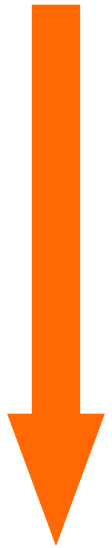
- *Device production and testing by Institute of Microelectronics – CAS / Synchrotron Beijing*
- *Device physics modeling by TU Wien and GTS*
- *Geant4 integration by Pete Truscott and GTS*

*Revamped effort of combining Geant 4 and Device TCAD*

- *Great advances in GTS device structure generation*
- *Require solution compatible with GRAS license and GTS IP*

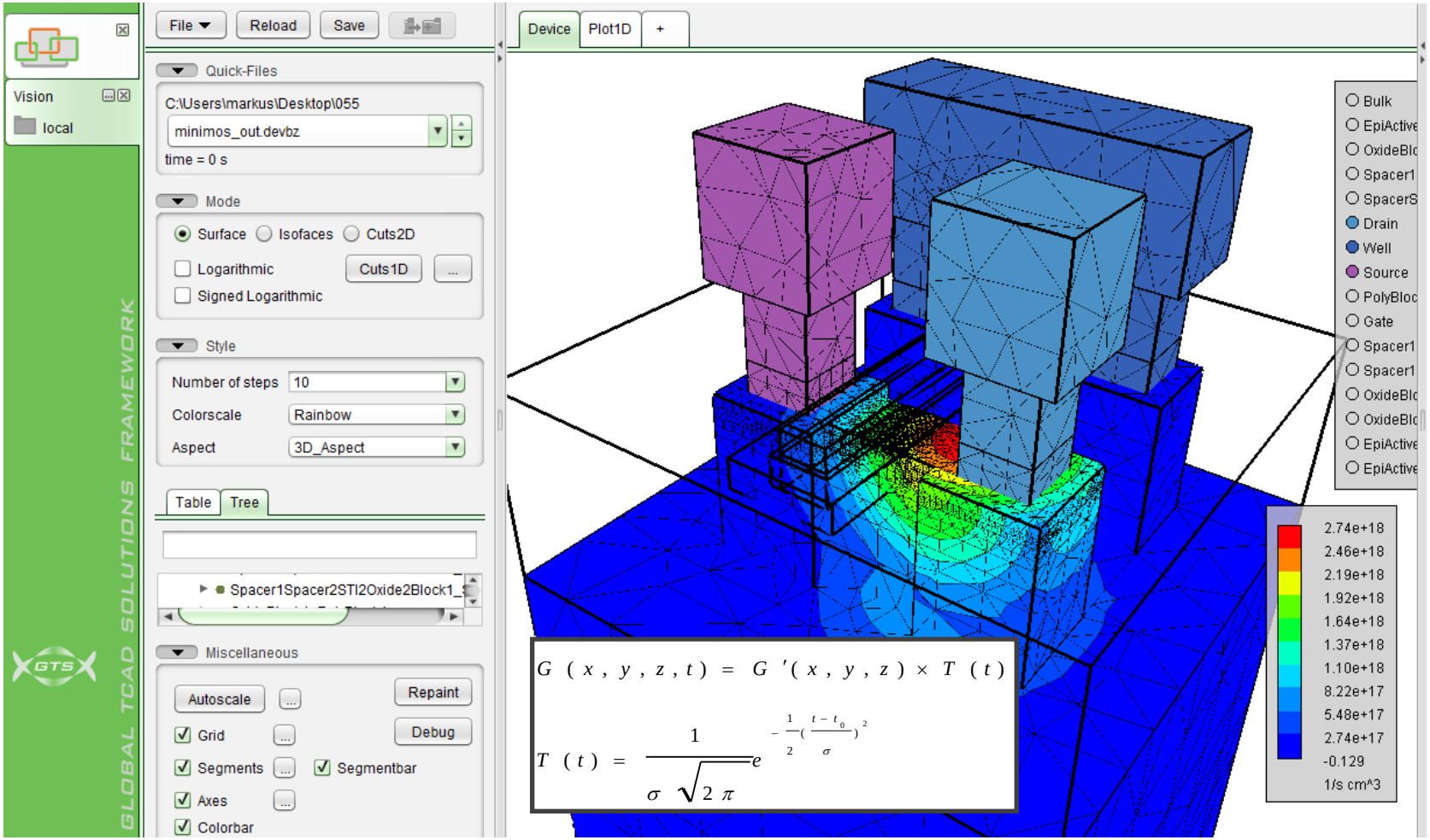
# Requirement for Radiation Effects Analysis and Priority

1. Single event latch-up
   - Effects of angle, impact position, temperature
2. Single event transients / DSETs + Multiple Transients
   - Effects of angle, position, clock-freq, cross-talk, temperature
3. Single event upsets / multiple-cell upsets
   - Effects of angle, position, temperature
4. Single event hard error (stuck bits)
5. Total ionising dose
   - Intra- and inter-device leakage across STI
6. Dose enhancement effects
   - Use of Cu and other high-Z materials



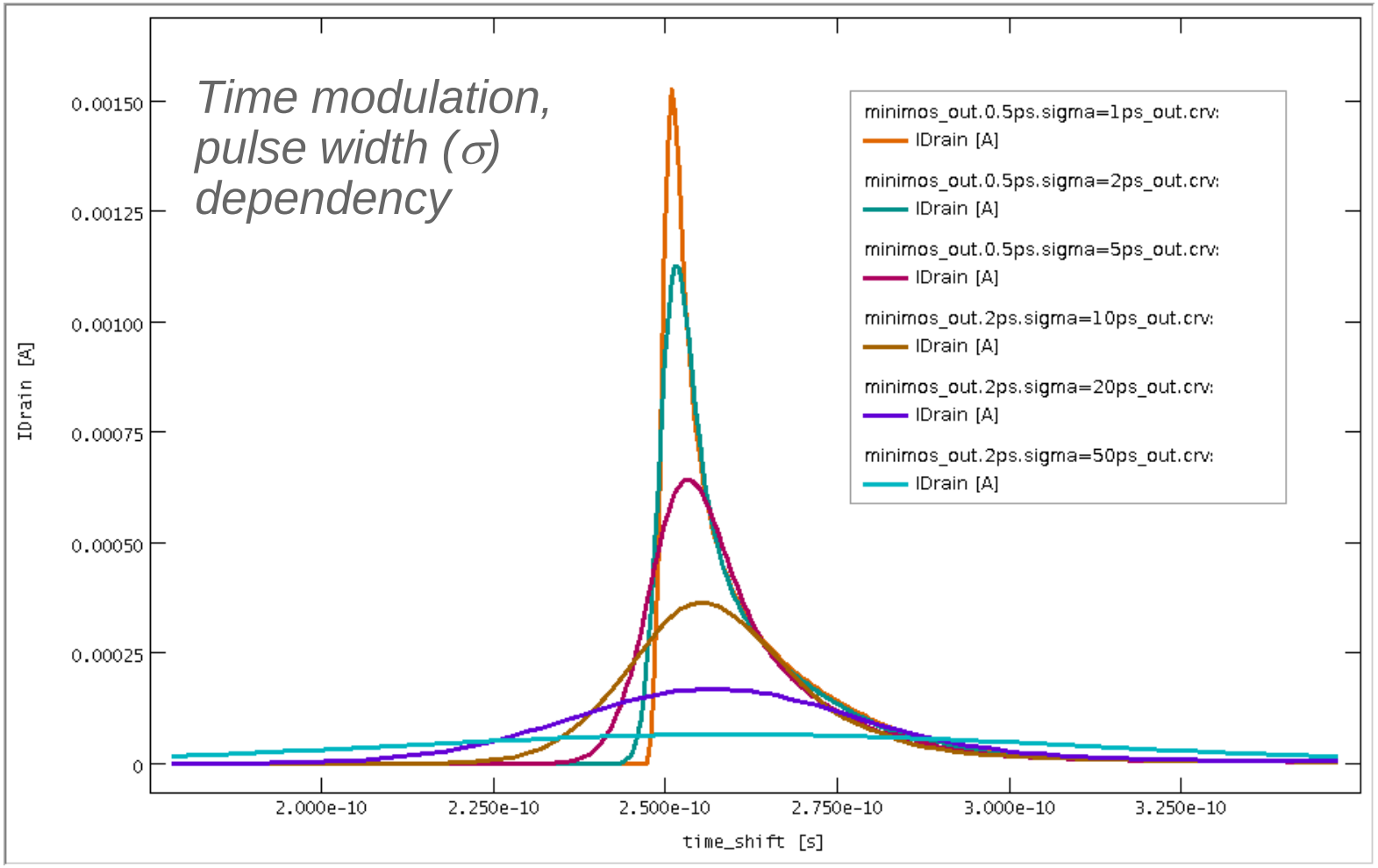
**Decreasing priority**

# SET - Charge Collection



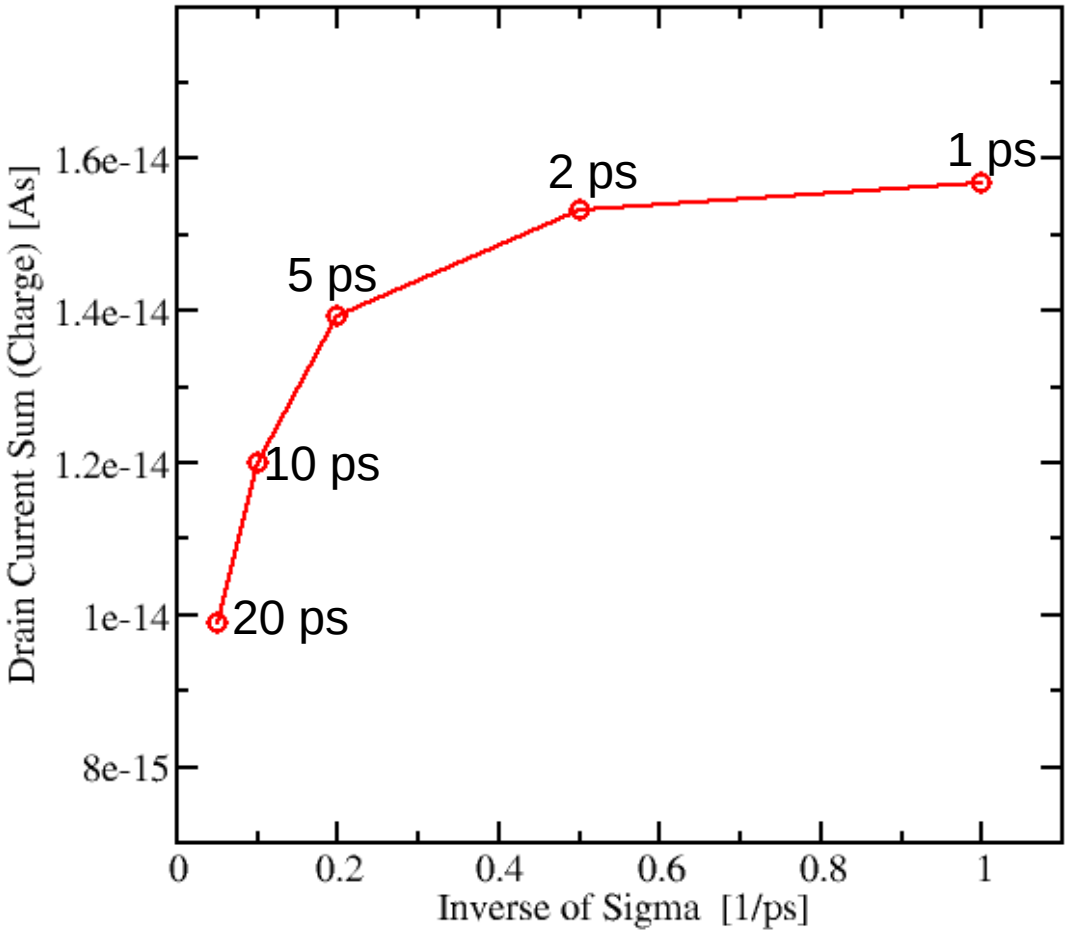

*Spatial generation rate profile*

# SET - Charge Collection




*Contact current over time*

# SET - Charge Collection




*Charge collection over inverse sigma (1/σ)*

$$G(x,y,z,t) = G'(x,y,z) \times T(t)$$

$$T(t) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{t-t_0}{\sigma}\right)^2}$$

*Time modulation, pulse width (σ) dependency*



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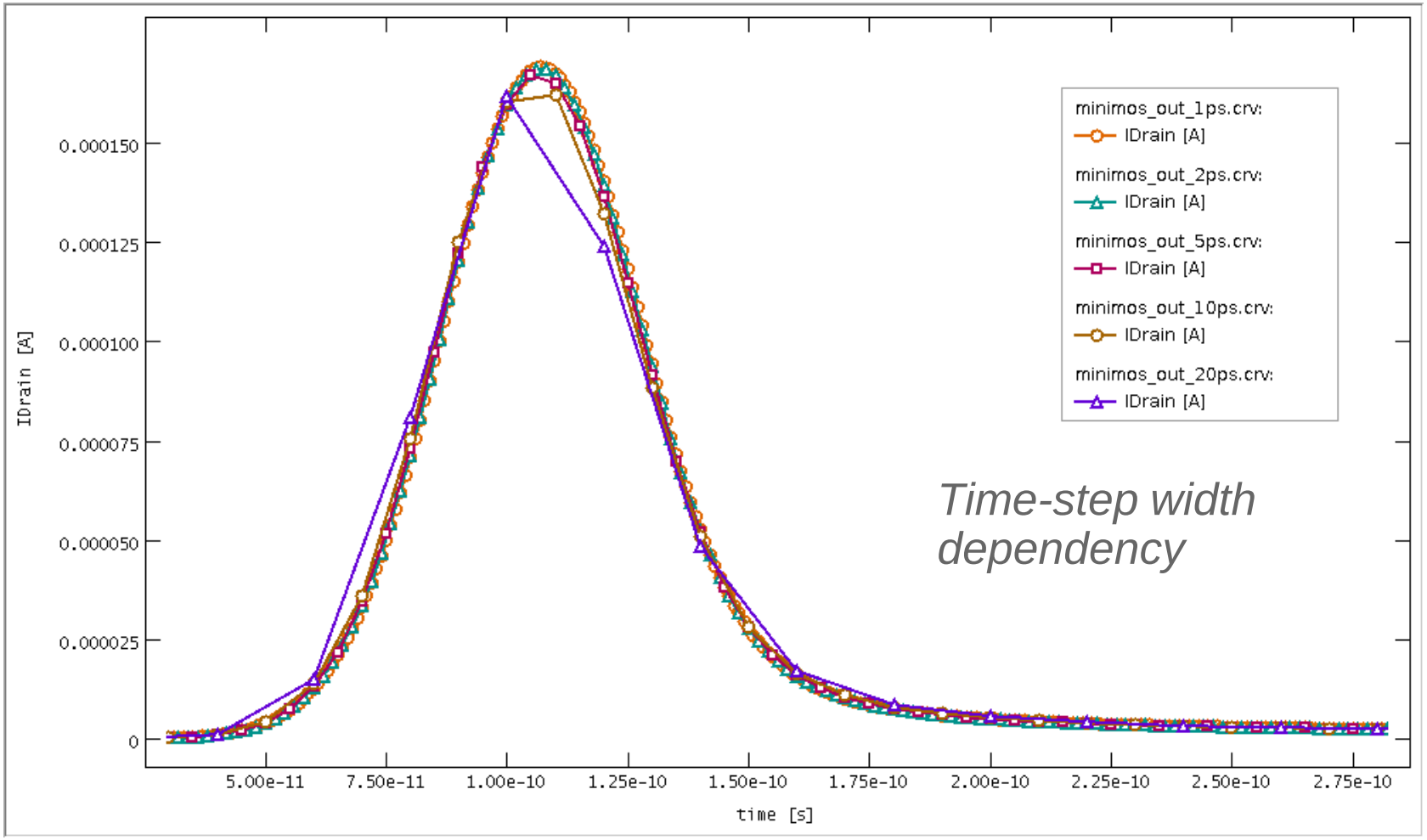
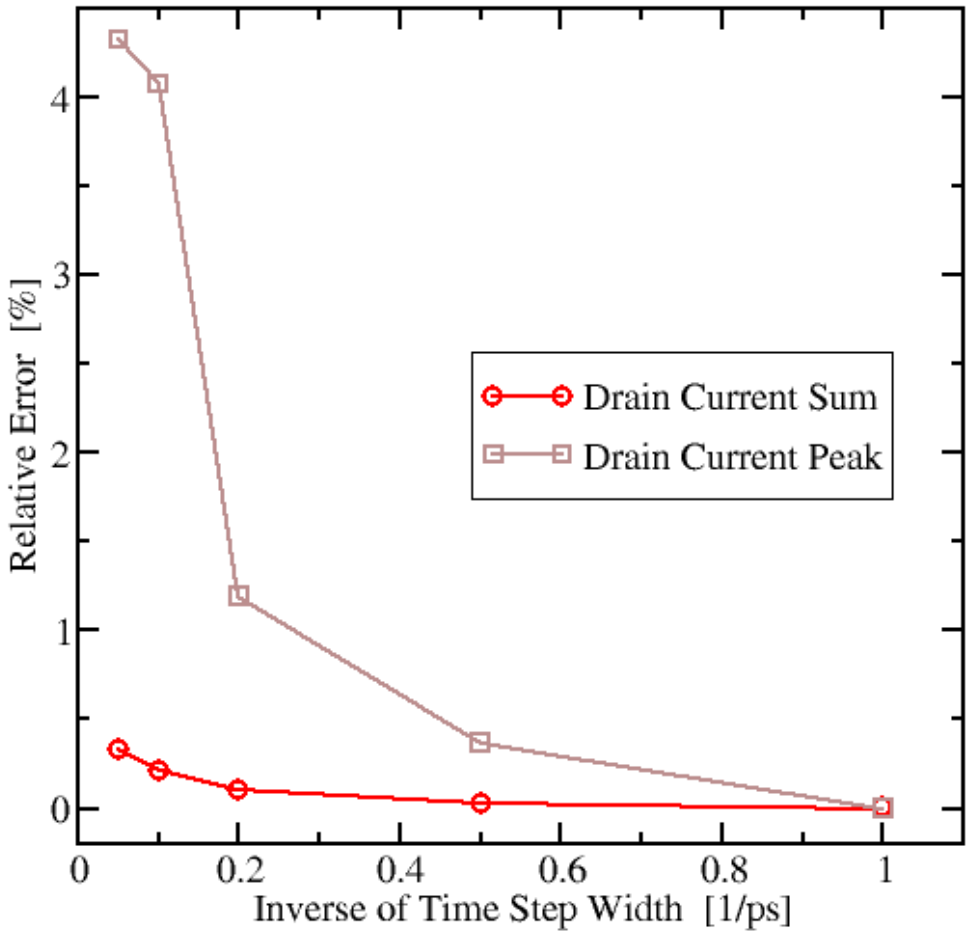
# SET – Time Discretization




*Contact current over time*

# SET – Time Discretization

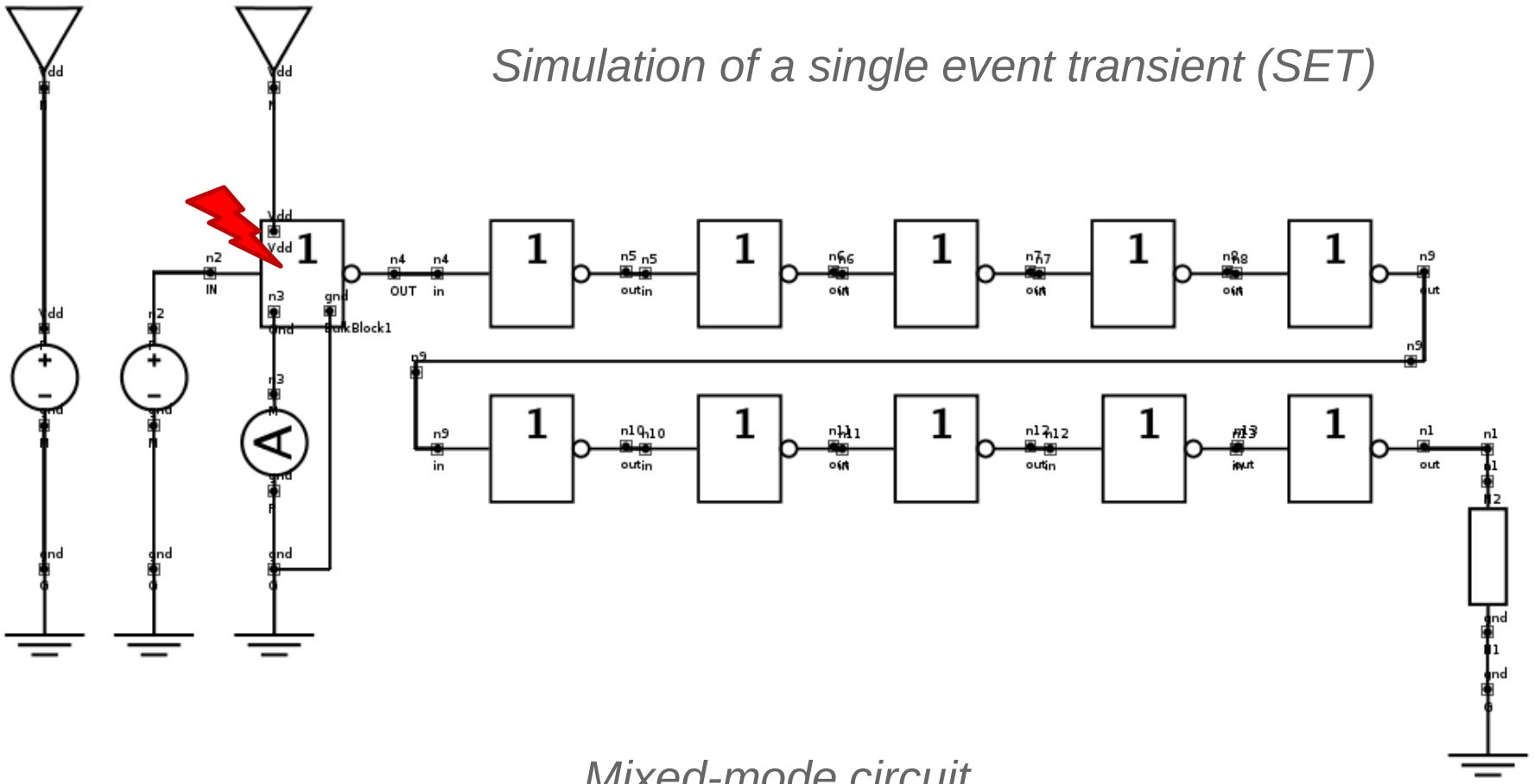



*Time-step width dependency*

*Charge collection over inverse step width $1/\Delta t$*

# Inverter - SET

Circuit




*Simulation of a single event transient (SET)*

*Mixed-mode circuit*



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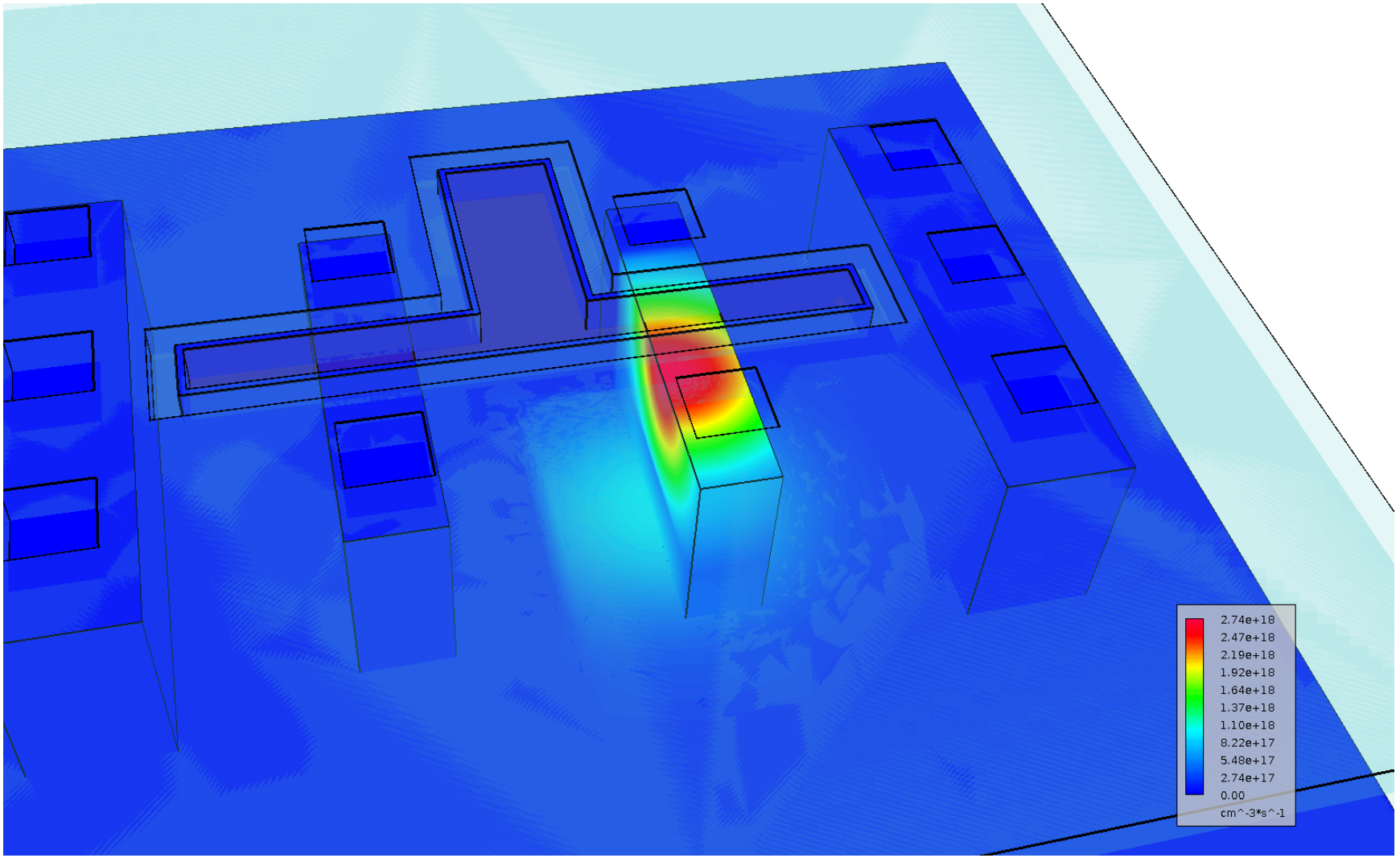
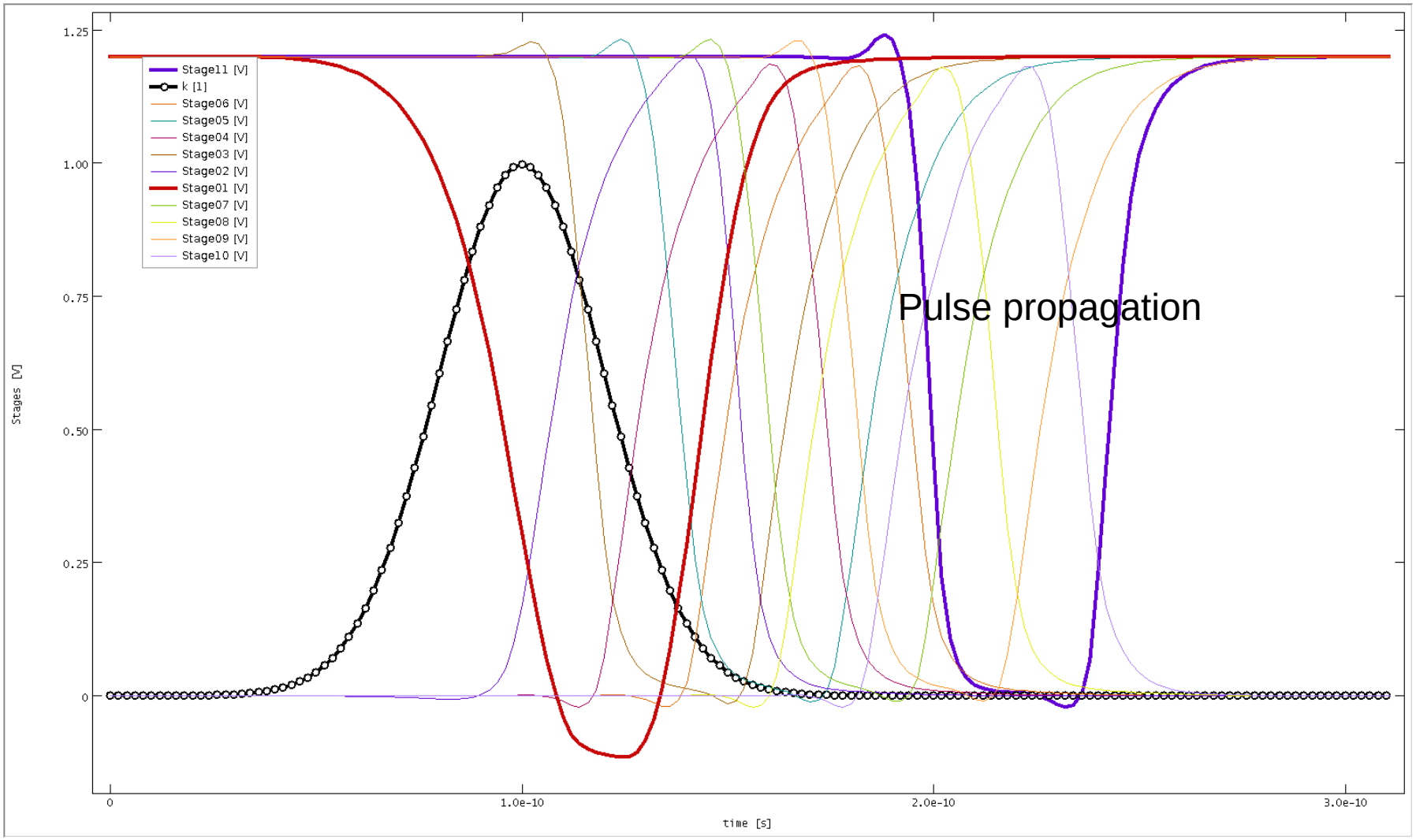
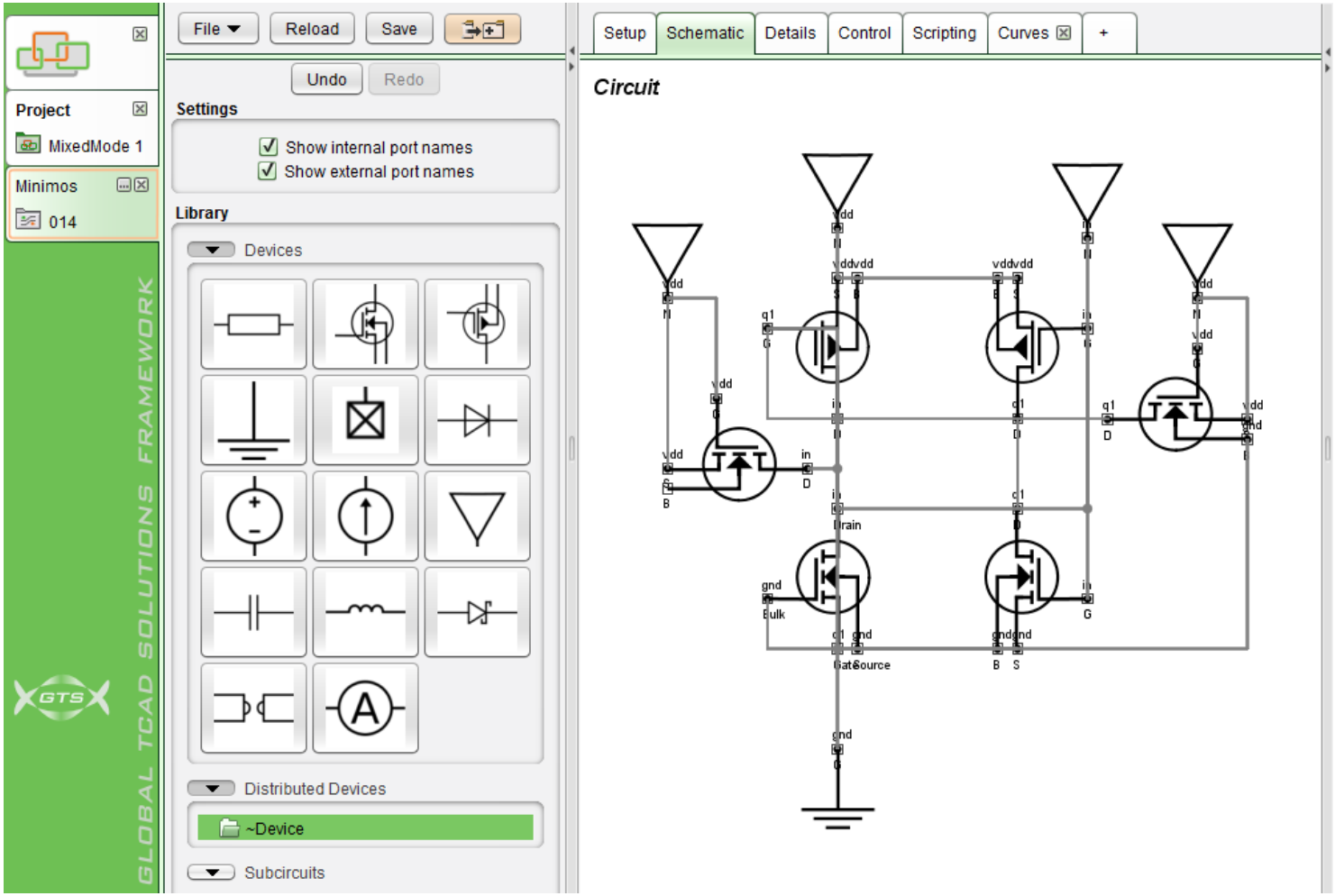
# Inverter - SET



# Inverter - SET

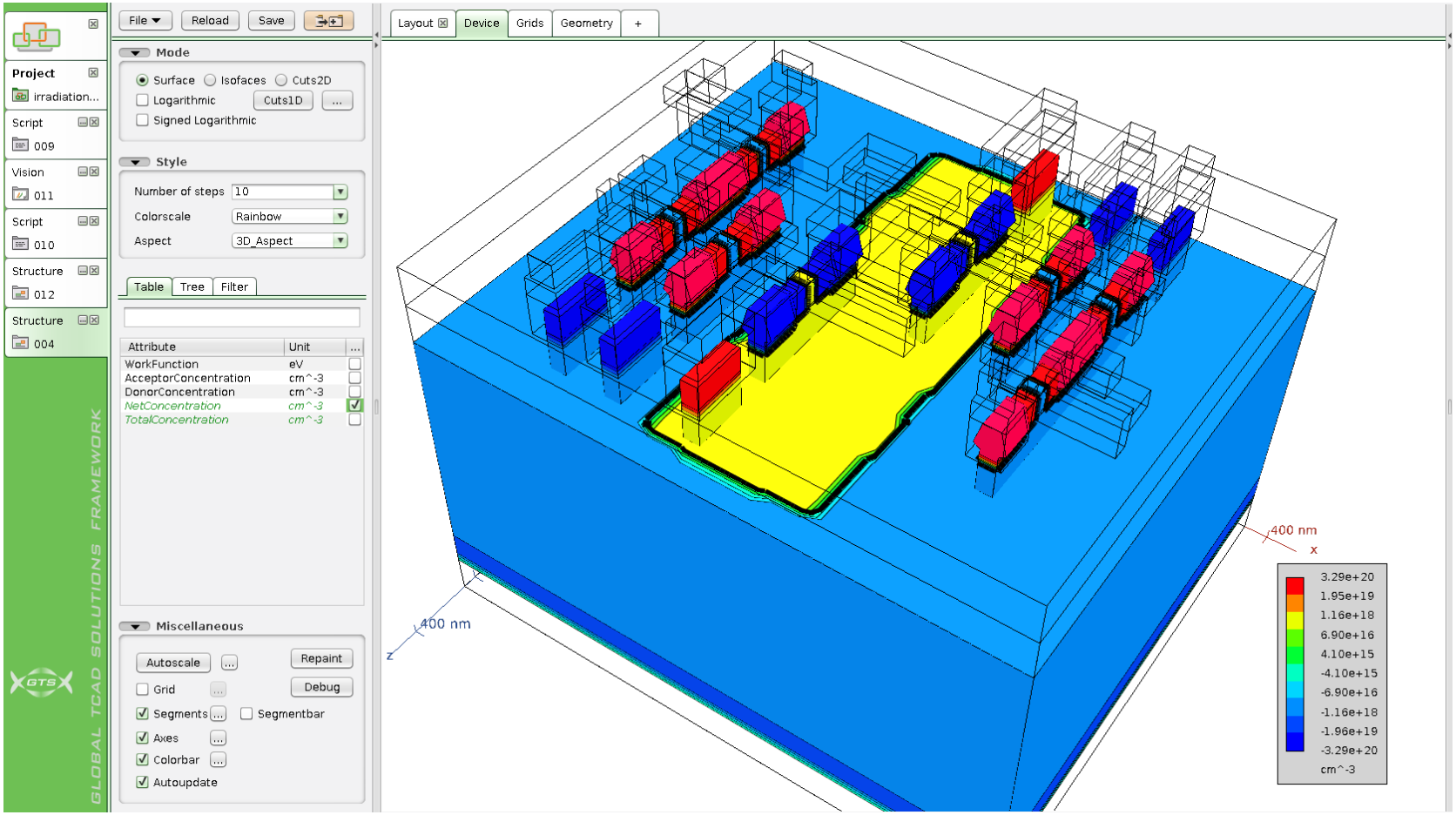


# 6T SRAM



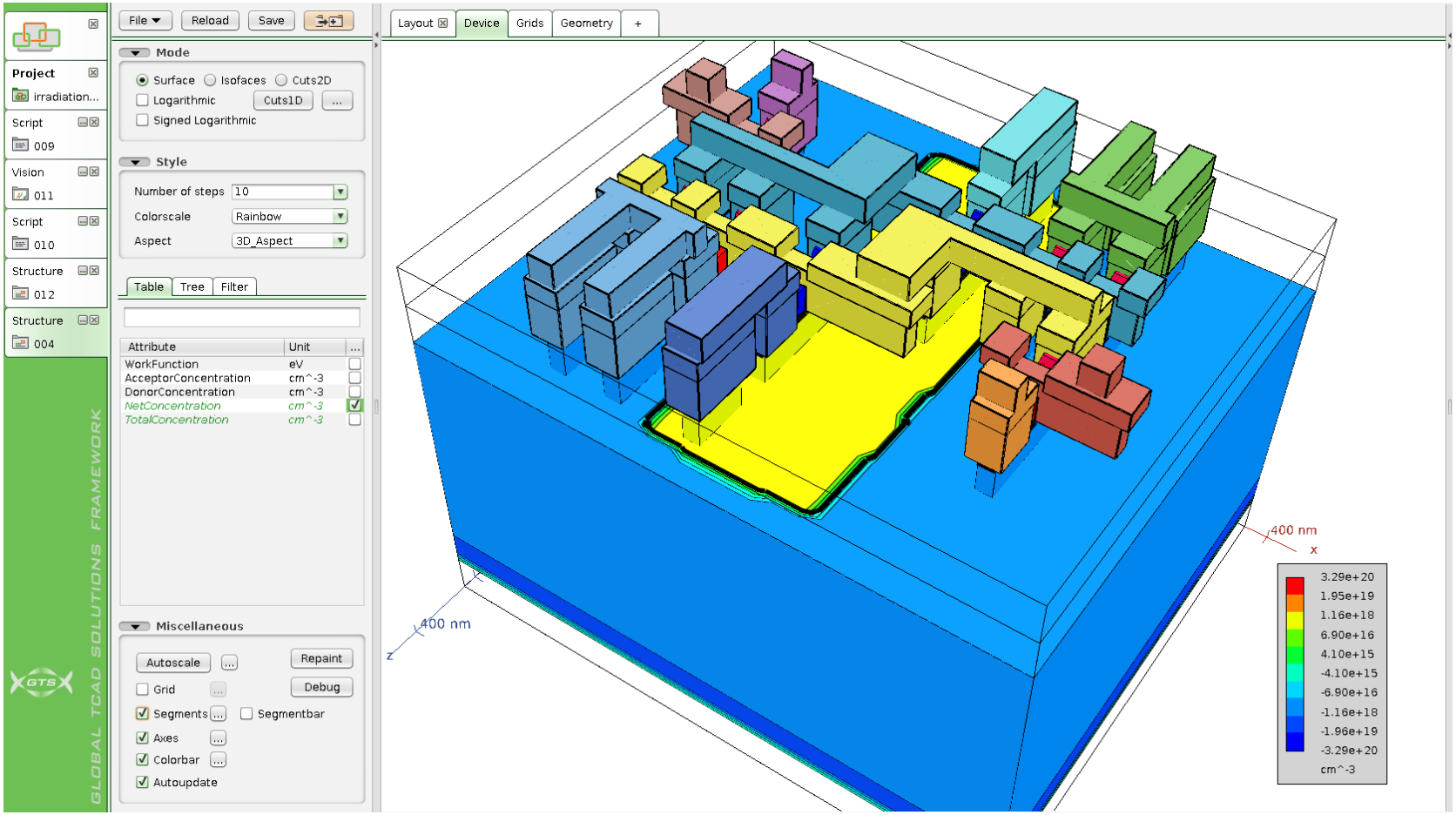

Compact circuit

# 6T SRAM



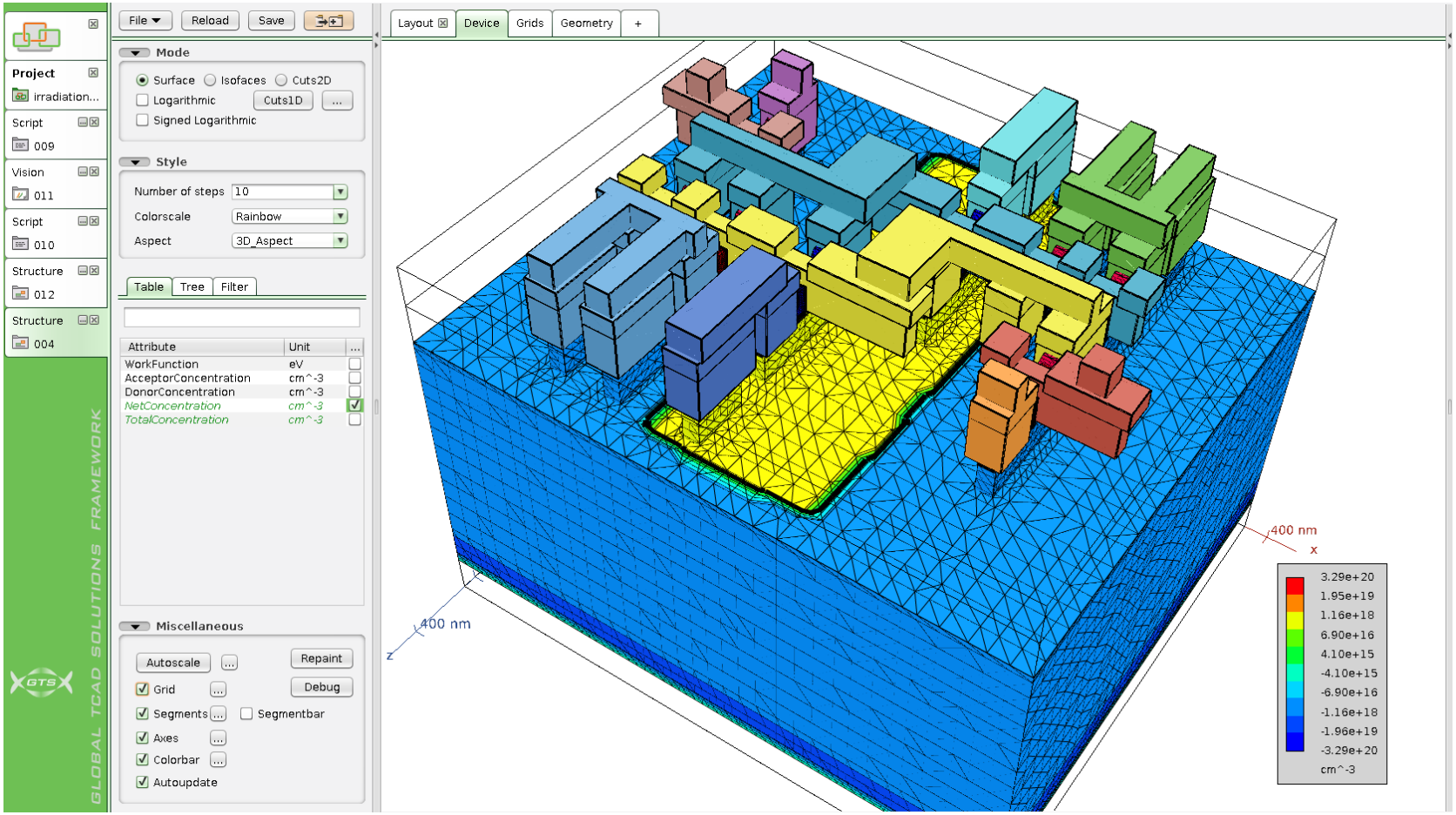

*Device structure with net doping concentration*

# 6T SRAM



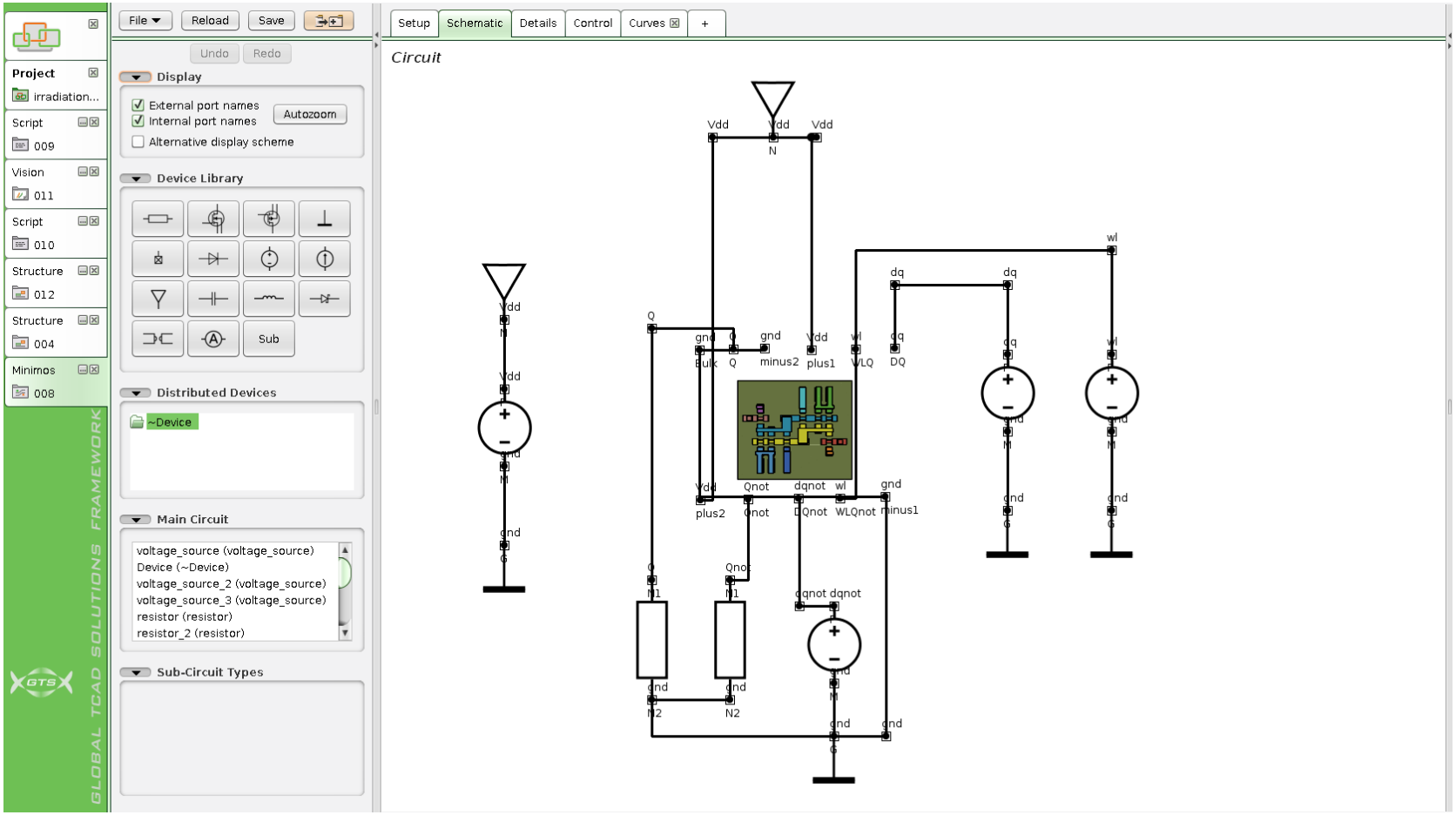

*Device structure with interconnects*

# 6T SRAM



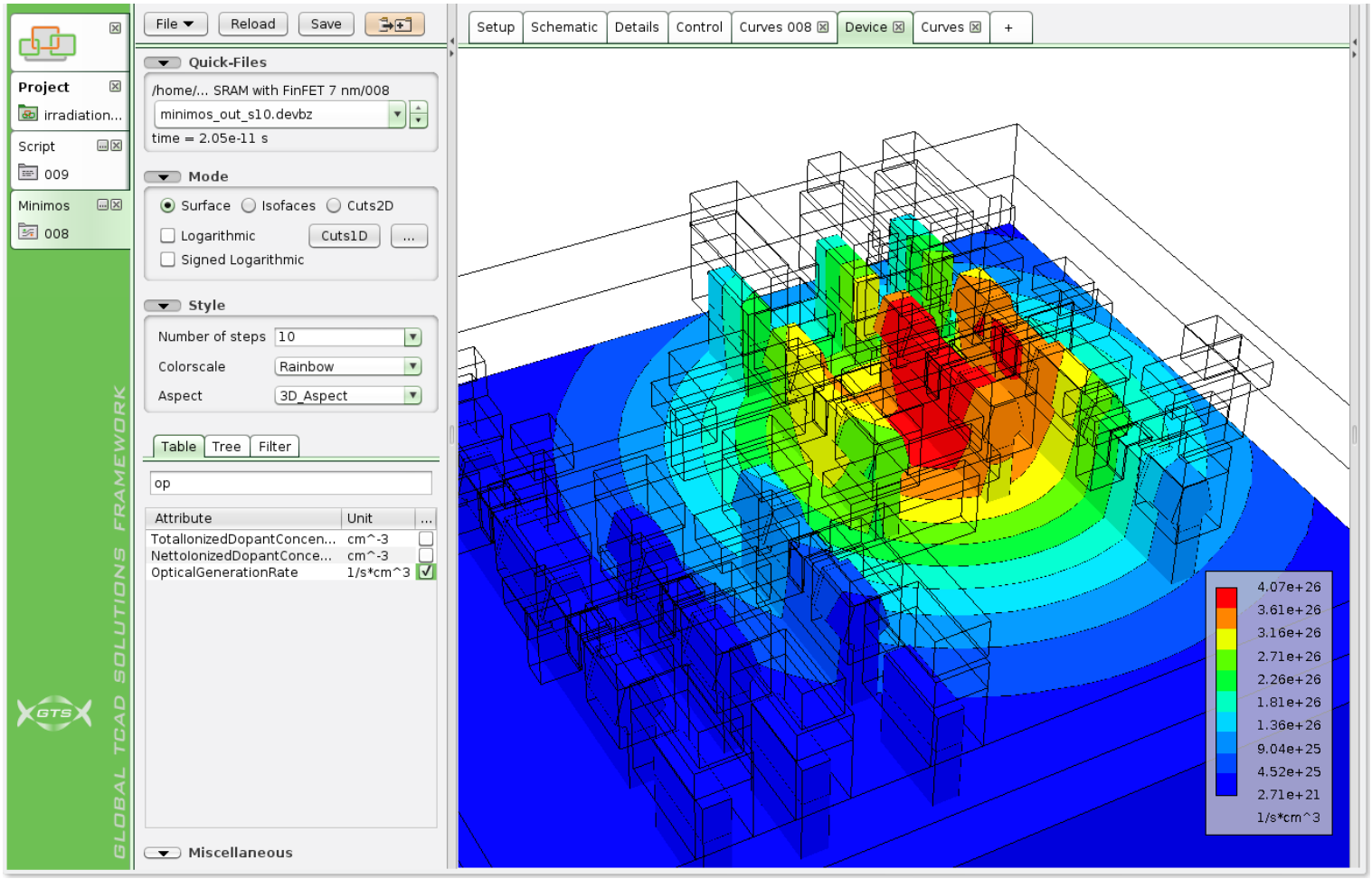

*Device structure with interconnects and grid*

# 6T SRAM



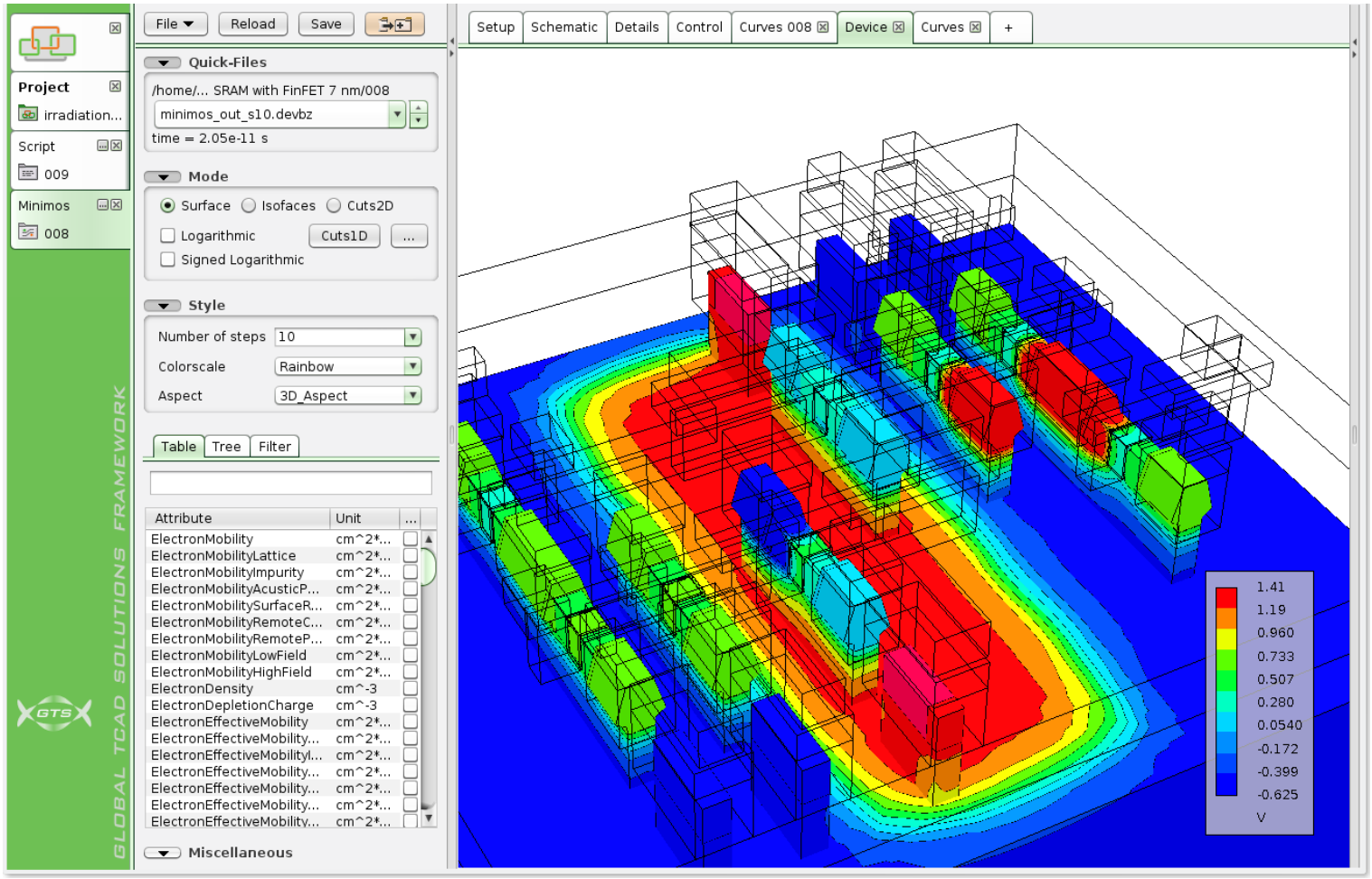

*Mixed-mode Circuit*

# 6T SRAM



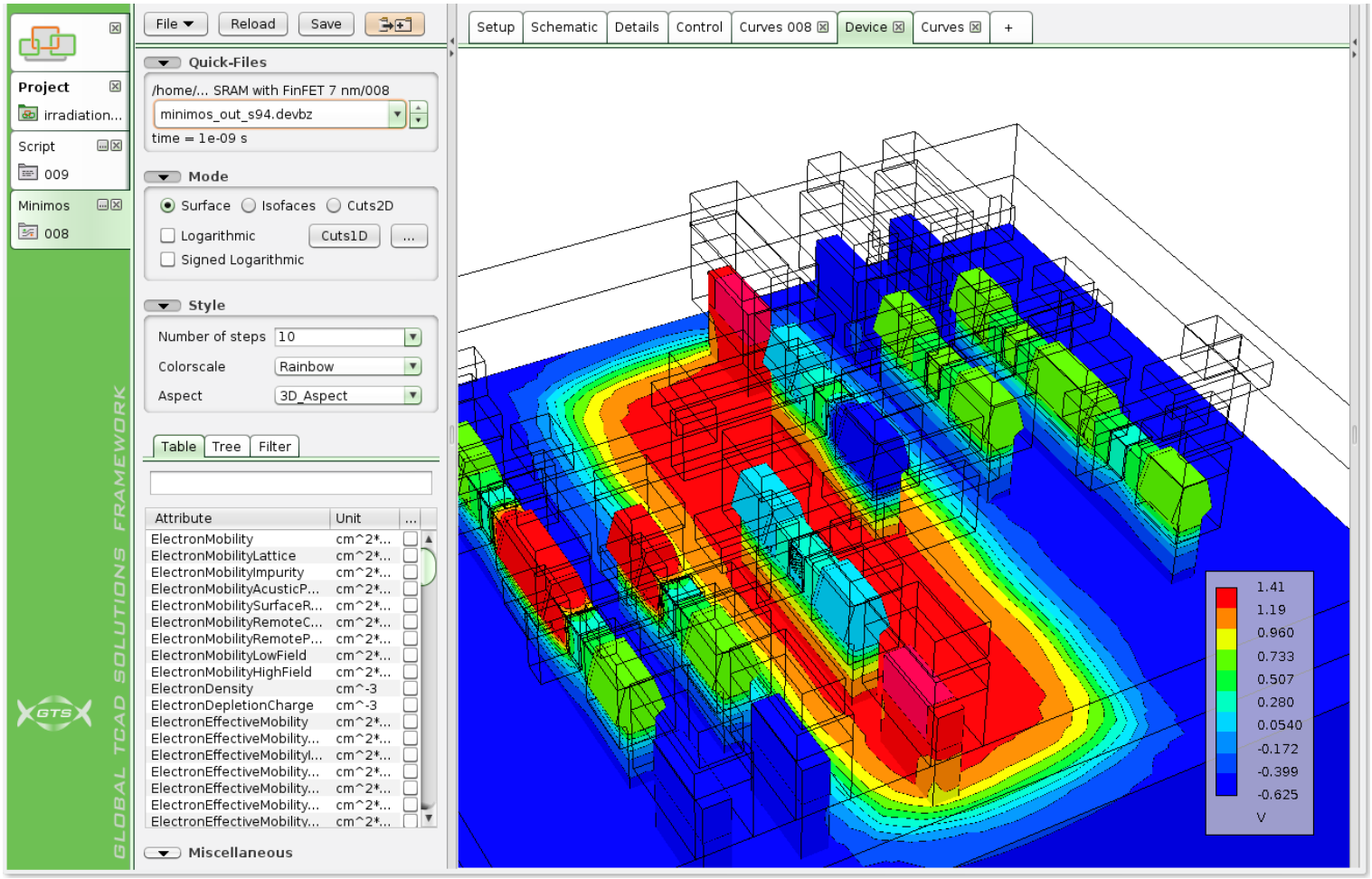

*Full 6T FinFET SRAM with rate generation profile*

# 6T SRAM



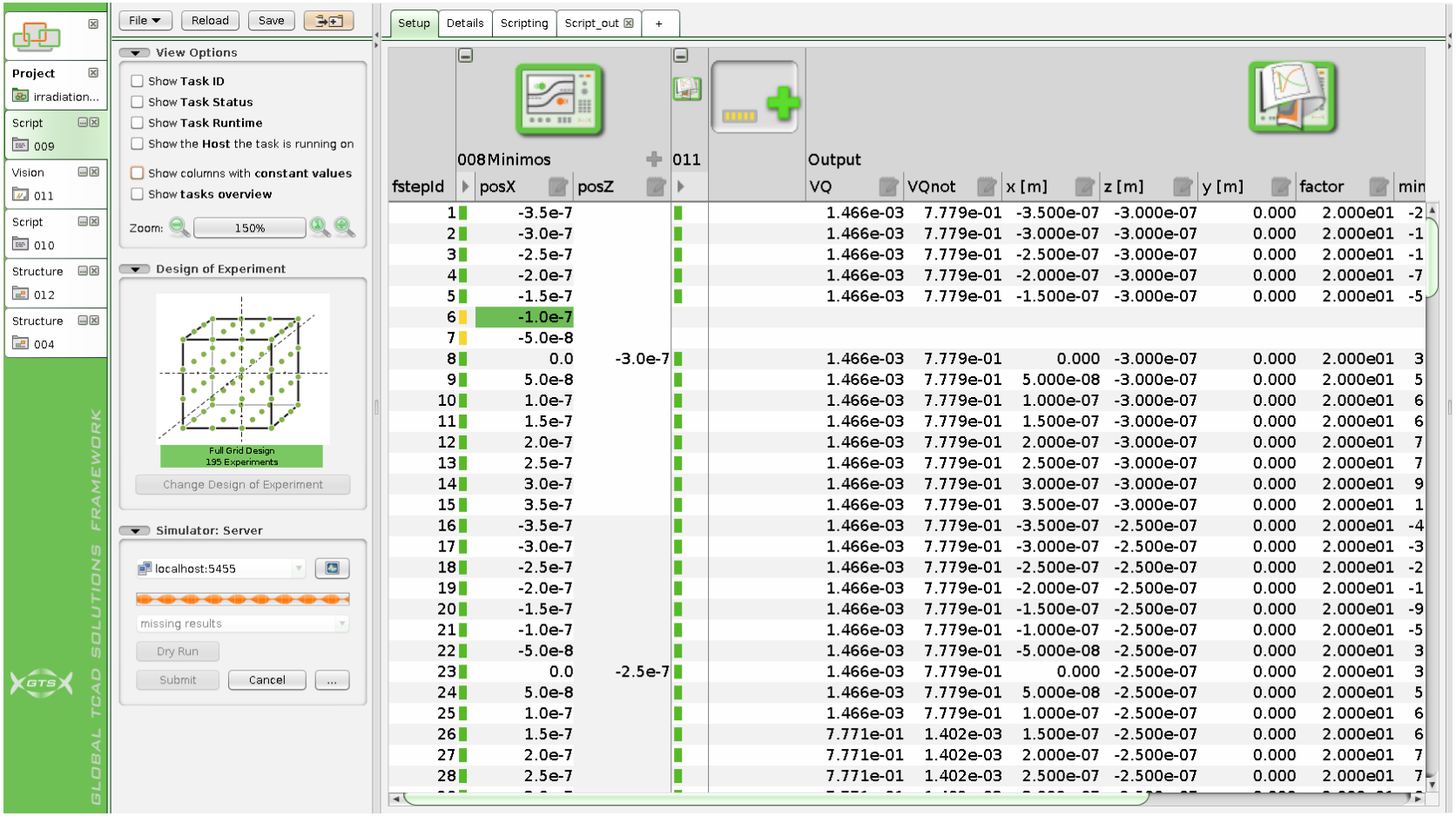

*Potential profile before impact*

# 6T SRAM



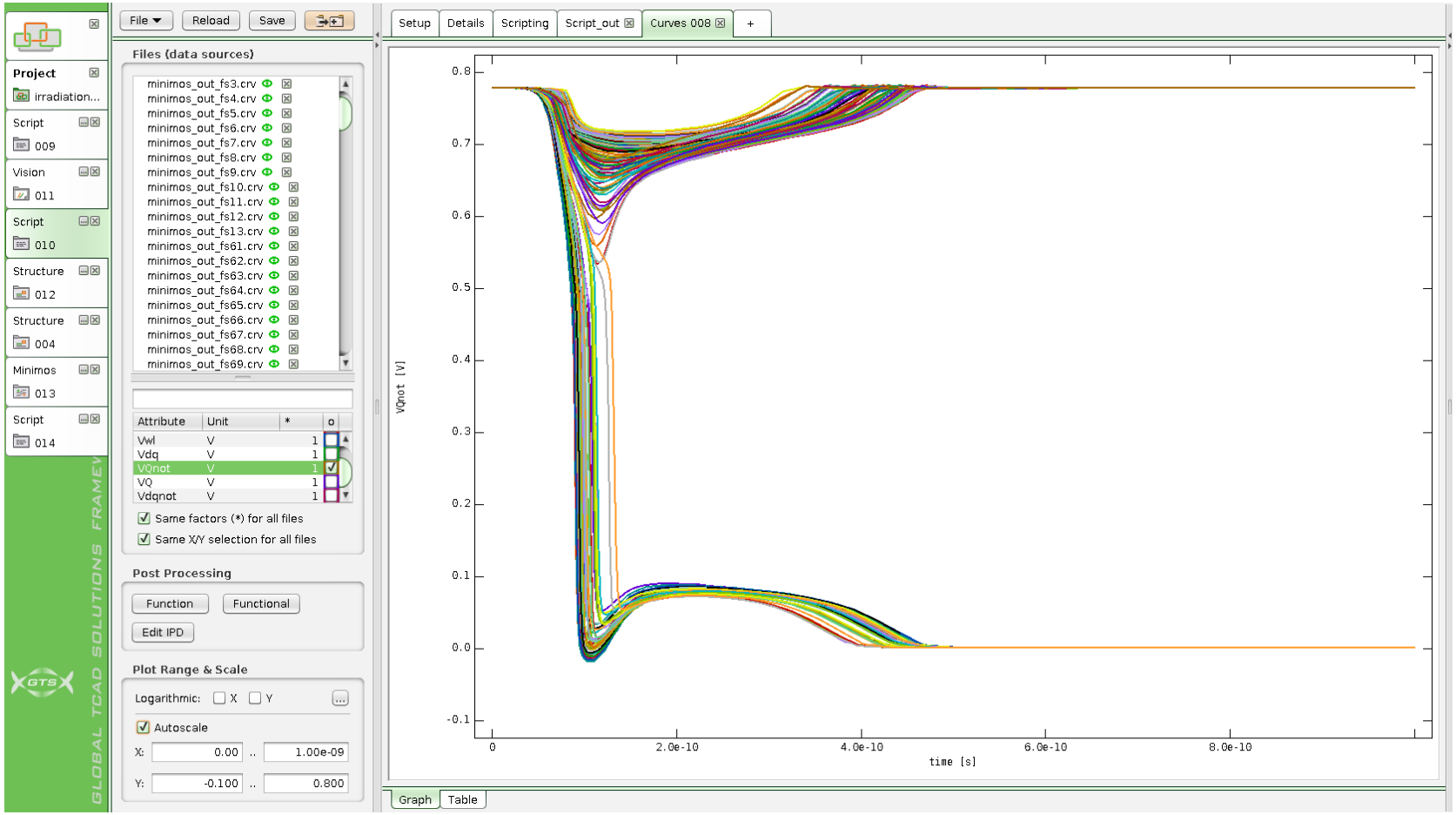

*Potential profile after impact*

# 6T SRAM



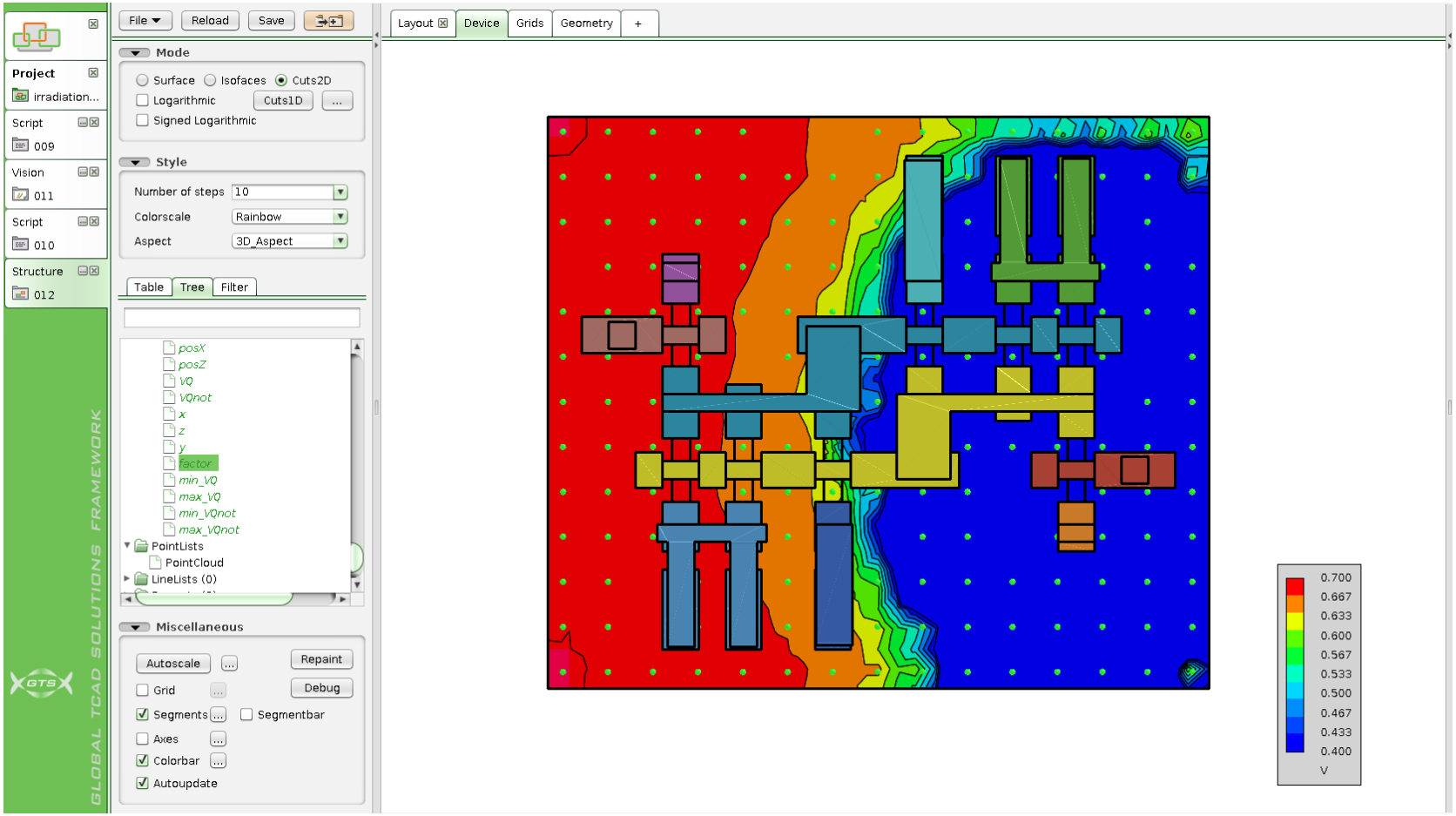

*Scripting engine / DoE*

# 6T SRAM




*Time evolution of Q/Qn outputs during impact at various sites*

# 6T SRAM




*Device top view with DOE ion impact points and min VQn*

# Summary & Outlook

## Layout-Based Structure Generation

- *Automated setup for different technologies (FinFET, NW)*
- *Meshing appropriate for technology and irradiation simulation*

## Physical Device Simulation for N7 and sub-N7

- *Subband-BTE (phase-space) solver for emergent devices*
- *Capture effects of quantization, ballisticity, scattering*

## Irradiation Simulation

- *Proof of concept implemented with GRAS*
- *Needs to be ported to Geant4 (ongoing)*
- *Analytical beam profiles for faster turn around*
- *Automated DoE allows for investigation of critical points*
- *Work in progress for flash devices (transnational project)*

# Acknowledgment

This work is supported by the Austrian-Chinese transnational project MORAFLASH No 850660