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## Highly versatile PicoSkyFT soft-core microcontroller for CAN based distributed system

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# Outline

- Background and competences
- Products portfolio
  - PicoSkyFT soft-core processor
  - PicoSkyFT Ecosystem
  - PicoSky family of development boards
- Application examples
  - nanoRACK concept
  - NANOimager-Miniaturized Multispectral SWIR Imager
  - NANOsky I - Nanoscale satellite platform

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# Background and competences

- Highly skilled mechatronics R&D engineering team
  - Embedded electronics and software development
  - Analog electronics, radio systems, and signal processing
  - IP Cores (digital and mixed signals)
- Engineering development approach
  - Miniaturization key aspect (following latest technology trends)
  - Hardware accelerated approach
  - Awareness of harsh space environment effect
- SkyLabs closely cooperates with University of Maribor – Laboratory for Electronic and Information Systems
  - Knowledge and technology transfer
  - Recruiting of highly skilled professionals
  - Core research capabilities (12 researchers)
  - TRISAT mission: First satellite developed with Slovenian know-how.

leis Laboratory for Electronic and Information Systems

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# SkyLabs products portfolio

**Nano and micro satellite platform**
Platform provider
for the emerging
space market.

**Fault tolerant IP cores**
PicoSkyFT™ radiation hardened
by design soft-core processor
and other peripheral units.

**Evaluation and development boards**
Providing an enhanced portfolio of
FPGA based development boards.

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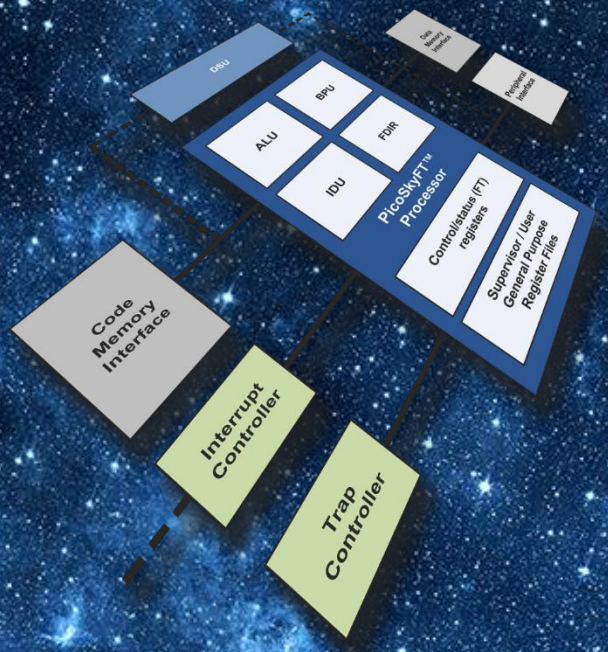
# PicoSkyFT soft-core processor

*Small footprint, radiation hardened by design processor core*




- Designed for embedded processing functions within SoC, but still preserving SoC flexibility.
- **Small footprint**, soft-core and **fault tolerant** processor core.
- **European Space Agency activity** (verification and radiation tolerance characterization)
- IP Core building block for true SoC architecture implementation and **technology independent**

Target applications

- Replacement for complex FPGA finite state machines with simpler piece of SW
- **PicoSkyFT SoC** fitted for **distributed intelligence**
- Smart sensors/actuators, RTU, payload TM/TC interface

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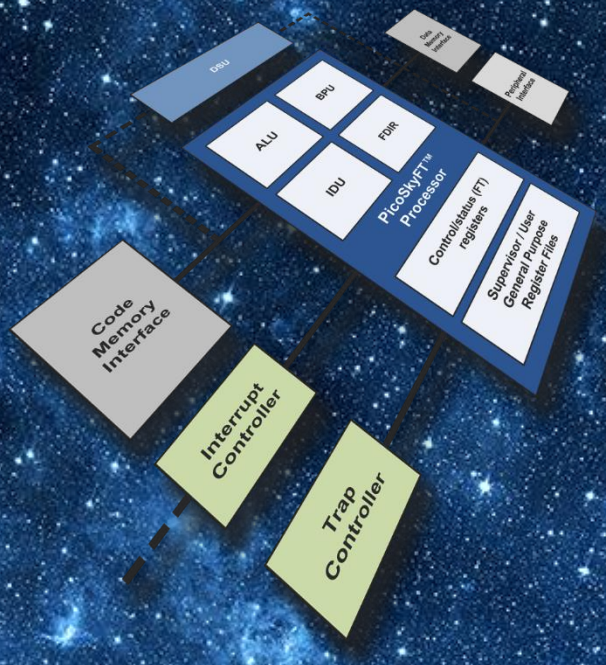
# **PicoSkyFT** soft-core processor

*Small footprint, radiation hardened by design processor core*




## Architecture

- **RISC** 8/16-bit Harvard architecture
  - Proprietary **PicoSky ISA**
  - Operation in two modes (supervisor – privilege mode / user operation mode)
- **Single pipeline** architecture
  - Highly deterministic operation
  - Hard real time interrupt response capabilities
- **140 instructions** (**97.5%** of 16-bit combinations used) provides extremely **high code density**
  - Low memory footprint of the application code
  - High integration capabilities (minimal number of external components)

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# **PicoSkyFT** soft-core processor

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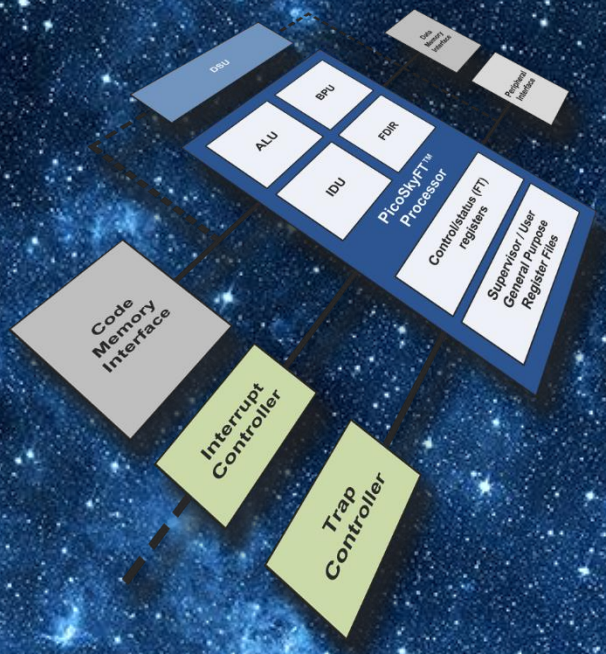


- Configurable **program memory** models **up to 8 MB**
- Configurable **data memory** models **up to 16 MB**
- **32** general purpose **user registers** (dual party protected)
- **Booting via SPI NVM memory** (EDAC protected) with multiple FW images support
- Hardware accelerated **multiplication instructions**
- Configurable Interrupt Controller
  - Customizable number of interrupt vectors
  - Prioritized interrupt vectors
- Non-intrusive **Debug Support Unit** over high-speed PicoSky-Link programmer.
- **Remote debugging and programming** capability over a CAN bus and SPI.

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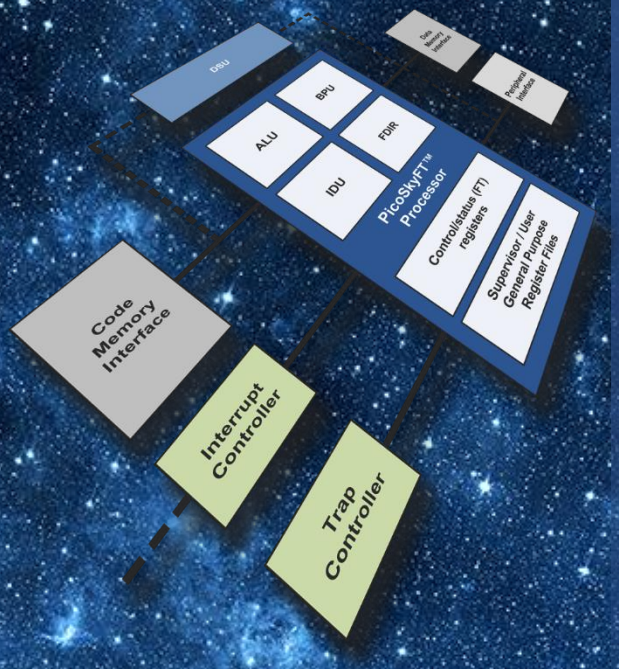
# PicoSkyFT soft-core processor

*Small footprint, radiation hardened by design processor core*




- **Processor benchmark**
  - **Mostly single cycle instructions reaching** 1 MIPS/MHz
  - CoreMark score: 0.57 CoreMark/MHz (*optimization level –O2*)
- **Radiation hardened by design approach**
  - Spatial triplication (TMR) on register level (optional temporal redundancy) using SEES™ Tool
  - EDAC protected all memory blocks, by Hamming scheme (8,4)
  - Multiple SEC-DED per word
  - Upon SEC detection and correction, the operation can be returned to user mode without a reset.
  - EDAC unit diagnostics functionality
  - Separate 16-bit supervisor-PROM interface w/ or w/o EDAC
  - Trap handlers invoked in single cycle upon detected faults
  - User defined FDIR policy for mitigation techniques for each trap respectively

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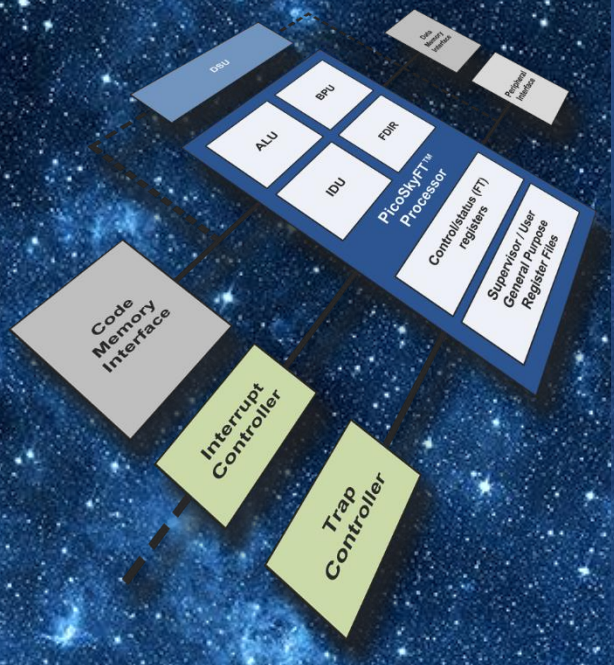
# PicoSkyFT soft-core processor

*Small footprint, radiation hardened by design processor core*




**Traps handlers**

1. **Reset** trap is a global hard-reset, e.g. at power-on or watchdog reset, etc...
2. **Register file** trap occurs at parity error during user register read operation in register file
3. **Program exception** trap occurs in case of invalid or privilege instruction fetch, or when program counter jumps to a protected program memory region.
4. **Program memory** trap occurs uncorrectable / correctable error on program memory or unacknowledged access.
5. **Data memory** trap occurs in case of uncorrectable / correctable error on data memory or unacknowledged access.
6. **Software** trap can be issued by application software, upon detecting erroneous condition within application itself (e.g. peripherial unit is not reponsding), or when a switch to supervisor (privileged mode) operation is required (e.g. FW upgrade).

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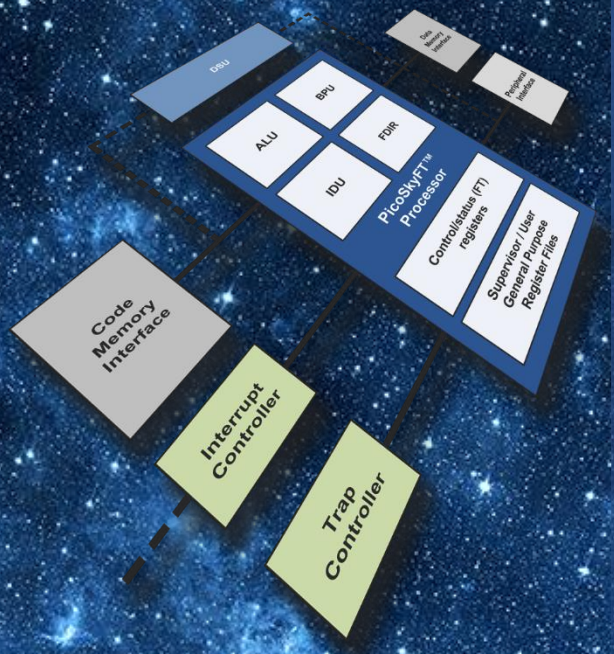
# **PicoSkyFT** soft-core processor

*Small footprint, radiation hardened by design processor core*




Key advantages of using PicoSkyFT processor

- **PicoSkyFT** makes development **less complex**, thus shortening the development time and verification cycles and ultimately providing **faster time to market**.
- Targeting applications requiring **scaled performance**, reduced peripherals functionality, **hard real-time performance**, and **high reliability requirements**.
- Using PicoSkyFT in application would benefit in terms of **ease of use**, **application performance**, static power consumption and overall production costs.
- PicoSkyFT enables highly customized designs thanks to its availability as IP Core.

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# **PicoSkyFT** Ecosystem

*Development environment*

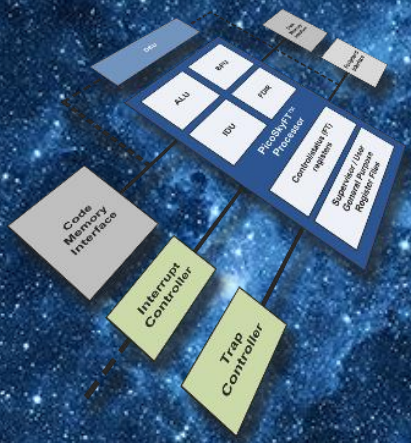
***PicoSkySIM-Interface***
*Extenstion board*

***PicoSkyWARE***
*PicoSkyWARE is a collection of software development tools to provide the effective development of PicoSkyFT code solutions. PicoSkyWARE is a standalone package compliant with Windows and Linux operating systems.*

***PicoSkyTEST***
*PicoSkyTEST is an enhanced test suite platform enabling highly efficient verification of SoC RTL design at each step of the development. The test suite thoroughly examines processor functionality with regrestion testing at RTL simulation level, RTL implementation on FPGA or even in PicoSkySIM.*

***PicoSkySIM***
*PicoSkySIM is a cycle exact software based PicoSkyFT processor simulator. PicoSkySIM fastens the development cycle and in addition increases the system's testability as tests can be performed already at the early design stages.*

***PicoSkyFT processor***




***ecosystem***

***PicoSkyLINK –*** *programmer and debbuger*

***PicoSkySIM-Interface***
*PicoSkySIM Interface board is an extension of the PicoSkySIM providing a bridge between the simulated environment and the real world. Simulated and custom developed peripheral units can be easily interfaced to real physical interfaces.*

***PicoSkyLINK***
*The **PicoSkyLINK** is an **debugger and programmer** for the PicoSkyFT processor. The high speed synchronous debugging interface enabling astonishingly fast programming times and incredibly responsible debugging.*

***SEES™***
*SEES ™ (**Single event effect simulation**) is a comprehensive tool for SEE simulation on the FPGA gate-level (SET, SEU). Technology independent simulator, enables low cost design analysis against soft-errors.*

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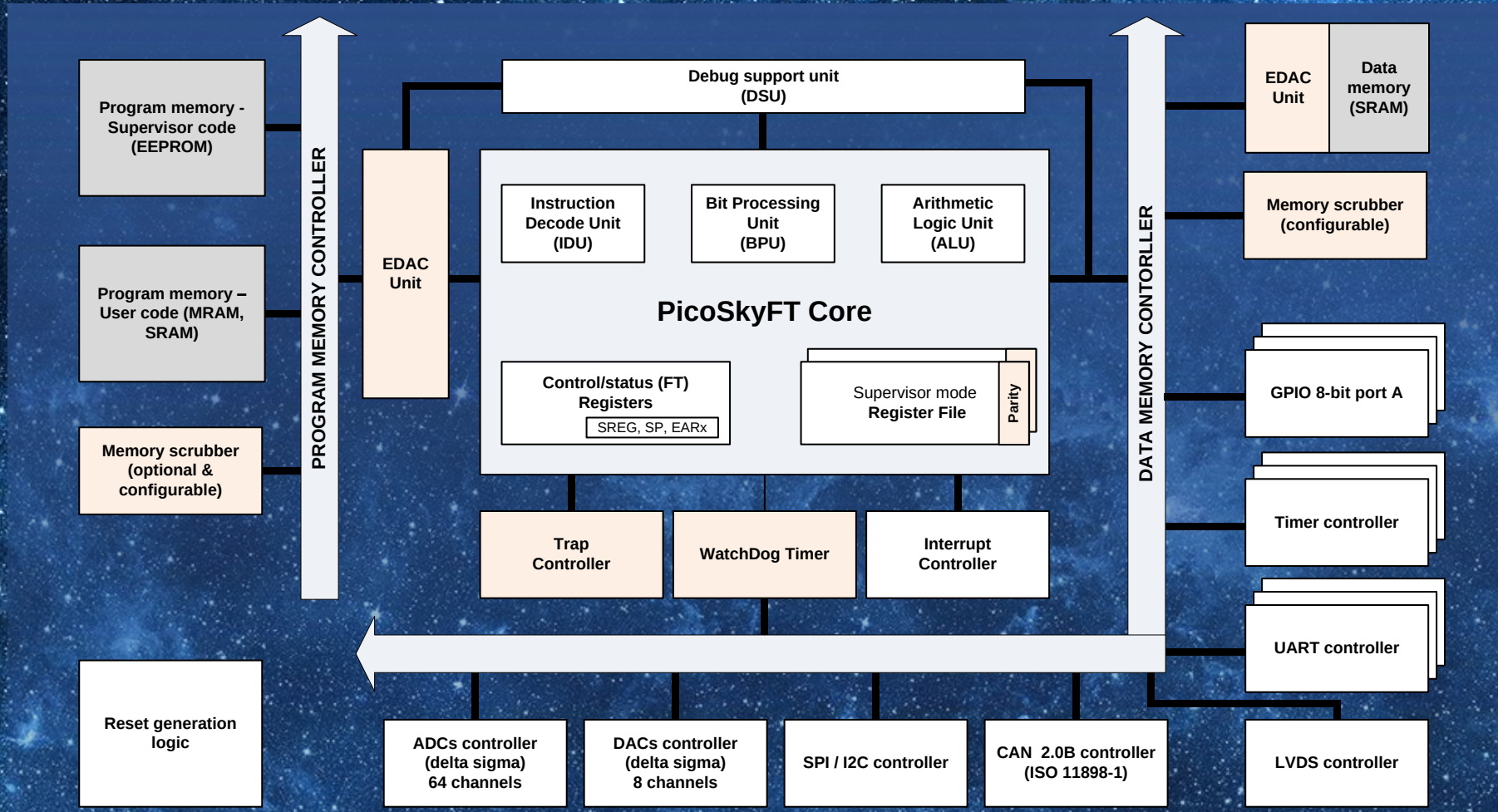
# **PicoSkyFT** SoC example

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*SkyLabs standard **PicoSkyFT SoC implementation***
*(all cores avalible)*

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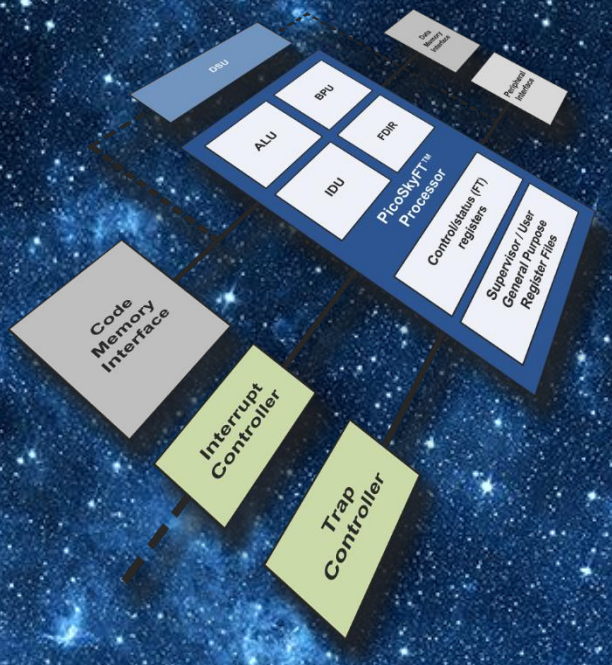
# **PicoSkyFT** soft-core processor

*Software development support*




**Platform support**

- **FreeRTOS** real-time operating system
- ***C Standard library***
- *PicoSkyFT **Drivers library** (SPI, TWI, CAN, UART, GPIO, Timers, LVDS, DACs, ADCs...)*
- *Comprehensive **code examples** for quick hands on experiences*

**Communication stacks**

- ***CANopen stack implementation** (according to ECSS-E-ST-50-15C)*
- ***CAN-TinyStack** simple reliable CAN stack*
- ***Light weight TCP/IP** Stack*

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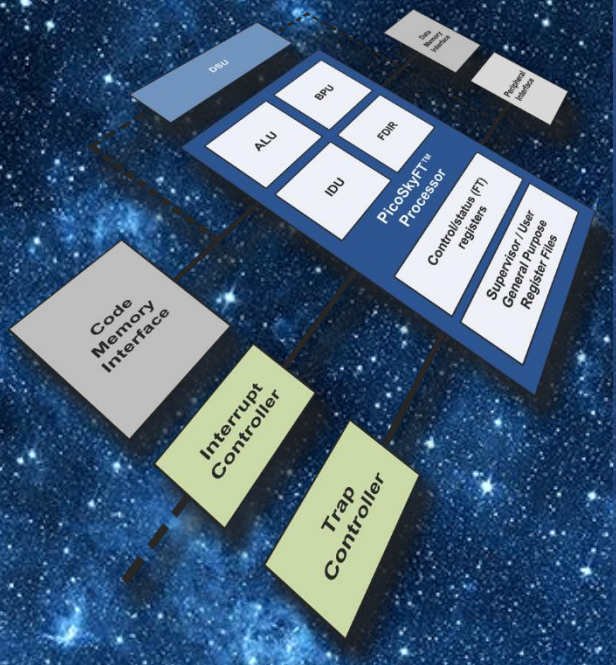
# PicoSkyFT soft-core processor

*Single Event Effects testing*




**SEE Testing** (soft-errors)

- Finished SEU simulation testing of PicoSkyFT SoC with SEES™
  - Simulating SBU and MBU on all memories
  - Simulating SEU on the TMR registers on PicoSkyFT SoC gate level simulation (post layout simulation)
  - Test has been passed successfully and confirming protection mechanisms to work as expected.
- Follows SEU + SET simulation testing of PicoSkyFT SoC with SEES™
  - The objective is to test PicoSkyFT SoC with TMR and temporal redundancy.
- Q3/2017 Radiation testing at PSI Proton Irradiation Facility (PIF) to establish the upset characteristics and determine the upset cross-section of PicoSkyFT

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# PicoSkyFT Ecosystem

## Comprehensive set of development boards

## PicoSky™ Development Board ProASIC3 SKY-9211

SpW dual | CAN dual | RS422 | RS232

- Microsemi ProASIC3e A3PE3000 FPGA
- On-board memories
  - MRAM 4 MB (1M x 32-bit, unlimited read/write endurance)
  - SRAM 4 MB (1M x 32-bit) and SRAM 2 MB (1M x 16-bit)
  - PSRAM 8 MB (4M x 16 bit)
- Interfaces available
  - 2 x SpaceWire interfaces
  - 2 x MIL-STD-1553B interface
  - 2 x CAN bus interfaces
  - 2 x RS232 interfaces (with RTC, CTS handshaking)
  - 4 x RS422 transmit and receive pairs
  - 4 x DAC and ADC channels, SPI/TWI interface, GPIO expansion headers
  - Ethernet PHY 10/100 Mbps interface
  - 2 x USB 2.0 Host interfaces and 2 x UART over USB
- Clocks
  - 2 x On-board oscillators with SMA extension connectors
  - Dedicated 100 MHz oscillator for SpaceWire interface
  - On-board RTC with calendar and backup battery
- User DIP switches, tactile switches and LED indicators
- Small board size 170mm x 145mm

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# PicoSkyFT Ecosystem

## Comprehensive set of development boards

## PicoSky™ Development Board IGLOO2/SmartFusion2 SKY-9212

SpW | CAN dual | SerDes dual high speed | LVDS high speed | eMMC | RS232

- Microsemi IGLOO2 M2GL050 M2S050 FPGA
- On-board memories:
  - - MRAM 4 MB (1M x 32-bit, unlimited read/write endurance)
  - - SRAM 2 MB (1M x 16-bit)
  - - High speed dual eMMC 32 GB
- Interfaces available
  - 2 x LVDS (SpaceWire compatible)
  - 2 x SerDes SATA interface
  - 2 x CAN bus interfaces
  - 1 x RS232 interface (with RTC, CTS handshaking)
  - 1 x MIL-STD-1553B expansion slot
  - 1 x SPI interface, GPIO expansion headers
  - 1 x UART/SPI over USB (interface provided over USB converter)
- Clocks
  - 2 x On-board oscillators
  - Dedicated 100 MHz oscillator for SpaceWire interface
  - On-board RTC with calendar and backup battery
- User DIP switches, tactile switches and LED indicators
- Small board size 140mm x 120mm

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NEW

# PicoSkyFT Ecosystem

## Comprehensive set of development boards

## PicoSky™ Evaluation Board SKY-9213

PicoSkyFT SoC on-board | PicoSkyLINK on-board | rich housekeeping telemetry | 104-pin CubeSat Kit Bus OBC | CAN dual | eMMC

- Pre-programmed PicoSkyFT processor with RTOS demo example
- Microsemi IGLOO2 M2GL050 FPGA
- On-board memories
  - MRAM 1 MB (256K x 32-bit, unlimited read/write endurance)
  - High speed mass storage (eMMC 32 Gb)
- Interfaces
  - CubeSat Kit compliant connector
    - 2 x CAN bus interfaces
    - UART interfaces
    - I2C/SPI interface
    - General purpose I/Os
  - JTAG interface for FPGA programming
  - High speed UART over USB interface
  - Integrated *PicoSkyLINK*
- Clocks
  - Dedicated 20 MHz clock source
- Board powered by USB (or via CubeSat Kit connector)
- Comprehensive local housekeeping data
  - On-board FPGA temperature sensor
  - Voltage monitors for each power supply rail
  - Board overall current monitor
- User tactile buttons and LED indicators (for easier development)
- PC/104-size form factor (96mm x 90mm)

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NEW

# PicoSkyFT Ecosystem

## Comprehensive set of development boards

## PicoSky™ cpciSDR 1x1 SKY-9202


Software Defined Radio | RF Agile Transceiver™ | Ouput power 20 dBm | CompactPCI® | CAN dual | SpW dual

- 3U CompactPCI® Software Defined Radio Card
  - Supports 32bit peripheral mode, 33/66MHz CompactPCI® bus
- Software defined radio characteristics
  - Xilinx Artix®-7 FPGA for RF closed loop control, modem management and signal processing
  - RF 1 × 1 transceiver with integrated 12-bit DACs and ADCs
  - Configurable frequency band for transmit and receive channels from 70MHz to 6GHz
  - Supports TDD and FDD operation
  - Tuneable channel bandwidth (BW): <200 kHz to 56 MHz
  - Superior receiver sensitivity with a noise figure of <2.5 dB with prior receiver matching
- Microsemi ProASIC3E A3PE3000 and IGLOO2 M2GL050 & Xilinx Artix®-7 FPGAs
- Rich set of on-board memories (MRAM, EEPROM, SRAM, eMMC)
- Interfaces
  - SDR: Dual SMA receivers' inputs, dual SMA transmitters' outputs and single SMA for Tx power monitor
  - Redundant SpaceWire and CAN bus ports
  - Serial UART, SPI and JTAG interface over USB
  - External PPS and RefCLK clock sources via MMCX connectors
  - Up to 126 single-ended I/Os, two Rx/Tx differential, two Rx/Tx and clock for SERDES
  - Dedicated 3A power supply for mezzanine connectors

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# **PicoSkyFT** Application examples

**nanoRACK** concept

- Remote Terminal Unit in 2.5” card slots

**NANOimager**

- Miniaturized Multispectral SWIR Imager

**NANOsky** I

- Nanoscale satellite platform

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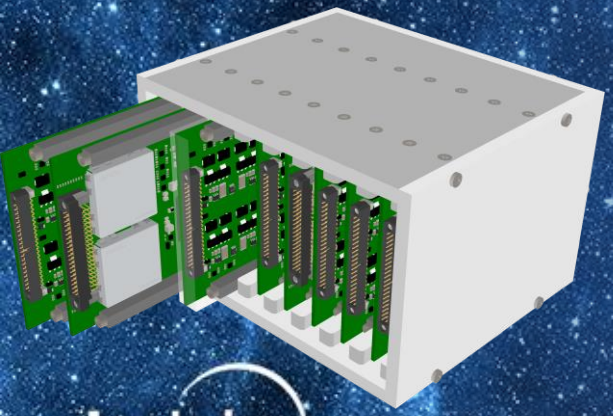
*„We innovate space for Space“*

# **nanoRACK** concept

## *Remote Terminal Unit in 2.5” card slots*

**nanoRACK** concept



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*The **nanoRACK** concept utilizes a compact **NANOrtu** cards and presenting the **concept of distributed intelligence** for aerospace applications.*

*The **nanoRACK** concept **introduces highly scalable and modular** approach for satellite systems. Interoperability with any other equipment is assured, as a **standardized CAN communication** protocol is supported.*

*The main objective is to preserve a high number of user interfaces and their flexibility at significantly reduced volume and mass, whilst providing rugged design, comprehensive local telemetry acquisition, and power requirements.*

***nanoRACK** technical characteristics*

- *Fully modular architecture, due to autonomous **NANOrtu***
- *ruggedized R-SATA connectors for **nanoRTU** cards,*
- *backbone communication based on redundant CAN busses,*
- *data rates up to 5 Mbit/s (CAN FD) and fully ISO 11898-2:2003 complian,*
- *application layer communication based on **CANbus extension protocol** (ECSS-E-ST-50-15C) or propretery **CAN-TS stack**.*

*„We innovate space for Space“*

# **nanoRACK** concept

## *NANOrtu-PowerIO card*

**NANOrtu-PowerIO card**

***NANOrtu-PowerIO*** *is a power input/output card, providing a power or general purpose digital input/output.*

*Primary application examples for* ***NANOrtu-PowerIO***

- *gathering digital telemetry from sensors and units (Releay Status Acqusiction, Digital Status, etc.)*
- *controling AOCS actuators (as Reaction Wheels, Stepper motos, Magnetotorquers, etc.)*
- *controling the Propulsion S/s and Solar Array Drive Equipment*
- *To distribute power to heaters and active loads.*

***Power Digital IO tehnical characteristics***

- *Number of Channels:* *4 fully configurable IOs with source/sink capability and monitoring*
- *Voltage Range:* *12 – 32 VDC*
- *Operational Monitoring:* *source current measurement, sink current measurement, input/output state*
- *Operational Modes:* *half/full bridge operation, general on/off, PWM control*
- *Operational Features:* *adjustable death times, separate high/low side PWM, high side Sigma Delta*

***General Purpose Digital IO tehnical characteristics***

- *Number of Channels:* *8*
- *Input/output Type:* *LVCMOS/LVTTL*
- *Voltage Range:* *0 – 3.3 VDC*

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# **nanoRACK** concept

## *NANOrtu-DS-AI card*

**NANOrtu-DS-AI card**

***NANOrtu-DS-AI** is a delta-sigma analog acquisition card. Providing a high number of analog inputs,*

*Primary application examples for **NANOrtu-DS-AI***

- *gathering the analogue telemetry from sensors and units (Temperature, Pressure, etc.)*
- *to provide the conditioning for analogue sensors*
- *to monitor AOCS sensors (as Sun Sensors, Magnetometers, etc.)*

***Analog Inputs***

- *Number of Channels:* *up to 64*
  *default configuration:* *32 biased channels for resistive sensing*
- *32 non-biased channels for voltage sensing*

- *Type of ADC:* *Delta-Sigma*
- *Input Voltage Range:* *0 – 3.3 V*
- *Input Resistance:* *100 kOhm*
- *Analog Input Filter BW:* *160 kHz*
- *Resolution and Sample Rate:*
  *default configuration:* *16-bit, 300 sps @ 150 Hz effective bandwidth (adjustable to specific requirements)*

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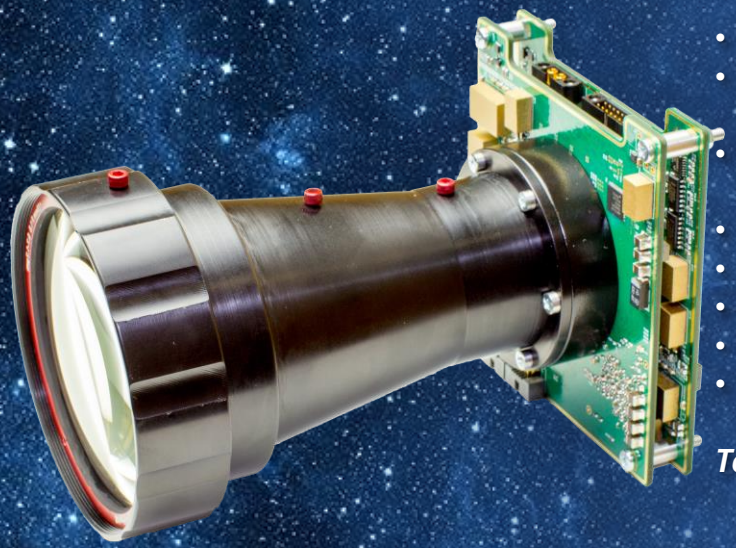
# Satellite payload **NANOimager**

## ***NANOimager*** *- Miniaturized Multispectral SWIR Imager*



**NANOimager (EQM)**
Launch Q2/2018

- *NANOImager with 20 spectral channels covering VNIR/SWIR*
- *Targeted for forest monitoring and agriculture tracking from space, and transport infrastructure progress tracking in air born applications*
- *Radiation hardened by design to increase reliability and robustness of the payload computer*
- *Hot redundant mass storage eMMC with capacity up to 64 GB*
- *Comprehensive local subsystem telemetry (currents, voltages, temperatures)*
- *LVDS interface link for high speed data transfer*
- *Hot redundant CAN interface for TM/TC*
- *Powered by PicoSkyFT™ processor*

***Tehnical characteristic:***

- *InGaAs highly sensitive SWIR sensor*
- *Spectral bands: 20 nonoverlaping bands*
- *Spectral bands resolution:18 nm – 42 nm*
- *Spectral range: 900 nm – 1700 nm*
- *GSD: 100 m @ 500 km NIR/SWIR*
- *SNR: > 100 on each channel*
- *F#: 4*
- *Focal length: 100 mm*
- *Power consumption: < 3 W*
- *Dimensions: 95 x 91 x 148 mm*
- *Mass: < 820 g*

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# Satellite platform **NANOsky I**

*Complete solution out of the box*

**The right solution for the emerging space market**

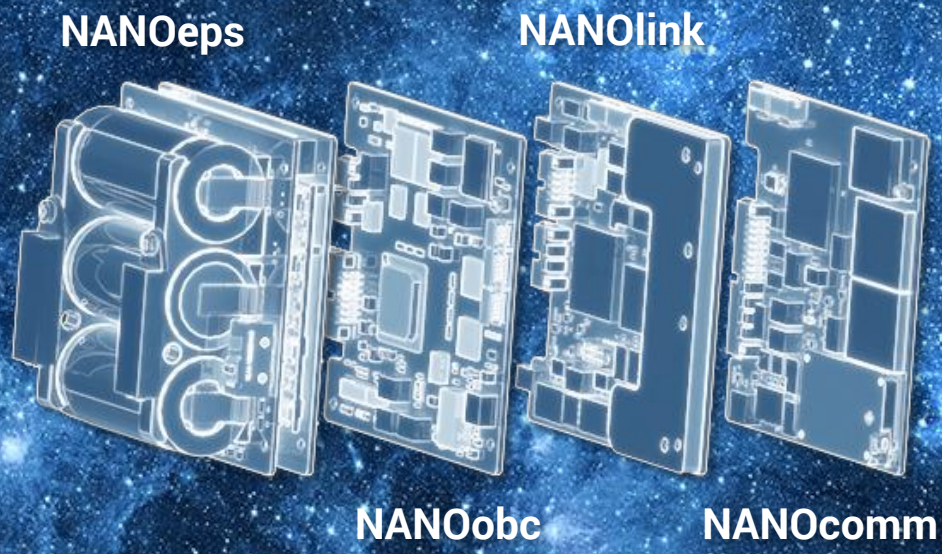
**Fault tolerant system design**

**New type of harness**

**Pushing the limits of system miniaturization**

**Designed for high reliability and availability**

**Tailor made to clients needs**




***Level of qualificaions:***

- *Full electrical and functional test*
- *Thermal and vacum testing*
- *Vibration test*
- *TID planned Q1/2017*
- *SEE planned Q3/2017*

***NANOsky I** is a highly miniaturized nanoscale platform with fault tolerant features as would be expected in high end systems. SEE tolerant, innovative error mitigation techniques, sophisticated three-level FDIR policy, redundancy on all critical functions and thoughtful component selection ensure robustness, high reliability and the availability of the platform. Small in scale and big on features are the key advantages addressing the new horizons of the emerging space market.*

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NEW

# picoRTU Demonstrator

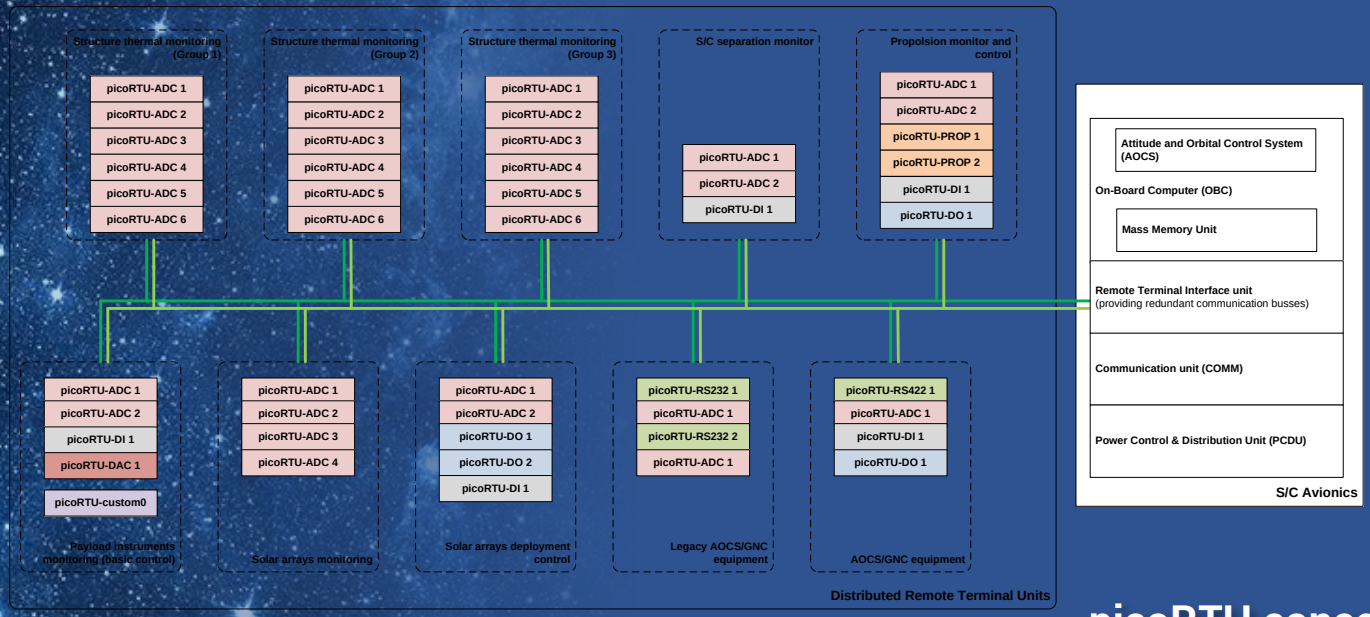
*European Space Agency GSTP activitiy*

*Activity objectives for building picoRTU*

- *Follow principle of distributed intelegence*
- *Interoperrable communication protocol for RTI*
- *Modular and scalabe RTU bulding block*
- *SAVOIR generic RTU specification*

*System integrator are invited to particiate*

- *System level requirements definitions*
- *User interface requirements*

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**picoRTU concept**

# Thank you and welcome at our stand

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