A 65nm hardened ASIC technology for Space applications

KIPSAT 2.1 / 2.2 activities

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TEC ED/SW final presentation days

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Agenda

- **C65SPACE library description**
- C65SPACE qualification status
- Roadmap and conclusions

C65SPACE top level requirements

- ✓ Reach Space required functionalities
  - ✓ 30 Mgates capacity
  - ✓ Hardened standard-cells and memories
  - ✓ Support for cold-spare IOs
  - ✓ Hardened High speed link (HSSL) up to 6.25Gbit/s
  - ✓ Hardened PLL
- ✓ Reliability
  - ✓ Insure long term reliability during the 20 years operating time of the satellite
  - ✓ Std-cells, RAMs, IOs, high speed link, very low FIT (< 100ppm) over 20 years for temperature range from -55 … +125 degrees (junction temperature / Tj)
- ✓ Radiation
  - ✓ **SEL free up to 60 MeV/mg/cm2** (in worst case conditions VDD / temperature)
  - ✓ **TID = 300krad** (in worst case conditions VDD / temperature)
  - ✓ **Ensure that all offer (std-cells, IOs, memories, PLL, HSSL) is radiation robust & characterized**
- ✓ Compliance with space qualification (ESCC)
  - ✓ Wafer level
  - ✓ Product level
- ✓ Process
  - ✓ Assure stable performances along the C65SPACE manufacturing duration
  - ✓ Space process route frozen, specific process step, 10+ years supply guaranteed

Starting point ST65nm commercial process

- 65nm-LP CMOS from ST France : European technology, ITAR free
- 65nm CMOS commercially qualified in 2007
- 65nm CMOS Bulk Process :
  - Dual / Triple Gate Oxides
  - Dual / Triple Threshold Voltages for MOS Transistors
  - 7-9 Full Copper Dual Interconnect Levels
  - Low K

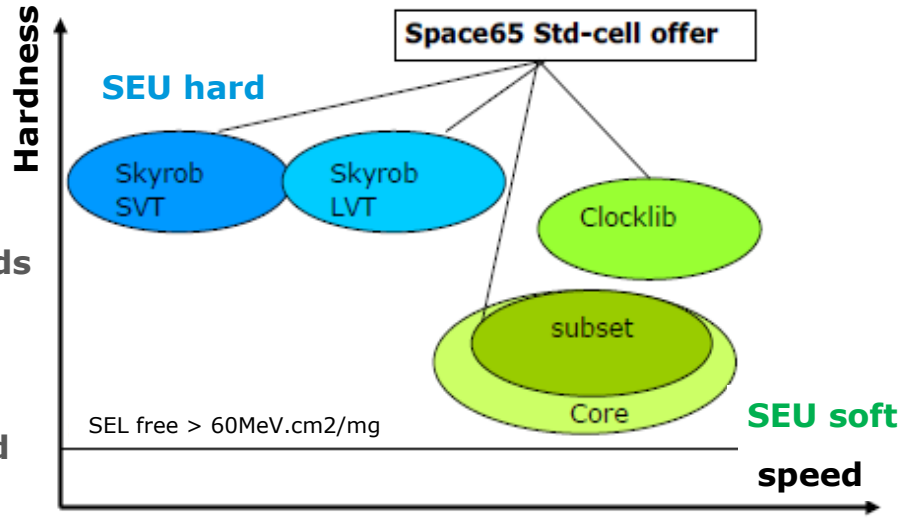
- performances:
  - 750 kgates/mm2
  - 2GHz stdcells
  - 5.7nW/(MHz x gates)
  - 1.25-7.5GBit/s HSSL modules

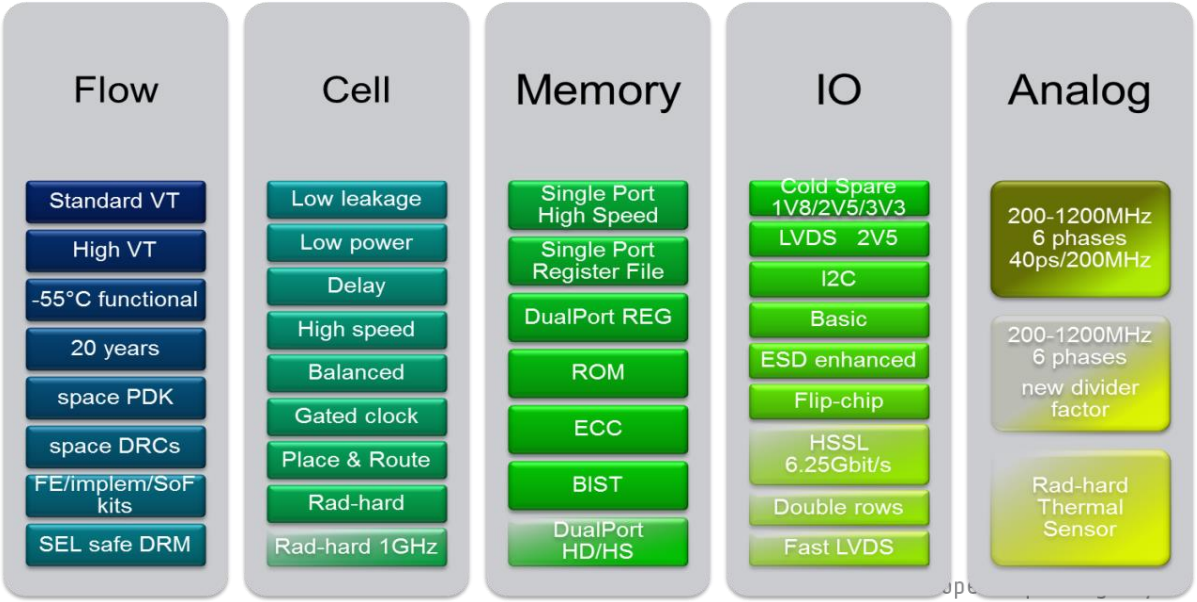
❖ ST Rad Hard offer based on CMOS 65nm-LP commercial process
❖ Reliability and Radiation maximisation performed at design stages

C65SPACE hardened process derived from ST65nm Low Power commercial process

C65SPACE offer

- **Libraries allowing best design trade off between speed, area, power and radiation hardening**
  - SEGR & SEL immune
  - SEU performance adjusted according local design needs
- **C65SPACE flow adapted to specific radiation hardening needs**
  - Extended corner cases (Lifetime, Temperature)
  - Extended design rule checks (SEL, SEU)
- **A full rad hard IP offer SEL free > 60MeV, SEU characterised**
  - memory compilers SRAM, ROM
    - ECC RTL wrappers, BIST
  - Cold spare IOs
    - Compatible with wire bond / flip chip
    - CMOS 1.8v, 2.5v, 3.3v
    - I2C
    - LVDS up to 2.6Gbps
  - High Speed Serial Link 6.25Gbps
  - 2x PLL 200MHz … 1.2 GHz
  - Robust flip-flops up to 1GHz
  - Robust combinatorial cells
    - Clock gating, NAND2, IV
    - Clock tree buffers
  - Robust thermal sensors





C65SPACE offer

Qualification domain

- No single event latch-up up to LET=60Mev/mg/cm2 at 125C and Vdd at 1.3V
- No significant parametric drifts up to TID = 300 kradSiO2
- SEU: ultra low fail rates by design and technology (SEU rate divided by up to 500)
- Extended reliability corners over 20 years at VDD max = 1.3V (nominal + 10%)
  - Std-cell, RAMs, IOs → -55 … +125 degrees (Tj)
  - High speed serial link → -55 … + 110 degrees (Tj)

Operational domain

- Mission profile: 20 years at Tj=110 degrees and VDD nom = 1.2V

Features summary

- 7 copper metallization with 5 thin and 2 thick

- Corelib (performance = speed + density + power)

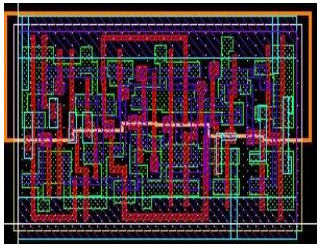
  - 1000+ general purpose cells (high density / non SEU hardened)
  - Standard speed grade cells → Standard Voltage Threshold (SVT)
  - High speed grade cells → Low Voltage Threshold (LVT)

- Skyrob (performance = SEU / SET mitigation)

  - 100+ hardened cells SVT → optimised for leakage current
  - 100+ hardened cells LVT → optimised for speed

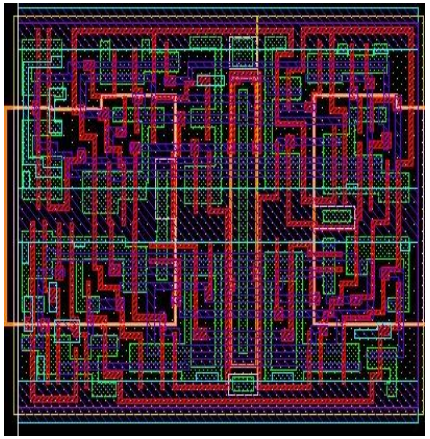
- Clocklib (performance = SET mitigation)

  - 100+ hardened cells SVT
  - 100+ hardened cells LVT



CoreLib Regular Flip-flop

SEU
/100 … /500



SkyRob Rad-hard Flip-flop

C65SPACE hardened DFFs

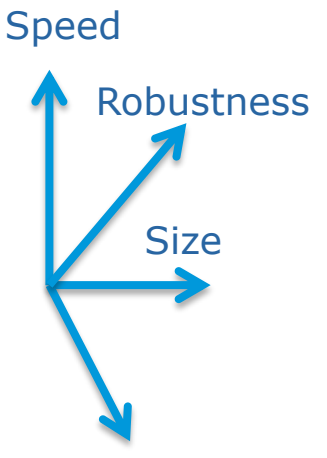
"SEU rate improvement factor with SKYROB ranging from 80 to 500"

Cell type	library	Upset rate in GEO (SEU/bit/day)	Improvement factor compared to standard commercial DFF		description
			best	worst	
Standard DFF from CORELIB with latchup protection	CORE65LPSVT (Standard Vt = Slow)	1.6E-7 (best)	x	x	Reference DFF (commercial lib - CORELIB)
Standard DFF from CORELIB with latchup protection	CORE65LPLVT (Low Vt = fast)	4.1E-7 (worst)	x	x	Reference DFF (commercial lib - CORELIB)
SKYROB65_LSDGURFD12_DFPQX6	SKYROB65LPSVT (Standard Vt)	0.812E-9	197	**504**	Harden DFF with drive 6. D-type flip-flop with 1 phase positive edge triggered clock, Q output only
SKYROB_LSDGFD12S_SDFPRQTX10	SKYROB65LPSVT (Standard Vt)	1.23E-9	130	333	Harden DFF with drive 10. Scan-out D flip-flop with 1 phase positive edge clock, reset active low, Q and TQ outputs
SKYROB_LSDGFD12S_DFPQX18	SKYROB65LPSVT (Standard Vt)	1.82 E-9	87	225	Harden DFF with drive 18. D-type flip-flop with 1 phase positive edge triggered clock, Q output only

Data computed with tool web based CREME96

- GEO orbit @ solar quiet
- Shielding 100mils Aluminium
- ions up to element Z=92
- Weibull fit from experimental results at RADEF (December 2010)

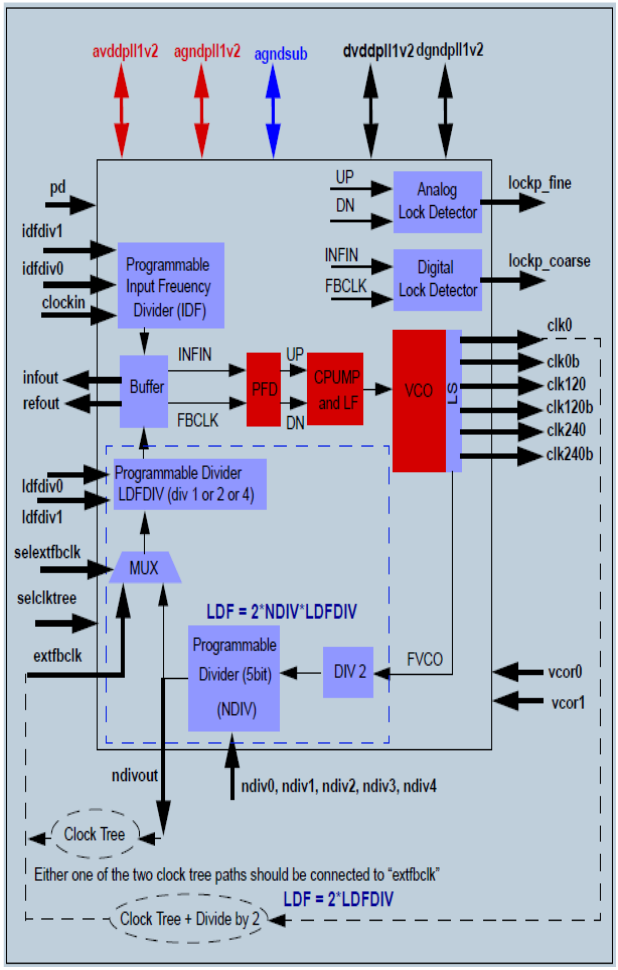
C65SPACE hardened memories



Memory model	Word Count	Mux Range	Voltage Range Supported	Reliability	Radiations
Dual port high speed C65LP_ST_DPHS_SPACE **Large memory block**	64-8K	8	1.1V - 1.35V	**Sustain 20 years, worst case operations**	**Full immune with ECC against GEO harsh radiations**
Dual port high density C65LP_ST_DPHD_SPACE	80-8K	4,8,16	1.1V - 1.35V		
Single port register file C65LP_ST_SPREG_SPACE **Small memory block**	16-2048	2,4,8	1.1V - 1.35V		
Dual port register file C65LP_ST_DPREG_SPACE	16 - 4096	2,4,8	1.1V - 1.35V		
Read only memory C65LP_ST_ROMHS_SPACE	128 - 131072	16,32,64	1.1V - 1.35V		

Comprehensive **Rad Hard** SRAMs offer
single or dual port memory optimised for density or speed

1.2 GHz PLL



Highlights

- 1.2V PLL (for both analog and digital supplies)
- Programmable VCO frequency with very wide VCO frequency range
- 6 equidistance output clock phases
- Supports clock de-skew (with delay up to 8ns)
- Digital lock detection for coarse frequency lock
- Analog lock detection for fine phase lock
- Static Phase error : Reduced to +/-125ps v/s +/-200ps for earlier PLL
- Maximum Input Frequency : Increased to 400MHz v/s 200MHz for earlier PLL
- Feedback Path and divider change

Area	0.33514 mm^2
Maximum Power	29.25 mW
Analog Supply	1.1V – 1.3V
Digital Supply	1.1V – 1.3V
Input Frequency	20MHz - 400MHz
PFD Frequency	20MHz - 100MHz
VCO Frequency	200MHz - 1200MHz
Output Phases	6 (60 degrees apart)
Pk-pk Period jitter	+/-60ps@200MHz output

2.6 Gbps LVDS

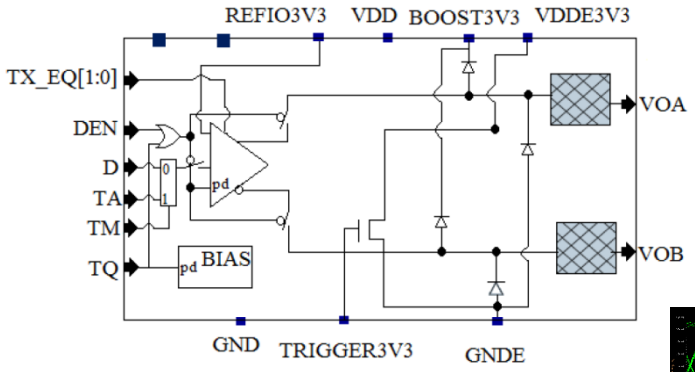
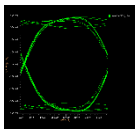


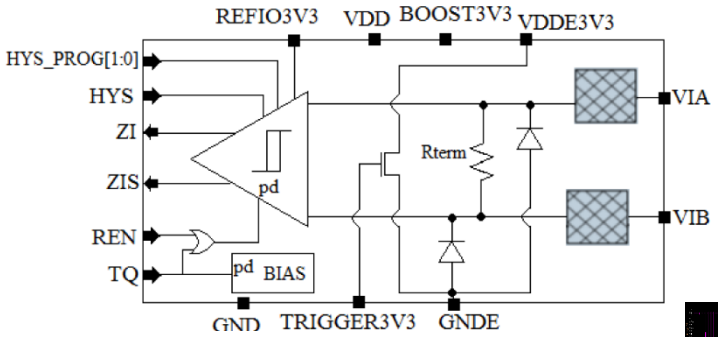
Figure 1: LVDS driver functional diagram

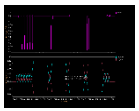


TX eye @ PLS rcc @ 2.6Gbps

Highlights

- Tx / Rx supporting 2.6 Gbps rates
- 1.2V core and 2.5V IO supply
- driver cell is tri-stated when IO-power is up but core power is down
- receiver deactivated when IO-power is up and core power is down
- receiver with: with & w/o termination
- programmable hysteresis
- flipchip and wirebond configuration
- coldspare IO



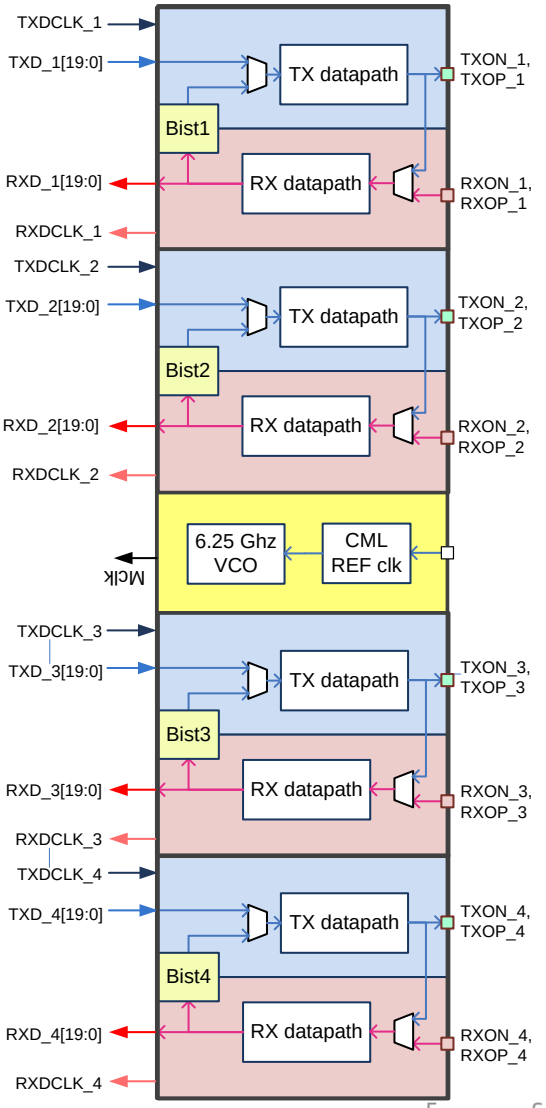


Demonstration of RX reception capability @ 2.6Gbps

Area	Tx: 0.044 mm^2 Rx: 0.046 mm^2
Maximum Power	xx.xx mW
Analog Supply	2.25V – 2.75V
Digital Supply	1.1V – 1.3V
Input Frequency	20MHz - 400MHz
PFD Frequency	20MHz - 100MHz
VCO Frequency	200MHz - 1200MHz
Output Phases	6 (60 degrees apart)
Pk-pk Period jitter	+/-60ps@200MHz output

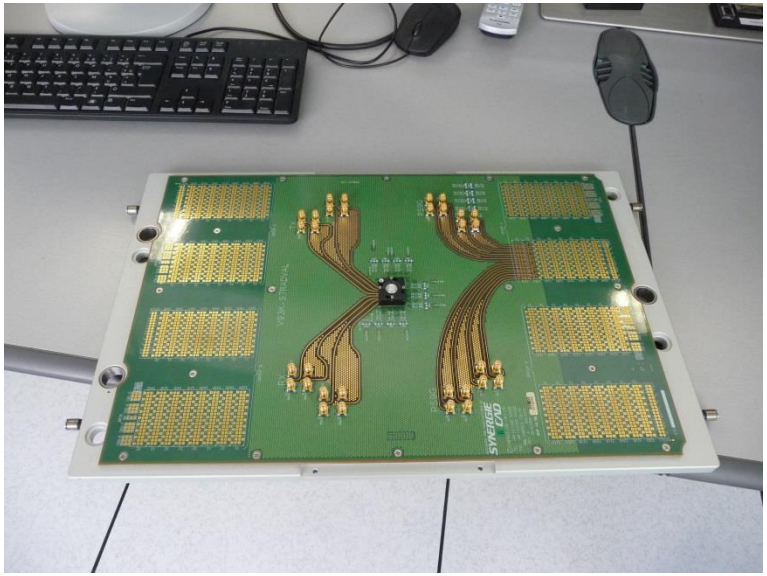
6.25 Gbps High Speed Serial Link

- ✓ HSSL IP features
  - ✓ BER < 10^{-14}
  - ✓ 4 independent serialisers/deserialisers on the same IP (data lanes)
  - ✓ Each data lane configurable in half or full duplex
  - ✓ 3 programmable rates, 6.25 Gbps, 3.125 Gbps or 1.5625 Gpbs
  - ✓ 25 Gbps aggregated data rate in half duplex
  - ✓ 50 Gbps aggregated data rate in full duplex
  - ✓ Differential CML input / output (serial interface)
  - ✓ 4 TAP programmable pre-emphasis
  - ✓ 4 TAP adaptive decision feedback equaliser (DFE)
  - ✓ Clock data recovery for pleisio synchronous operations
  - ✓ JTAG & BIST (PRBS for auto test)



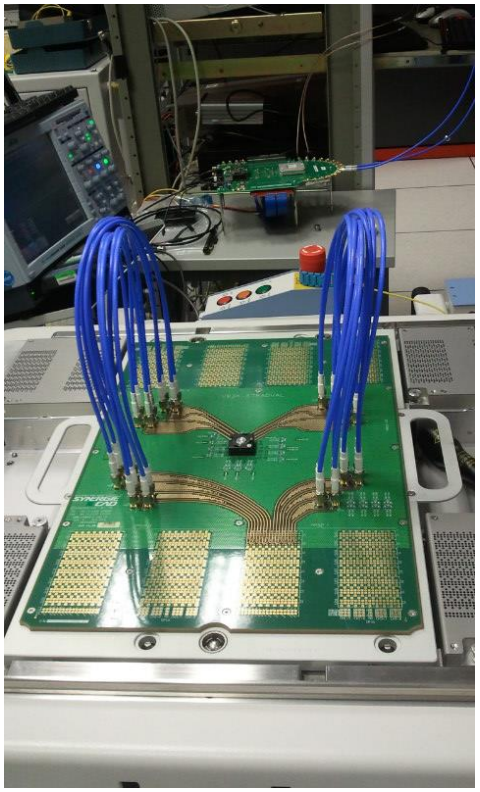
Note: data slice = Tx lane + Rx lane

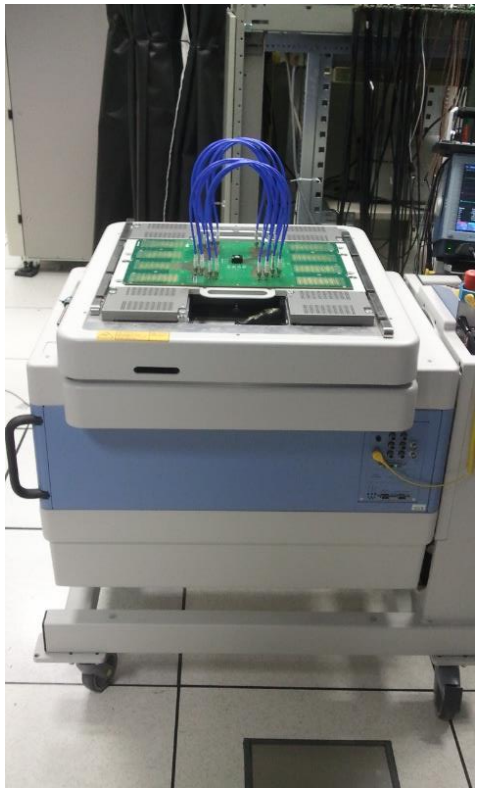
HSSL IP electric characterisations activities (ATE)



Advantest board

Co-developed by ESA-CNES





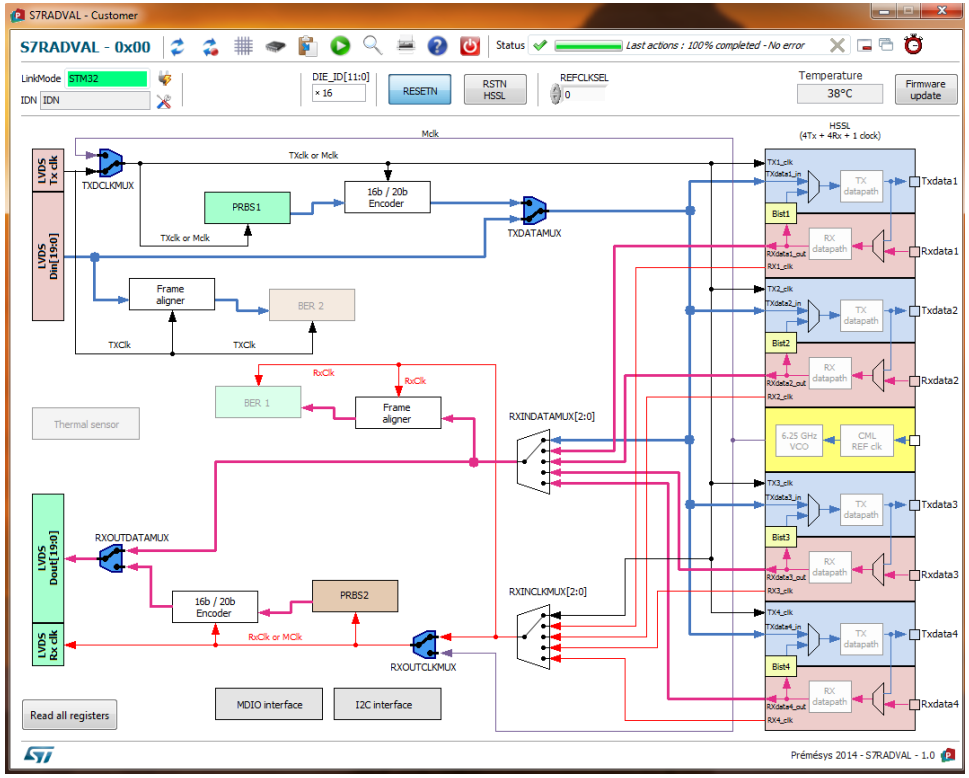
automatic test equipment
high speed testing capability

internal / external loopbacks
@ max data rate (6.25 Gbps)

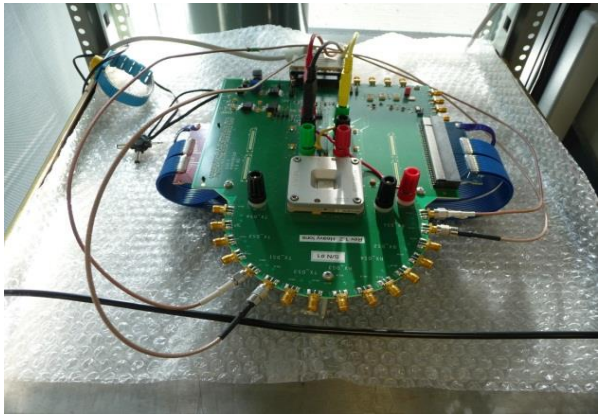
1024 digital pins @ 1.6 Gbits/s
64 digital pins @ 9 Gbits/s

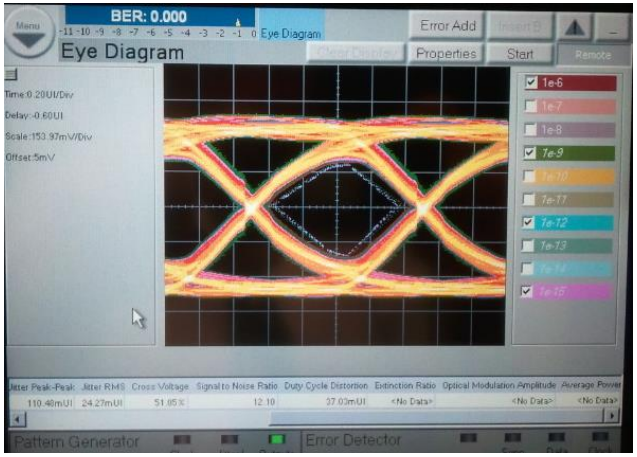
HSSL IP BER setup

S7RADVAL : New graphical interface for Validation



Electric characterisation board





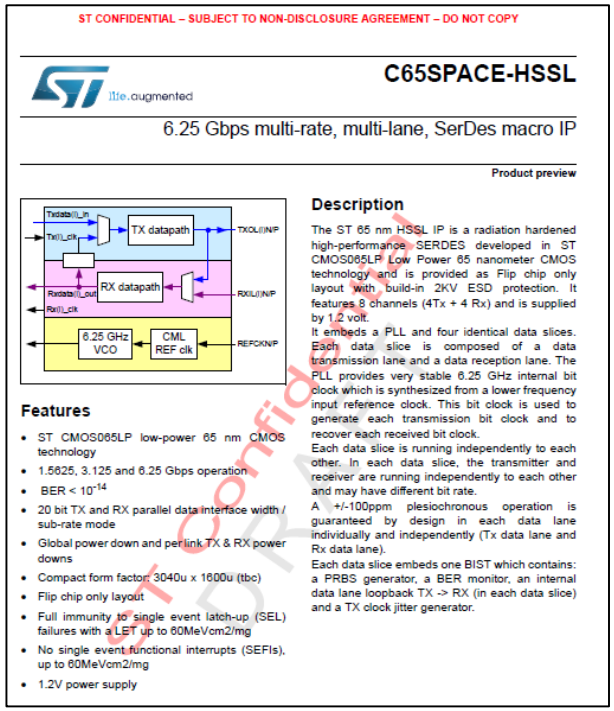
Agilent 4903B High performance serial BER analyser

Full data rate acquisition performed @ 6.25Gbps with (PRBS 31)

ESA-CNES measurement with equipment loaned by TAS-F

HSSL IP BER characterisations results

HSSL IP datasheet



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C65SPACE-HSSL

6.25 Gbps multi-rate, multi-lane, SerDes macro IP

Product preview

Description

The ST 65 nm HSSL IP is a radiation hardened high-performance SERDES developed in ST CMOS065LP Low Power 65 nanometer CMOS technology and is provided as Flip chip only layout with build-in 2KV ESD protection. It features 8 channels (4Tx + 4 Rx) and is supplied by 1.2 volt.

It embeds a PLL and four identical data slices. Each data slice is composed of a data transmission lane and a data reception lane. The PLL provides very stable 6.25 GHz internal bit clock which is synthesized from a lower frequency input reference clock. This bit clock is used to generate each transmission bit clock and to recover each received bit clock.

Each data slice is running independently to each other. In each data slice, the transmitter and receiver are running independently to each other and may have different bit rate.

A +/-100ppm plesiochronous operation is guaranteed by design in each data lane individually and independently (Tx data lane and Rx data lane).

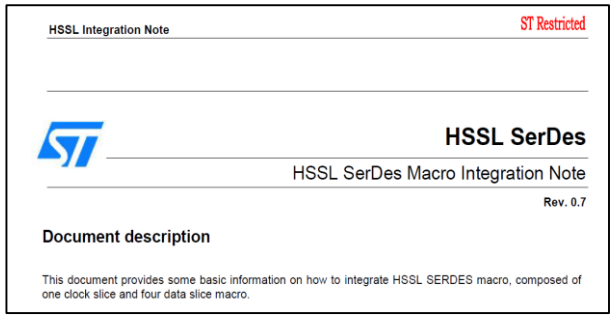
Each data slice embeds one BIST which contains: a PRBS generator, a BER monitor, an internal data lane loopback TX -> RX (in each data slice) and a TX clock jitter generator.

Features

- ST CMOS065LP low-power 65 nm CMOS technology
- 1.5625, 3.125 and 6.25 Gbps operation
- BER < 10^{-14}
- 20 bit TX and RX parallel data interface width / sub-rate mode
- Global power down and per link TX & RX power downs
- Compact form factor: 3040u x 1600u (tbc)
- Flip chip only layout
- Full immunity to single event latch-up (SEL) failures with a LET up to 60MeVcm2/mg
- No single event functional interrupts (SEFIs), up to 60MeVcm2/mg
- 1.2V power supply

ST Confidential
DRAFT

HSSL IP integration note



HSSL Integration Note — ST Restricted

HSSL SerDes

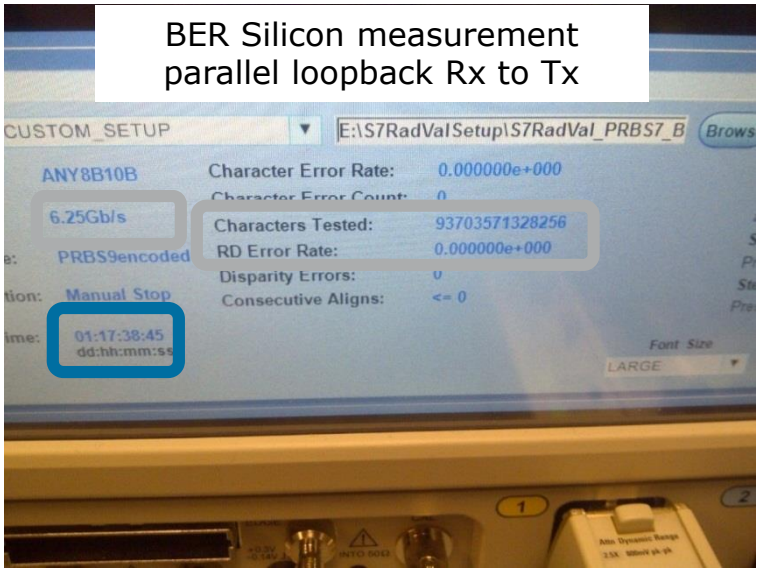
HSSL SerDes Macro Integration Note

Rev. 0.7

Document description

This document provides some basic information on how to integrate HSSL SERDES macro, composed of one clock slice and four data slice macro.

BER Silicon measurement
parallel loopback Rx to Tx



After 6 days
0 errors @ 6.25Ghz
BER=1^{e}-15, CL=96%

Figure 7: RADI

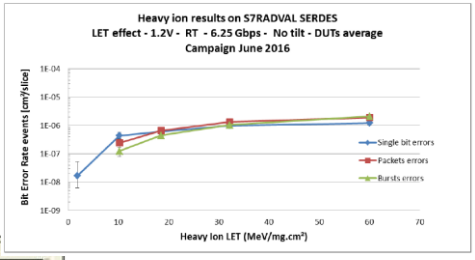


Figure 8: RADEF Monitoring Software

No SEL, No SEGR
SEU Register Event
in GEO orbit is
<5.10-8 event/day

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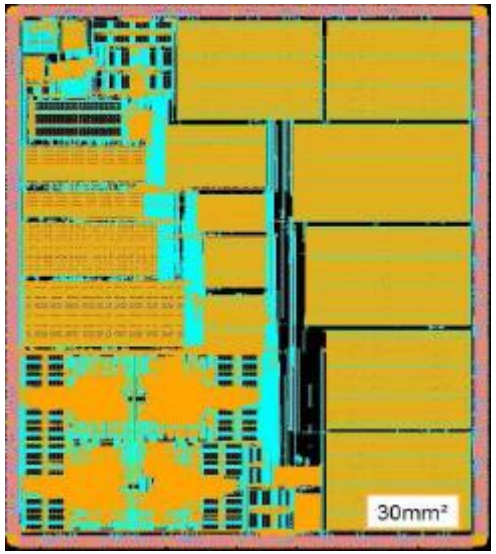
C65SPACE test vehicles

TC1 (rad hard digital library):

- SKYROB65 ALLCELL blocks
- SKYROB65/CORE65 ROs
- FF shifters SKYROB65LP
- SRAM compilers
- Application digital blocks

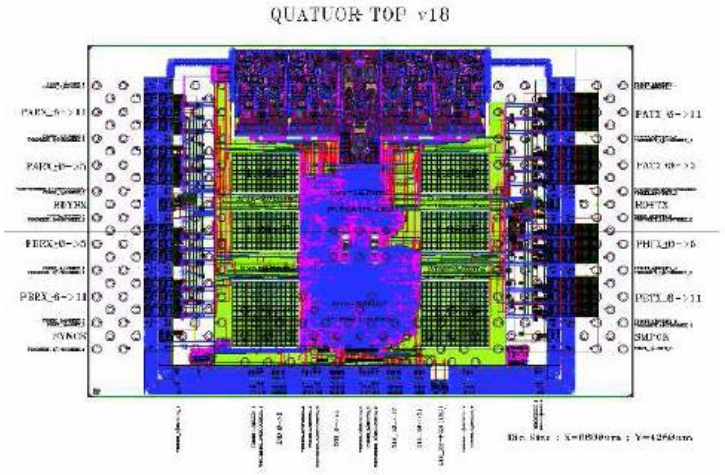


TC2 (rad hard analog library):

- high performance multiphase hardened PLL covering frequency range from 50MHz … 1.2 GHz (6 phases)
- special IOs
  - cold spare CMOS
  - cold spare LVDS
  - Signal
  - I2C

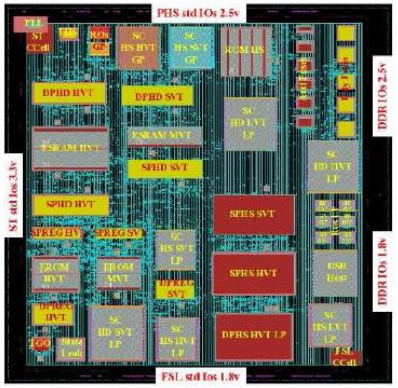
TC3 (rad hard high speed serial link):

- Quatuor / S7RADVAL quad high speed link 4 x 6.25 Gbps

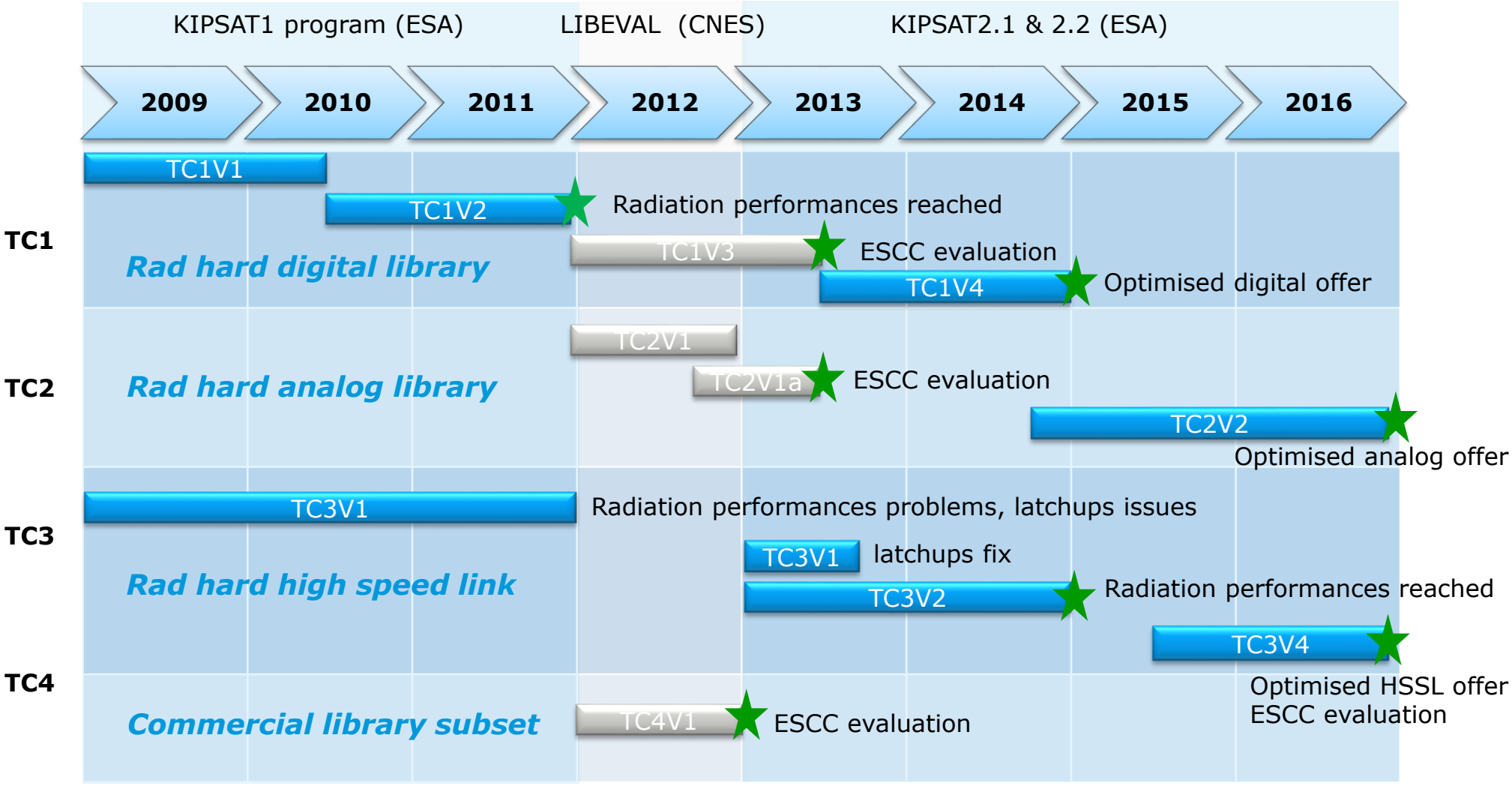


TC4 (C65 commercial library subset):

- Corelib 1000 general purpose cells



C65SPACE test vehicles development plan



12 test vehicles developed

Platform MAT30 – HTOL conclusions

Conditions	Vehicle	Lot	Parts	T°j	Vdd	RP 0h	RP 48h	RP 168h	RP 500h	RP 1000h	Equ. Life time for last RP
HTOL: **FIT rate measurement > 20 years**	**Digital vehicle TC1**	HTOL1	77	125°C	1V68	✓	✓	✓	✓	✓	34.33 yr
		HTOL2	77	150°C	1V68	✓	✓	✓	–	–	27.14 yr
		HTOL3	77	125°C	1V44	✓	✓	✓	–	–	0.25 yr
	Analog vehicle TC2	HTOL1	77	125°C	1V80	✓	✓	✓	–	–	27.45 yr
		HTOL2	38	150°C	1V80	✓	✓	✓	–	–	129.14 yr
		HTOL3	38	125°C	1V44	✓	✓	✓	–	–	0.25 yr

Courtesy CNES: results produced in the frame of CNES LIBEVAL activity

HTOL1: OLT trial addressing 65nm space generic mission profile
HTOL2 & HTOL3: acceleration factors investigations to ensure 20 years equivalent life time (Voltage & Temperature accelerations)

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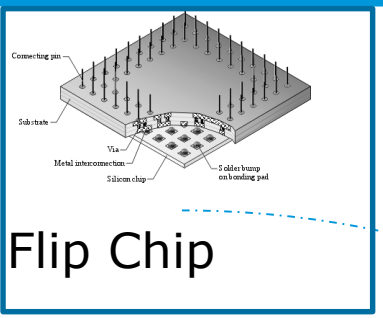
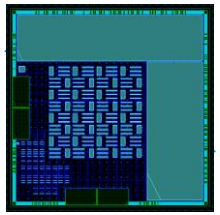
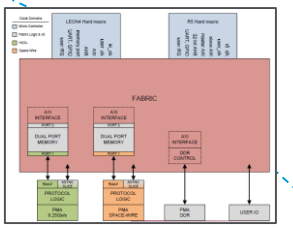
C65SPACE roadmap



Flip Chip



Thales telecom ASIC
(flight model)



NGFPGA
Large

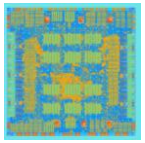
2019

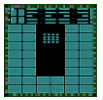
2018

2017

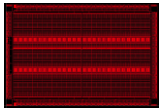
2016

VT65
telecom





HPDP

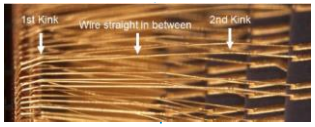


NGFPGA
Medium

NGMPU

TTC

WireBond



European Space Agency

Conclusions

- ✓ ST 65nm hardening activities are completed
- ✓ ~ 3000 pages data book compiling datasheets + radiation reports (HI + Protons + Gamma)
- ✓ 4.5M€ may appear as a large envelope but has been very challenging to complete all tasks described in the presentation and the 12 test vehicles manufactured and characterised
- ✓ ST C65SPACE flow deployed to Alpha users in 2015 (Thales, Airbus and Cobham Gaisler)
- ✓ Three application chips have been produced and functionally validated in 2015/2016
  Four additional application chips have been produced and are currently under validation in 2017
- ✓ HSSL IP hardening has required significant efforts, 5 iterations. The last update fully validated under radiations has been released in Q1/2017
- ✓ Two new IPs introduced in Q1/2017. PLL02 (1.2 GHz) and LVDS02 (2.6 Gbps).
- ✓ Telecom ASIC designed by Thales ~ half Billion transistors, 1000 memory instances, 32 HSSL IP @ 6.25Gbps each. Probably the most complex ASIC ever developed for Space applications.

Conclusions

Perspectives beyond 65nm

- ✓ Future developments will benefit from the lessons learned on ST C65SPACE program. C65SPACE has paved the way for future developments with ST.
- ✓ ST Fully Depleted SOI technologies 28nm / 14nm are promising nodes with respect to radiation hardening
  - ✓ Better starting point with respect to latchup and SEU hardening
  - ✓ Self heating might be an issue to tackle with care but FDSOI is a better starting point compared to “bulck” CMOS
- ✓ Cost might be a limiting element for the development and qualification of general purpose ASIC technology beyond 65nm node
- ✓ Economic considerations will instead push for the design and qualification of standard products (micro processor or FPGA)
- ✓ Necessity to tackle reliability not only at technology level but also at architecture level with concepts such as FPGA, Network on Chip or GPU (many cores).

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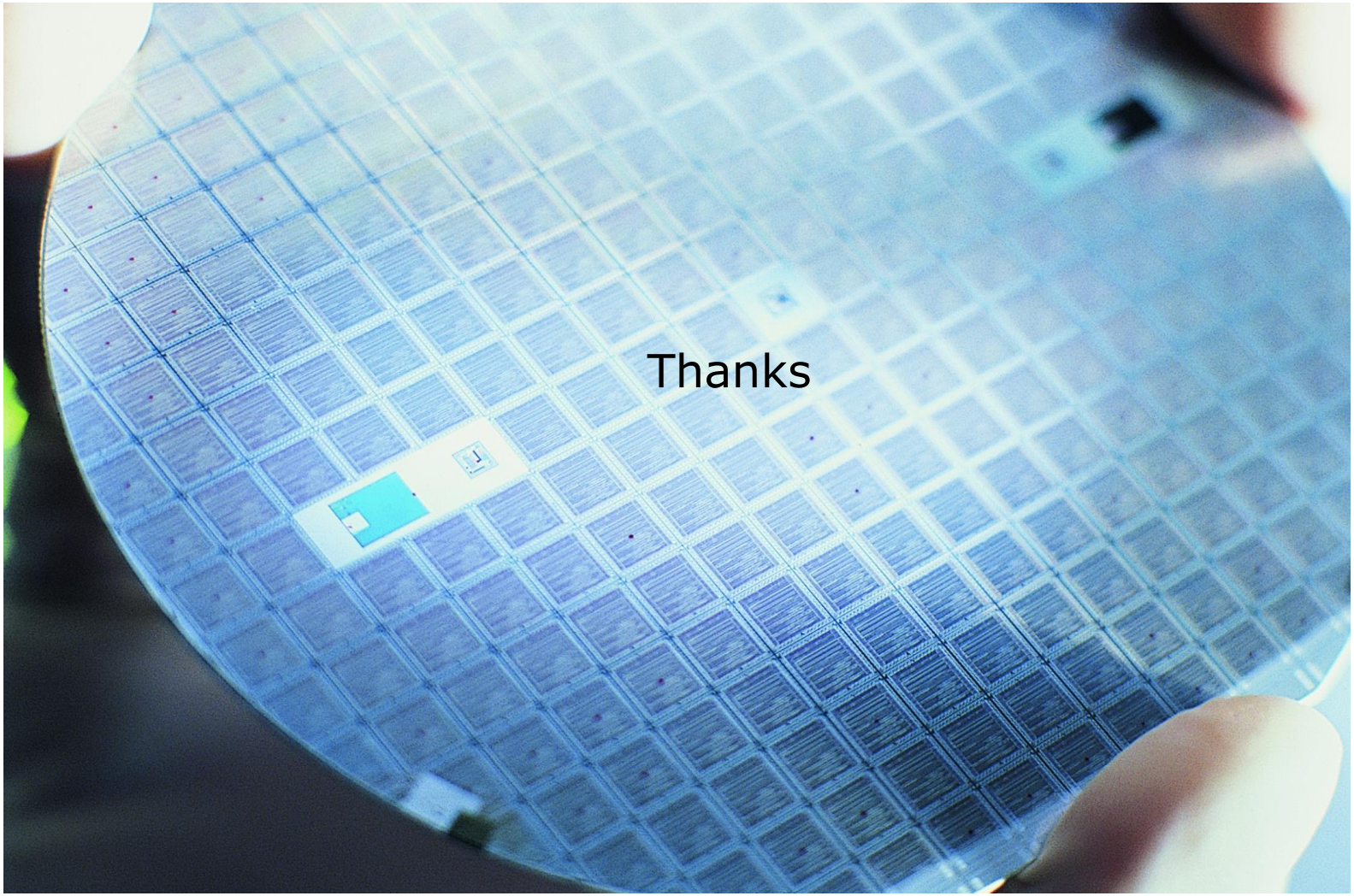
- ✓ Acknowledgements to TAS Toulouse, Airbus, ISD and Cobham Gaisler for their support in validating ST design flow on real applications cases (Telecom ASIC, High Performance Data Processor and Next Generation Microprocessor)


Thanks