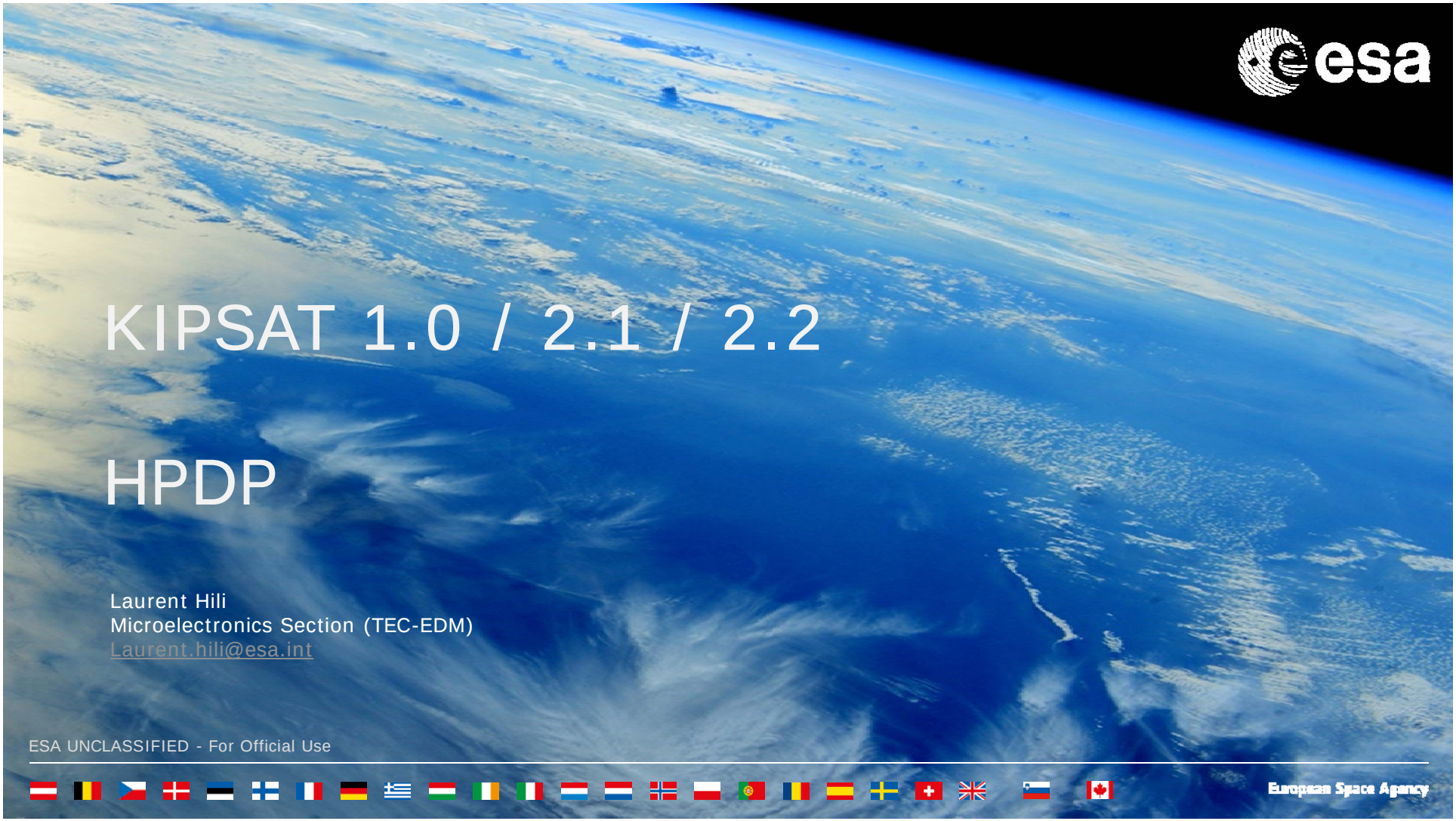


KIPSAT 1.0 / 2.1 / 2.2

HPDP

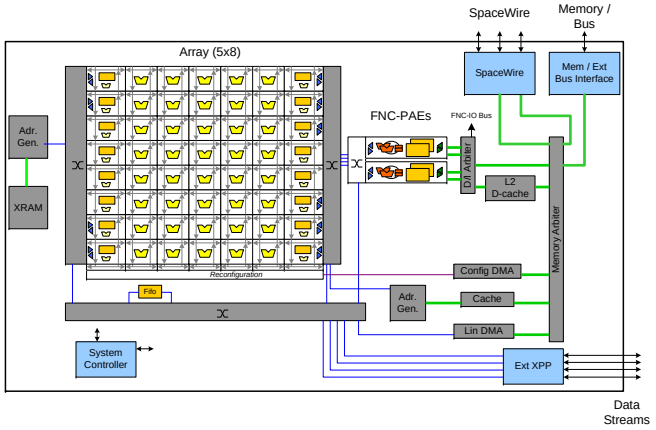
Laurent Hili
Microelectronics Section (TEC-EDM)
Laurent.hili@esa.int

KIPSAT 1.0 /2.1 / 2.2

- Activity title: KIPSAT (**K**ey **IP**s for **SAT**ellites)
- Budget / program: TRP ~ 4.5M€
- Duration: 9 years (kick off Phase1.0 in February 2008)
- Prime and subco:
  - Prime: STMicroelectronics Grenoble
  - Subco: ISD, Thales, Airbus
- Objectives:
  - To harden the commercial ST 65nm ASIC technology for Space applications
  - To harden high speed serial links (HSSLP IP operating @ 6.25Gbps)
  - To evaluate reliability and radiation effects through dedicated test vehicles
  - To validate ST design flow through real application cases

HPDP

- ✓ Activity title: HPDP (**H**igh **P**erformance **D**ata **P**rocessor)
- ✓ Budget / program: GTF ~ 480K€
- ✓ Duration: 7.5 years (Kick off September 2009)
- ✓ Prime and subco:
  - ✓ Prime: ISD
  - ✓ Subco: Airbus Ottobrunn



- ✓ Objectives:
  - ✓ To develop a high performance DSP processor capable of delivering 40 Giga operations per second (ALUs 16bits fixed point)
  - ✓ To develop a highly parallel architecture in order to reach the performance level targeted (40 ALUs in parallel)
  - ✓ To keep the clock frequency to a moderate value (300 MHz) to mitigate the power consumption
  - ✓ To emulate floating point operations for specific applications where high dynamic range is needed
  - ✓ To have a scalable architecture (multi-chips on the same board)
  - ✓ To allow dynamic in-flight reconfiguration
  - ✓ To allow electric interfacing with common standards (SpaceWire)
  - ✓ Low complexity package to allow easy PCB mounting (CGA 625)