KIPSAT 2.1, 2.2

The ever increasing electronic miniaturisation has deeply changed our daily life with computers, mobile phones and more recently internet of things. While being more conservative the Space sector does not escape to this general trend. However Space electronic has to deal with extra constraints such as extreme temperature range (-55 … +125C), radiation environment and long term reliability (missions profiles up to 20 years). The Deep Sub Micron program initiated by ESA and CNES in 2008, set as a main objective to harden the commercial ST 65nm node and provide European Space industry with a state of the art ASIC technology free of any US export licences (ITAR). Today ST 65nm hardened process (C65SPACE) is one of the most advanced ASIC technology suitable for Space missions. The current presentation will give an overview of the last 9 years achievements putting the emphasis on hardening activities and features available in the final offer (Design platform). ST C65SPACE technology represents a major leap with respect to the previous generation of hardened ASIC technology (180nm). Finally, the presentation will conclude by listing few showcases where C65SPACE has been successfully deployed leading to major performances breakthrough (telecom, microprocessors, FPGAs, network applications).