SETA tool update: SETs in Flash-based FPGAs

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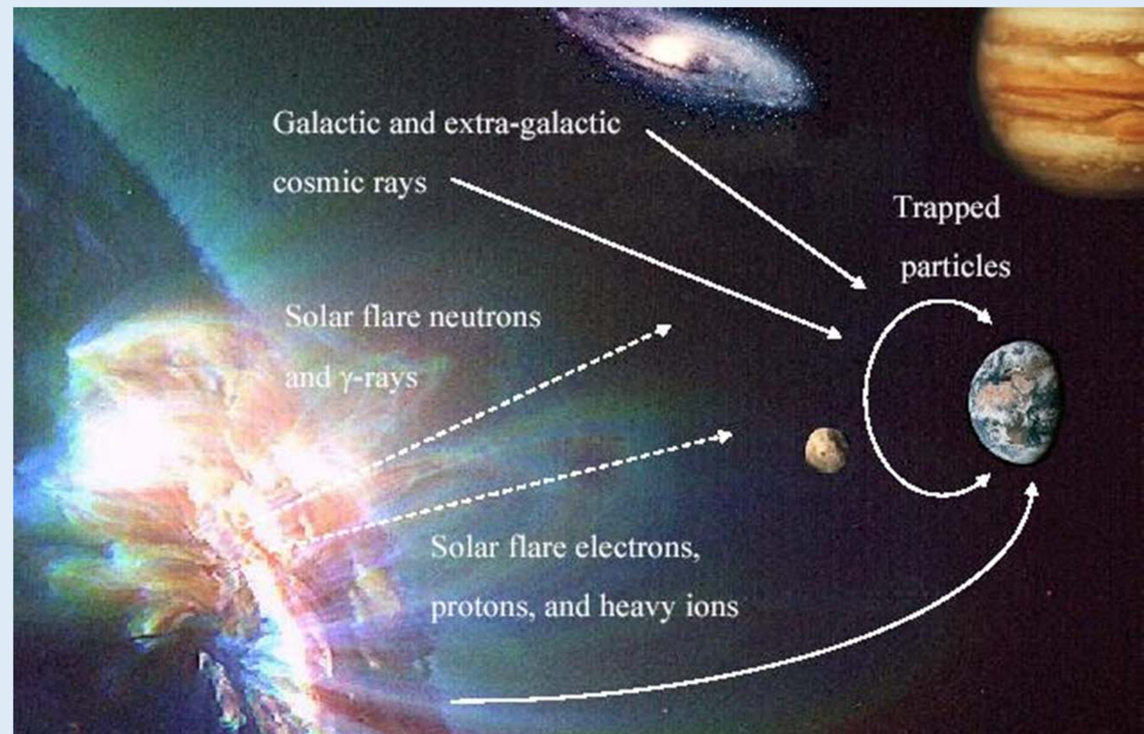
Motivations

Space environment is characterized by several types of radiation particles:

Heavy ions

Protons

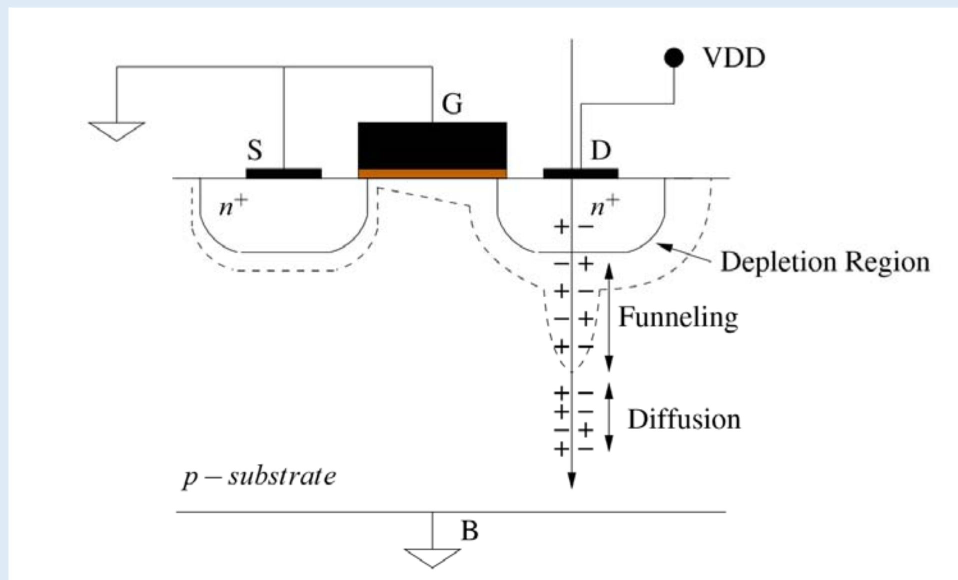
Neutrons

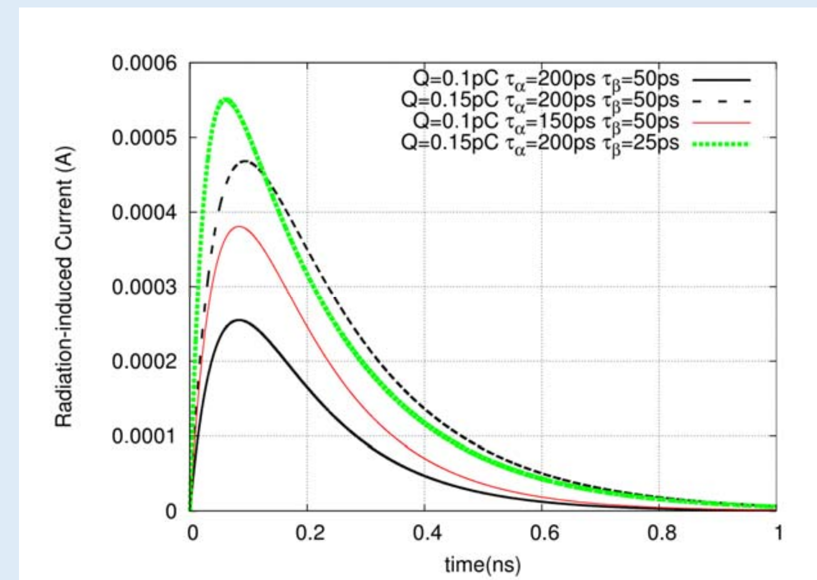


Motivations

Charge deposition and collection by a **radiation particle strike crossing the silicon structure**

Creation of a **current pulse** for a radiation particle strike

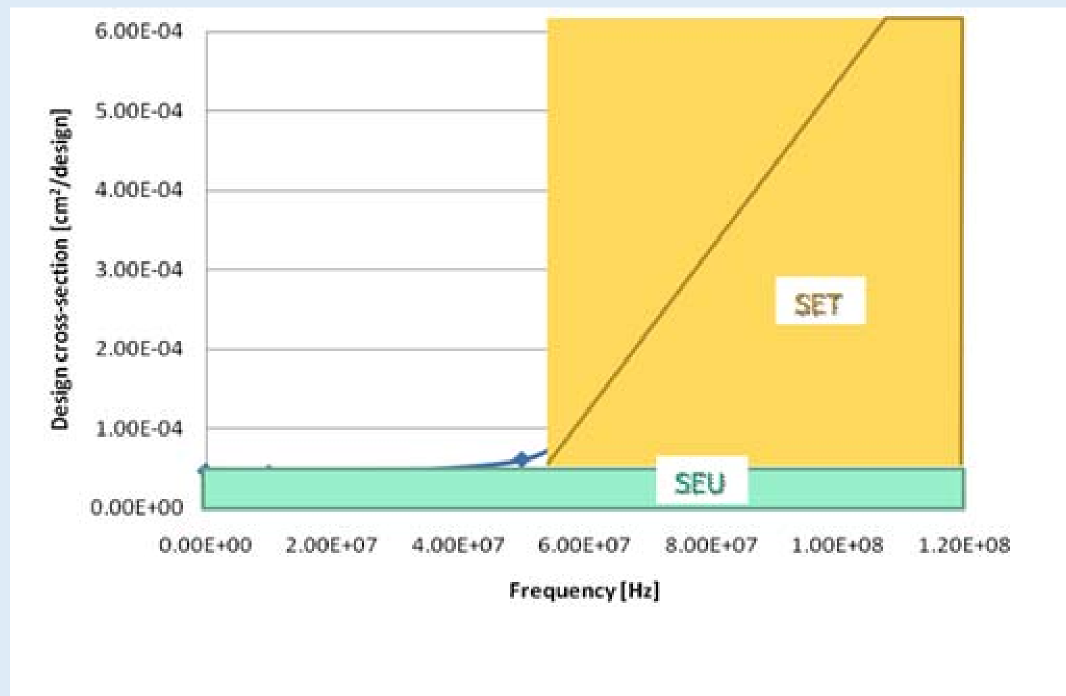




L.D. Edmonds, “A simple estimate of funneling-assisted charge collection”
IEEE Transactions on Nuclear Science, vol.38, no.2, pp.828–833, 1991

Motivations

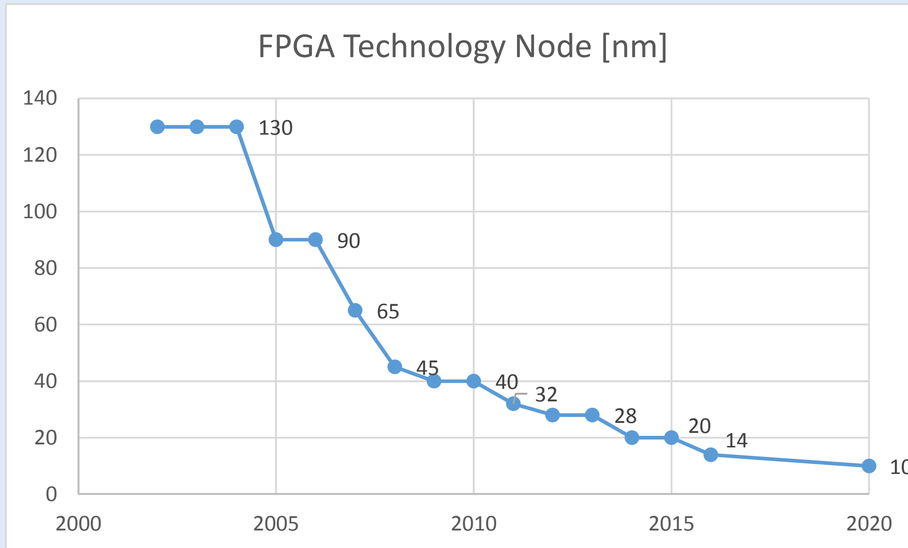
Circuit Error Cross-Section sensitiveness is frequency dependent



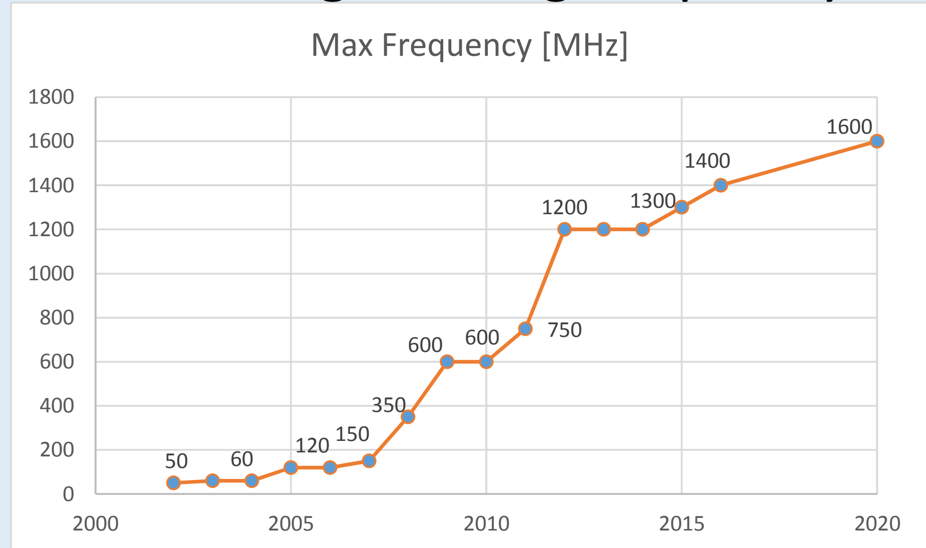
N. Battezzati, S. Gerardin, A. Manuzzato, D. Merodio, A. Paccagnella, C. Poivey, L. Sterpone, M. Violante "Methodologies to study freqyency-dependent Single Event Effecst sensitivity in Flash-based FPGAs", 2009
IEEE Transactions on Nuclear Science, Vol. 56, pp. 3534 – 3541, ISSN 0018-9499

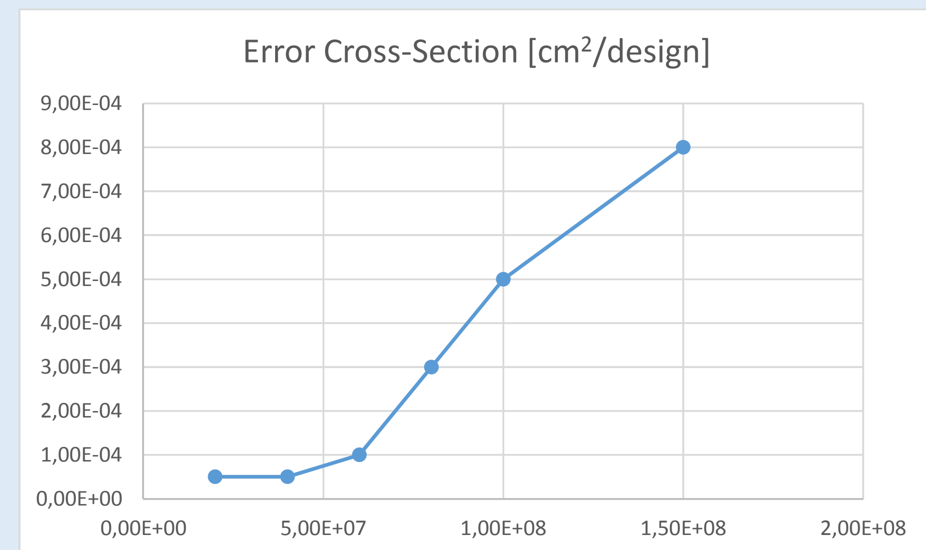
Motivations

Technology scaling



Increasing working frequency





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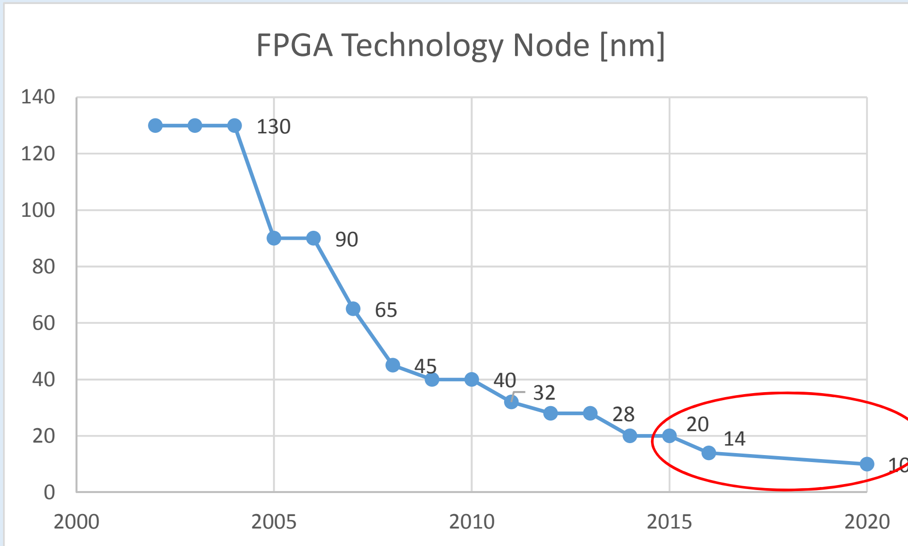

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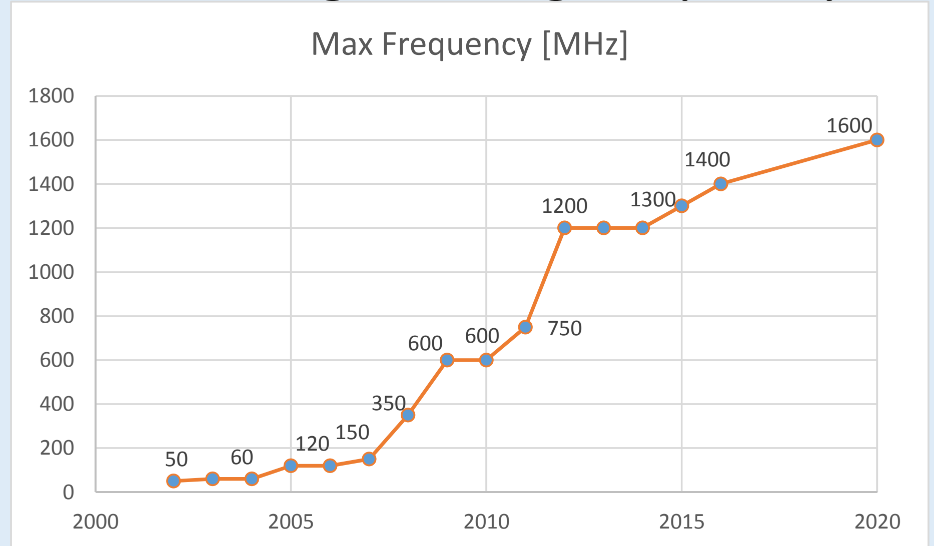
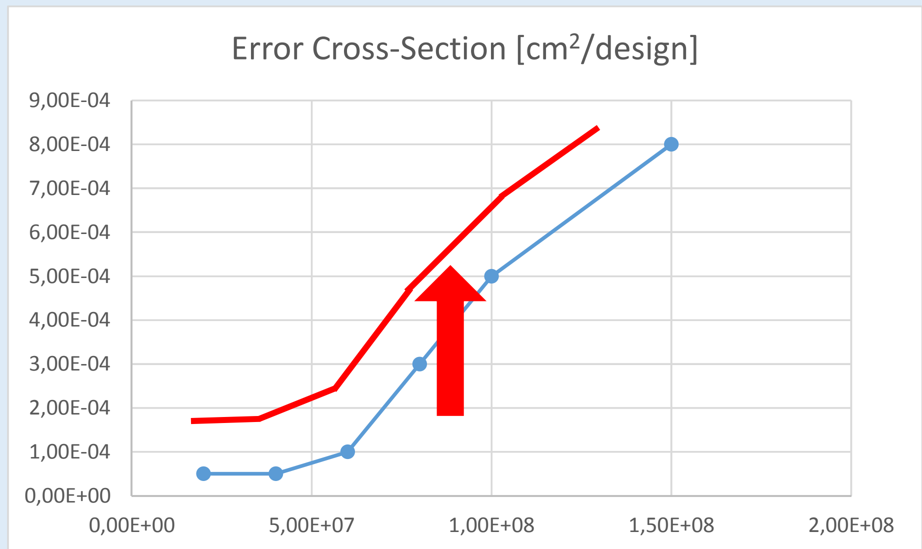


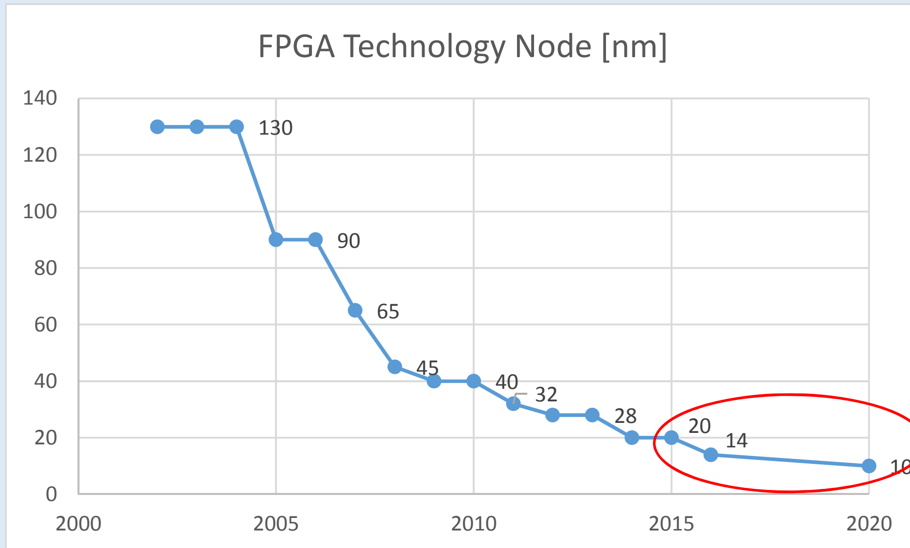
Decreasing device and interconnect dimensions
Reduction in the node capacitances of VLSI

Low energy particle can cause change in the node voltage

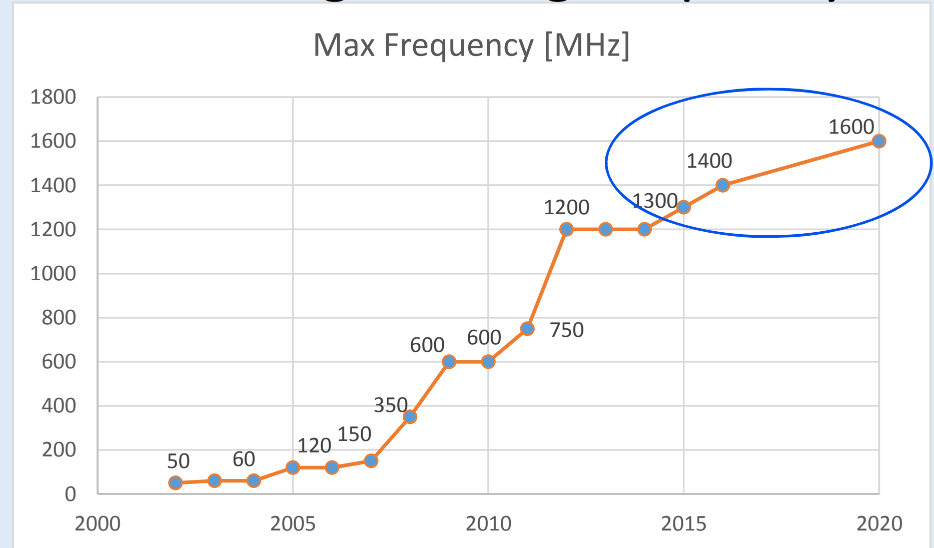


Motivations

Technology scaling



Increasing working frequency

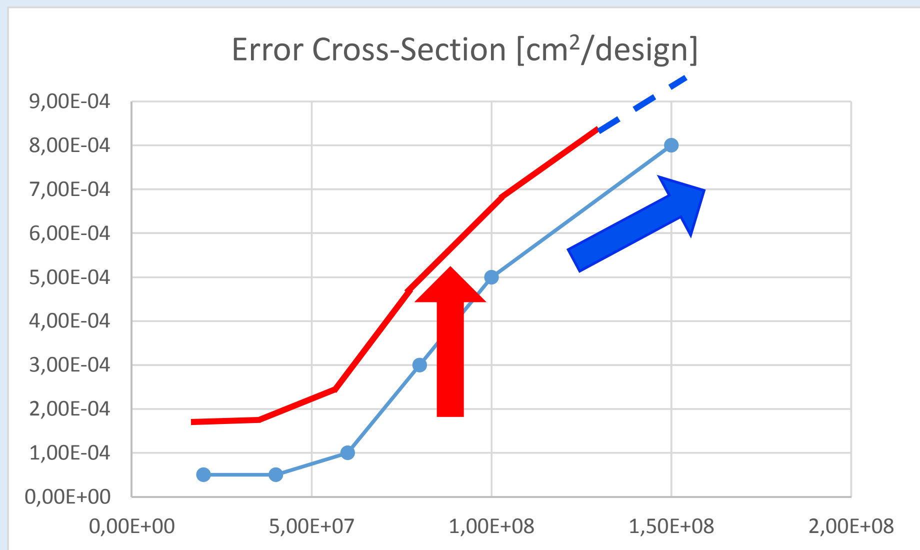


Decreasing device and interconnect dimensions
Reduction in the node capacitances of VLSI

Low energy particle can cause change in the node voltage

Increasing of the maximal working frequency

Drastically increase of the SET effect contribution on the circuit error cross-section

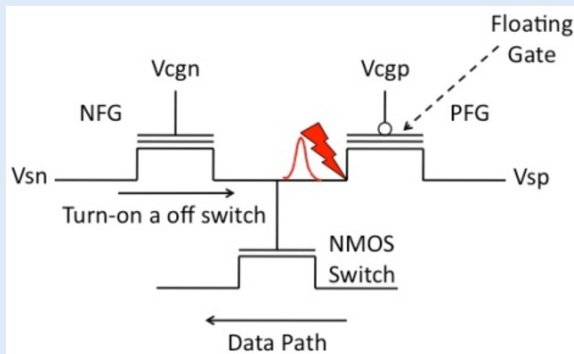


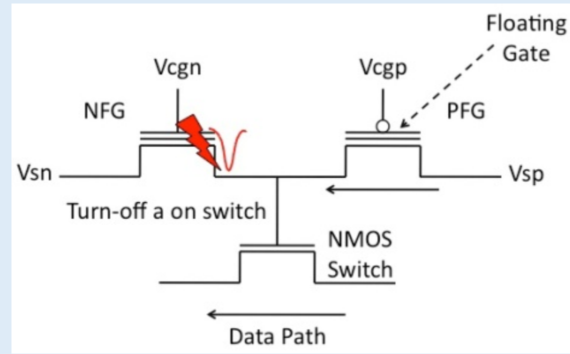
Outline

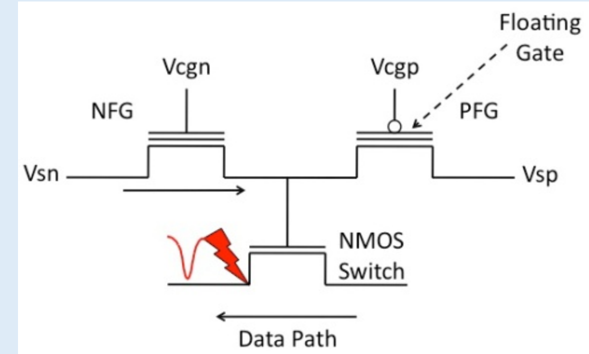
- SET on Flash-based FPGAs
- SET effects analysis
  - Injection
  - Characterization
- Mitigation design flow
- Experimental results
- Conclusions
- Future works

SETs on Microsemi Flash-based FPGAs

- Depending on the configuration, the SET may propagate through the logic or turn into an SEU

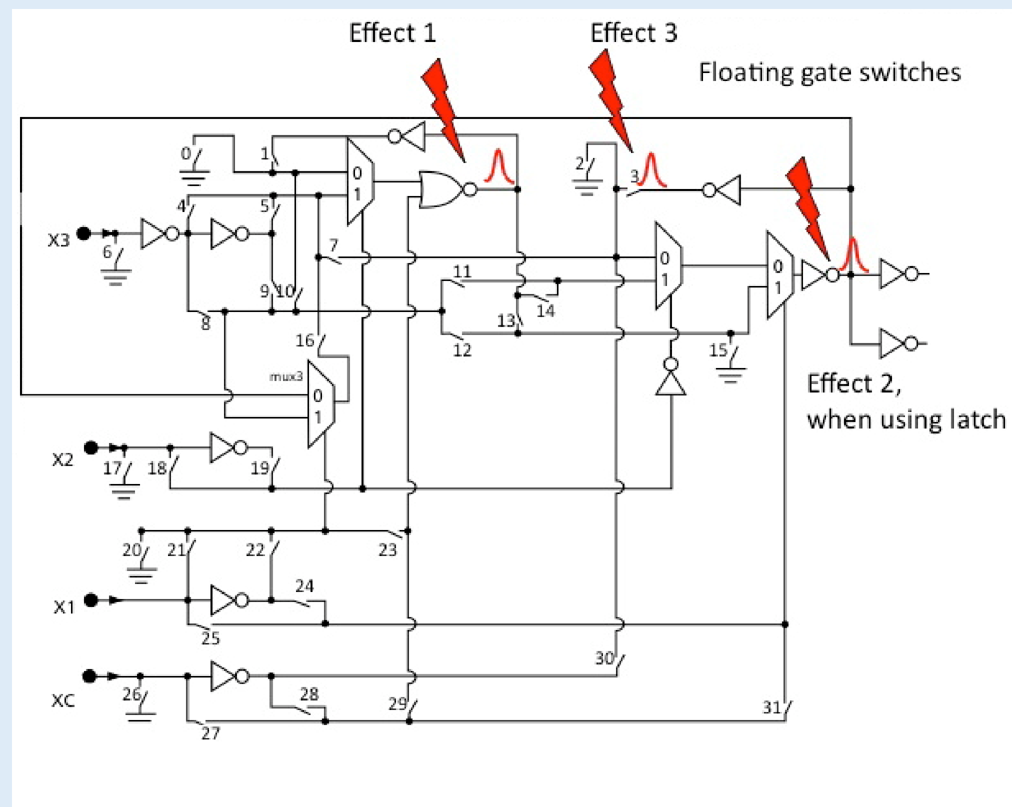






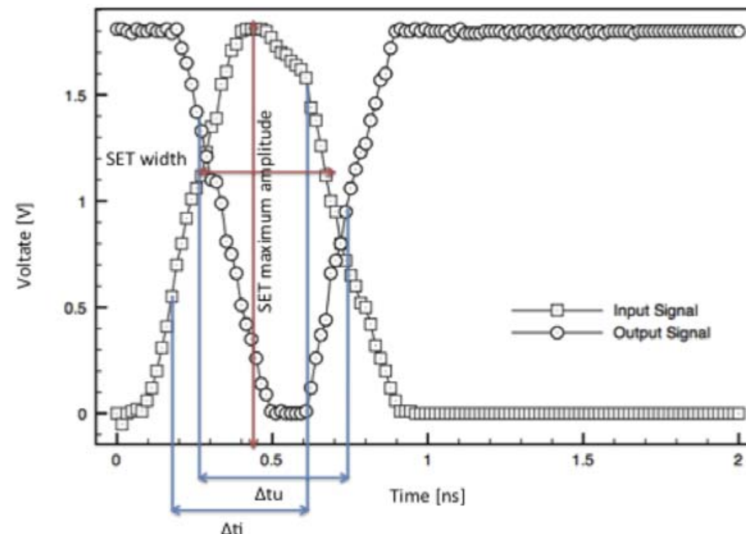
SETs on Microsemi Flash-based FPGAs

- A particle hitting the FPGA's basic block can provoke three effects:
  - 1. it can induce a pulse that propagates through the logic
  - 2. it can affect a logic cell configured as a latch → SEU
  - 3. it can hit a junction in the floating gate switch



SETs on Microsemi Flash-based FPGAs

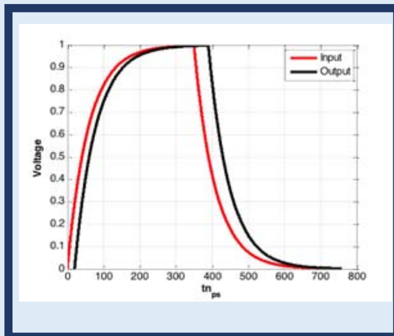
- Gate behavior obtained from electrical measurement of SET propagation
- Propagation Induced Pulse Broadening (PIPB) dependent two parameters:
  - output voltage differences: SET_{DMAX}
  - width of the SET pulse: SET_{WI}
    - **Broadening coefficient: $C_x = \Delta_{to} - \Delta_{ti}$**
    - **Attenuation coefficent: $A = SET^{I}_{DMAX} - SET^{U}_{DMAX}$**

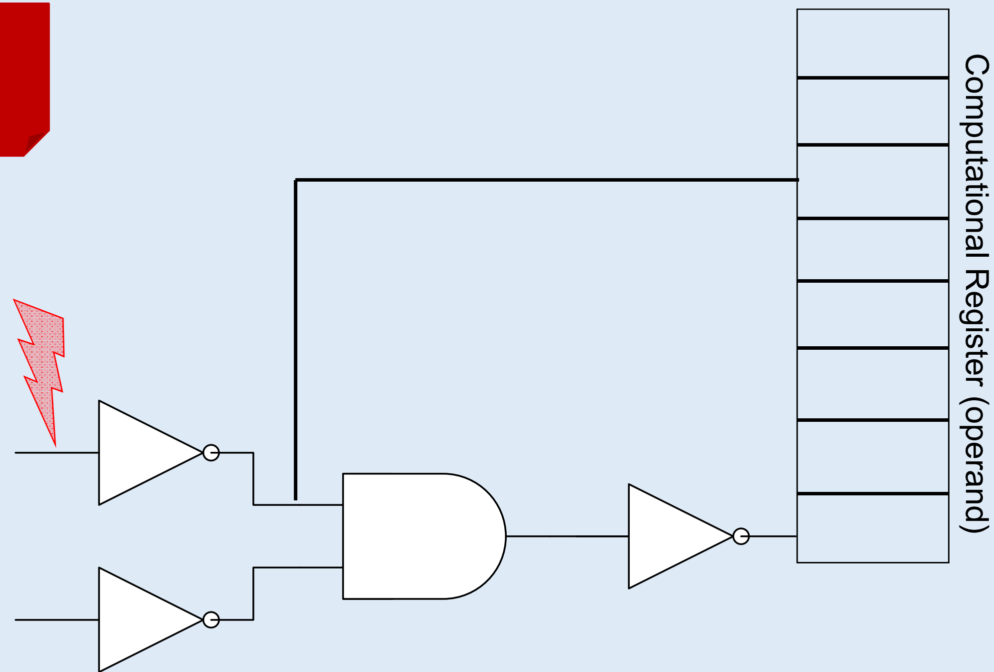


Background

- Single Event Transient

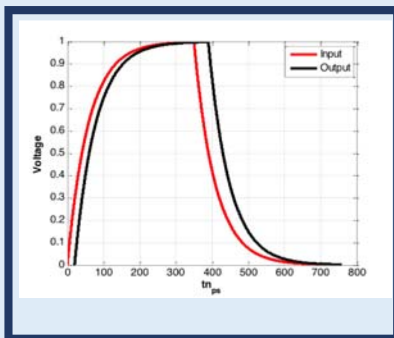
SET generation

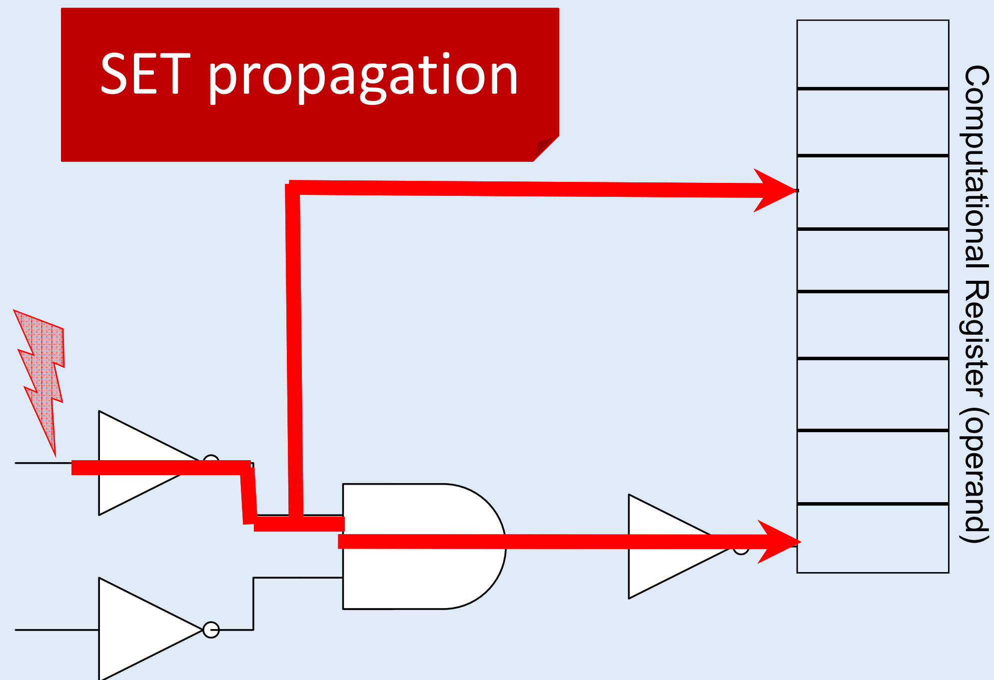




Background

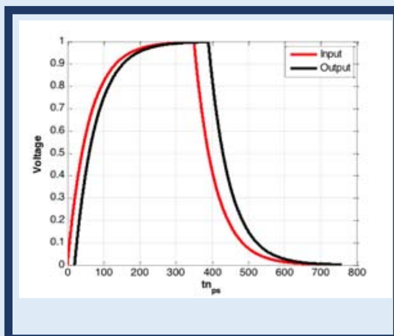
- Single Event Transient
  - SET propagation

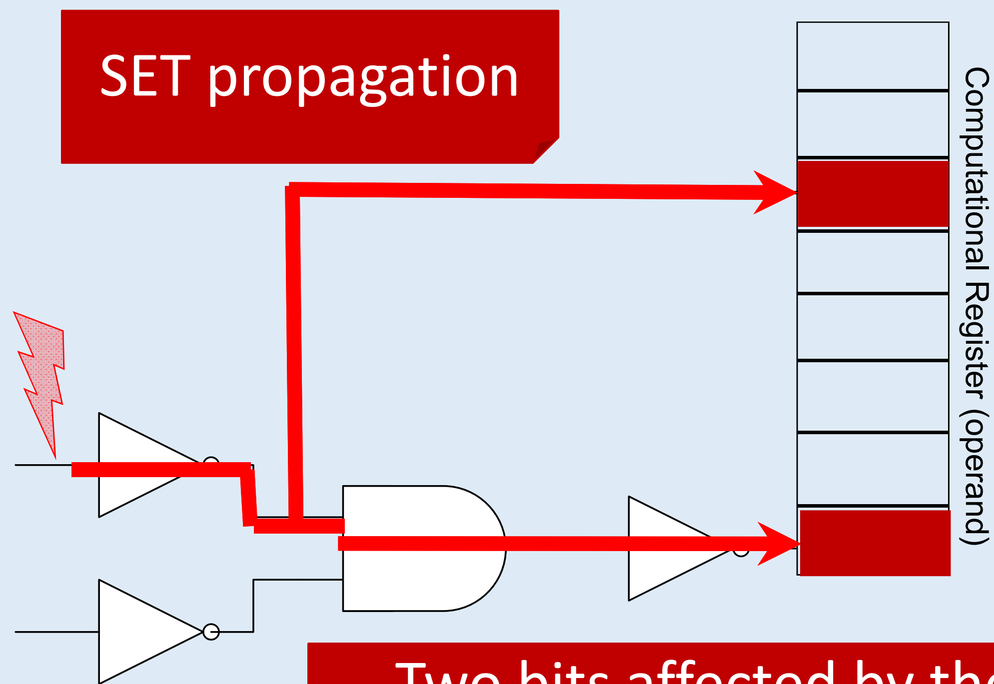




Background

- Single Event Transient
  - Sampled SET



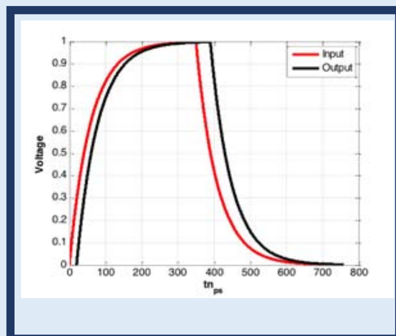


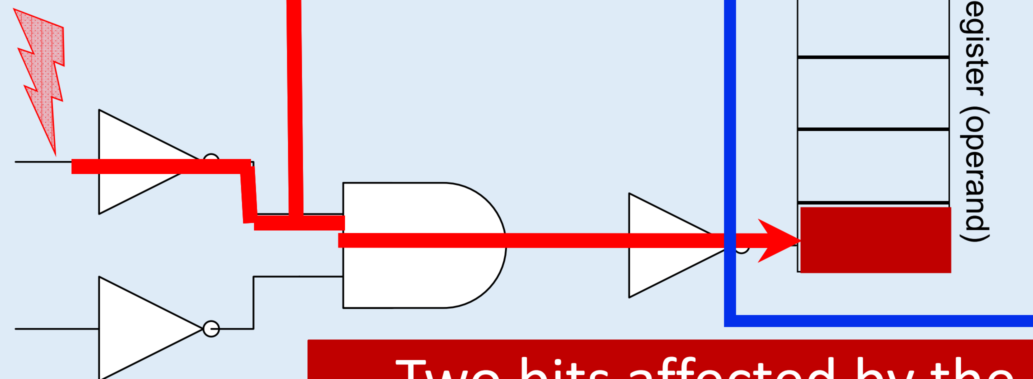
Background

- Single Event Transient
  - Multiple SEUs

Multiple SEUs

SET propagation

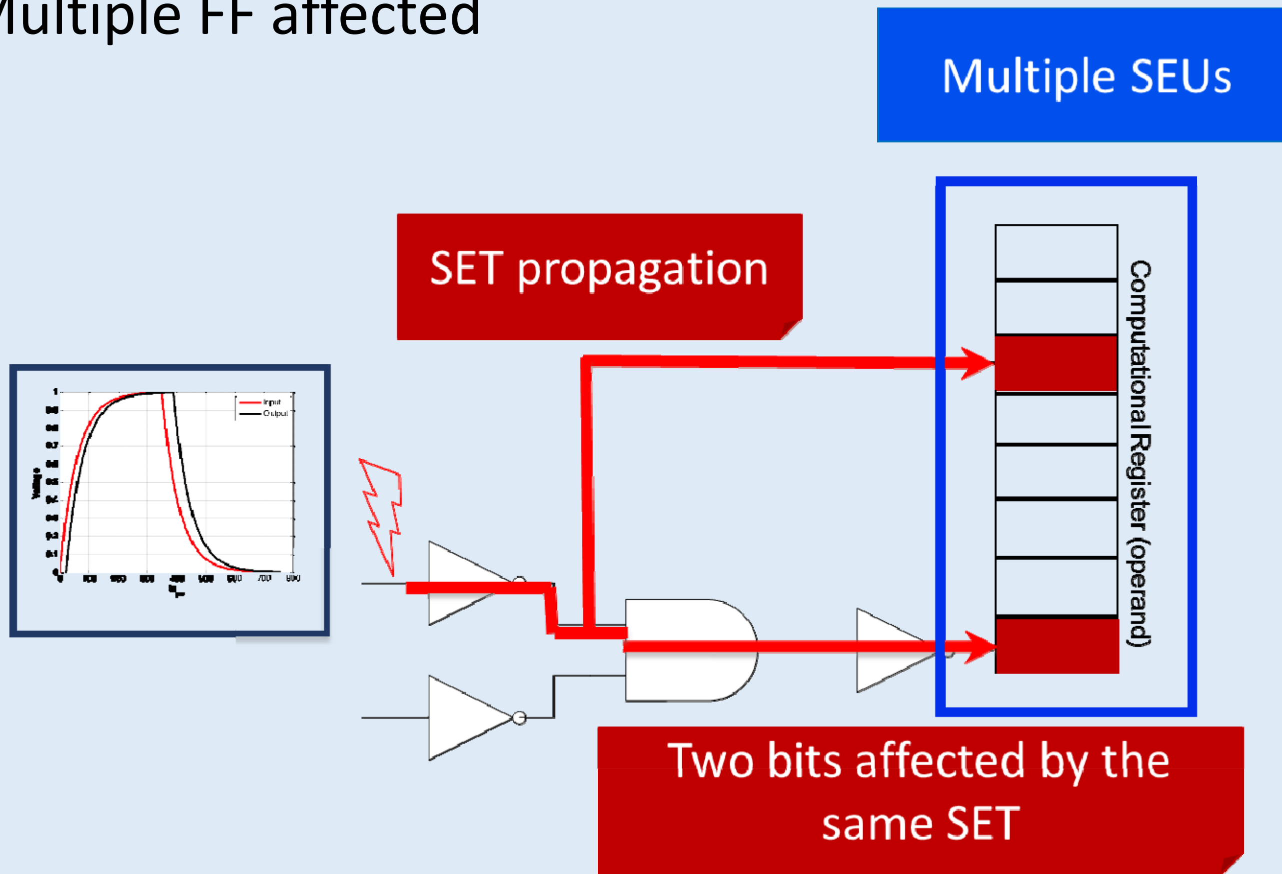




Two bits affected by the same SET

Single Event Transient

- SET main concerns
  - SET basic mechanism: generation and propagation
  - Single FF affected
  - Multiple FF affected

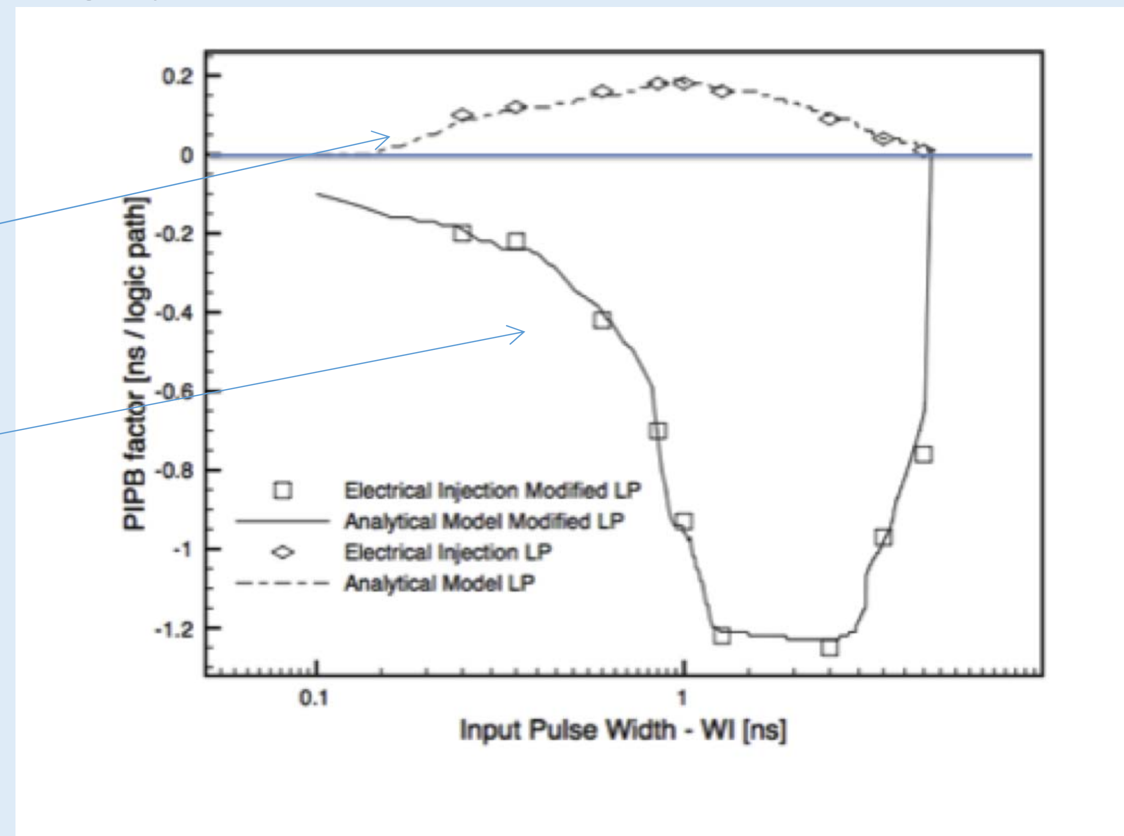


SETs on Microsemi Flash-based FPGAs

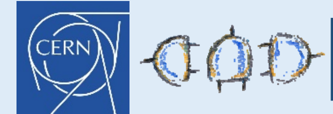
- Measurement of the PIPB factor on modified LP
  - 9 SET pulses ranging from 0.25 ns to 4.50 ns
  - Both SET transition
  - Error deviation ≈ 0.04 ns / logic path.

Non-inverting propagation condition with the same LP delay

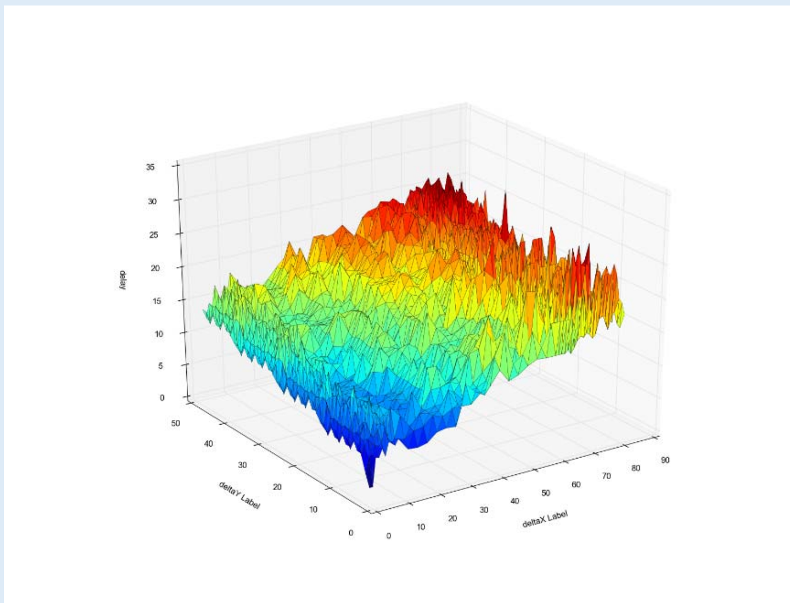
Inverting propagation condition with the same LP delay

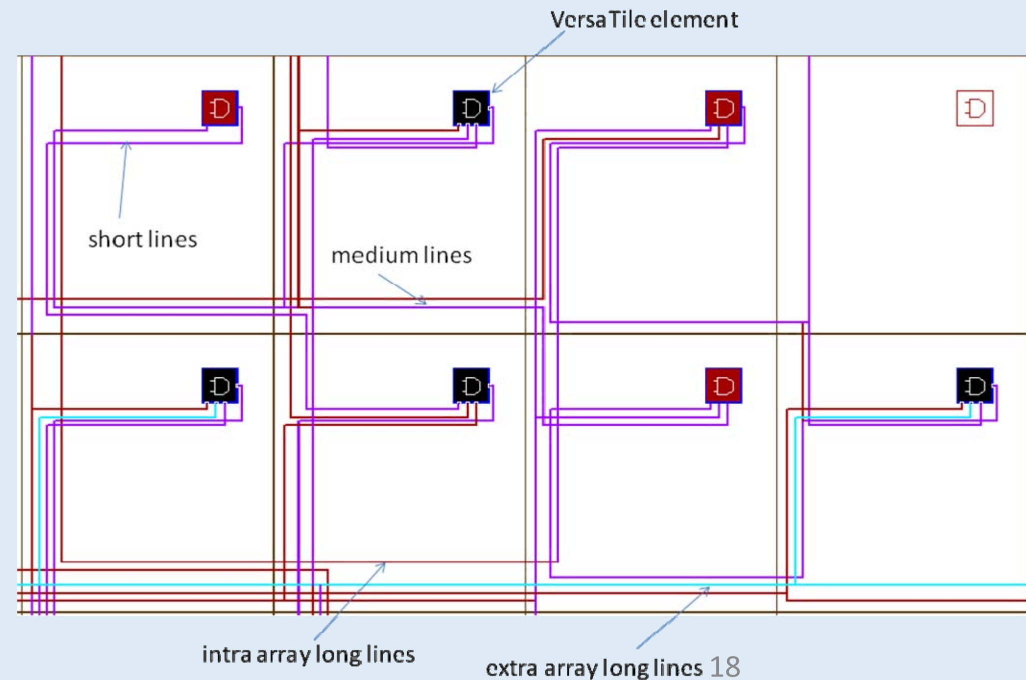


SETs on Microsemi Flash-based FPGAs



- We identified four hierarchical levels of interconnections and correlation to the FG switches:
  - Extra array long lines
  - Intra array long lines
  - Medium lines
  - Short lines





Mitigation and design flow

HDL

Synthesis and Implementation

Export

PDC

AFL

AFL2PDD

PDD

SETA

SET Report

Export Synthesized Netlist (V)

Source V

PDT_MITE

Register SET data

Mitigated V

Final PDC

Synthesis and Implementation

Export

PDC

AFL

AFL2 PDD

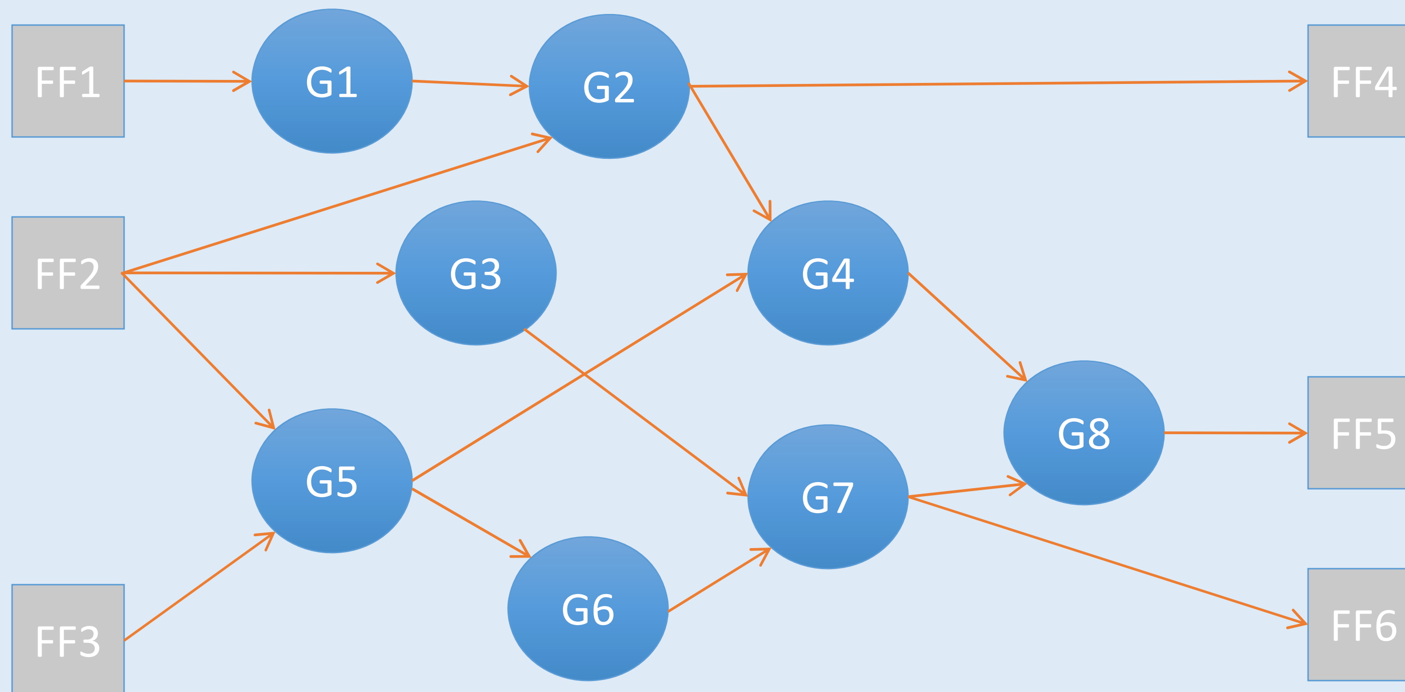
PDD

PDT_PLACE

Final Design

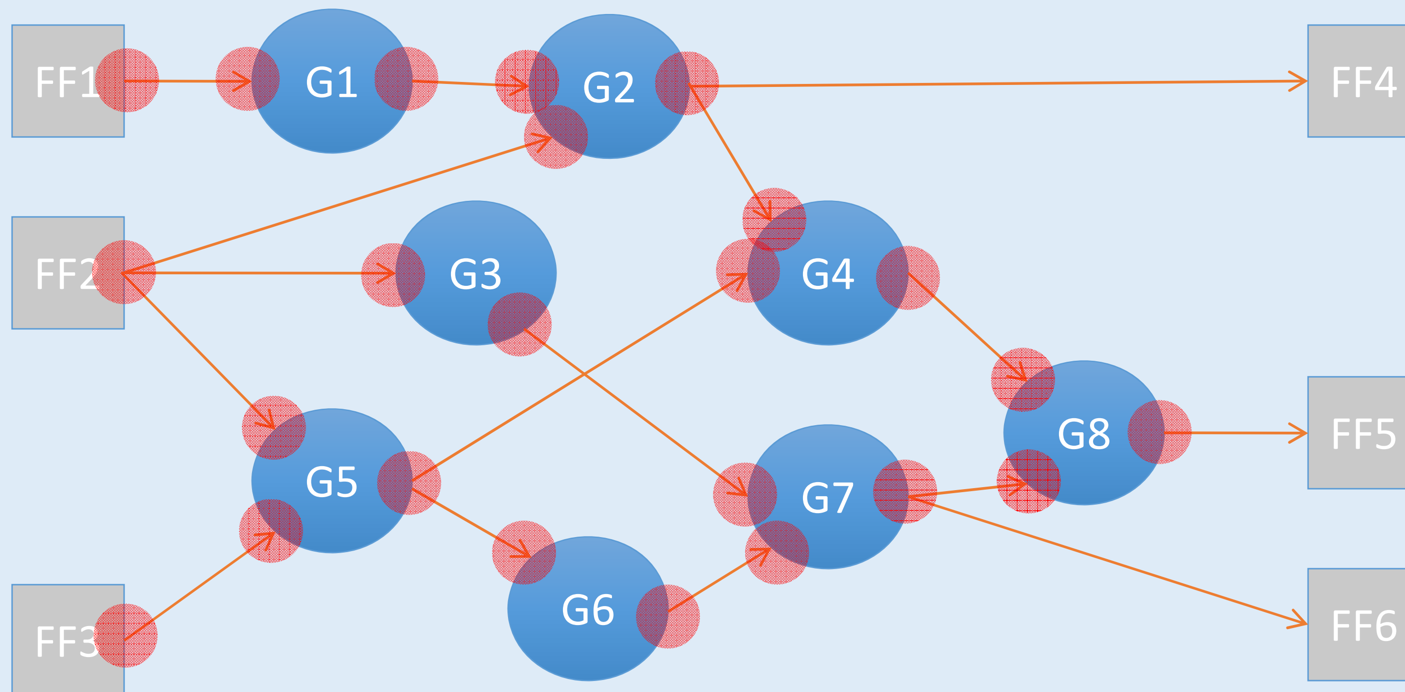
SETA tool

- Sensitive nodes identification



SETA tool

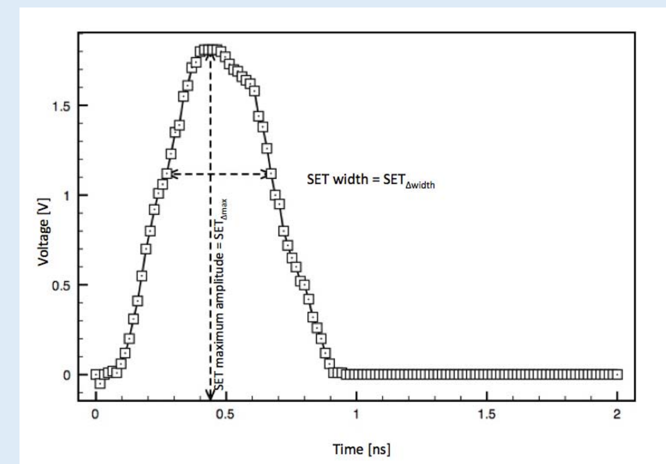
❑ Sensitive nodes identification



SETA tool

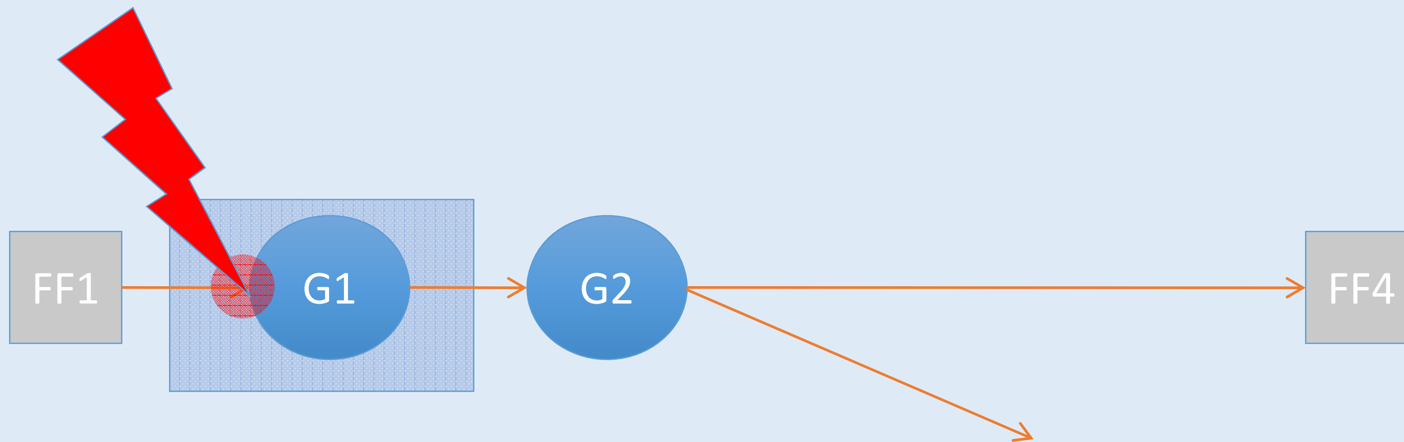
1. Generate the list of SET pulse: SET_{GP}
2. For each generated pulse $p \in (SET_{GP})$
   2. For each sensitive node $i \in (SN)$
   Apply pulse *p* to *i*
   Find destination node $dn \in (SN, i)$
      3. For each *dn*
      Propagate *p* on (*i*, *dn*)

- SET pulse is generated as a voltage spike
  - Maximal voltage amplitude
  - Maximal voltage width
  - Rise and fall DV/DT
  - Defined as 100.000 points: resolution of 1ps
  - Stored in a double float
  - V_IH, V_OL
  - Peak definition
  - SET pulse peak
  - SET pulse length



SETA tool

- The generated voltage array is applied to a selected sensitive node



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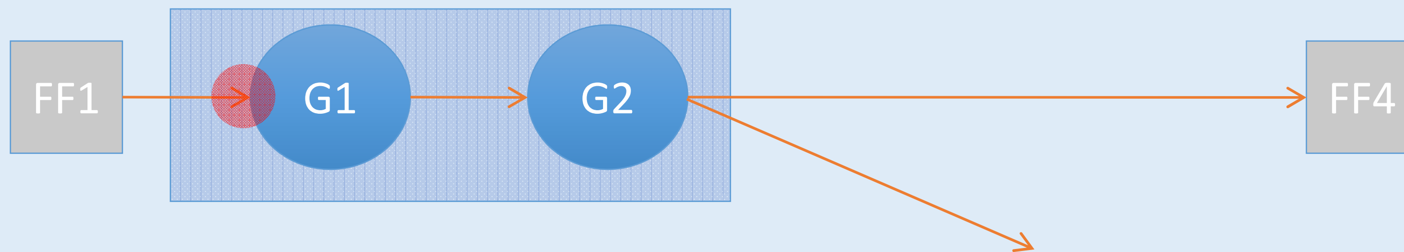

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   Find destination node $dn \in (SN, i)$

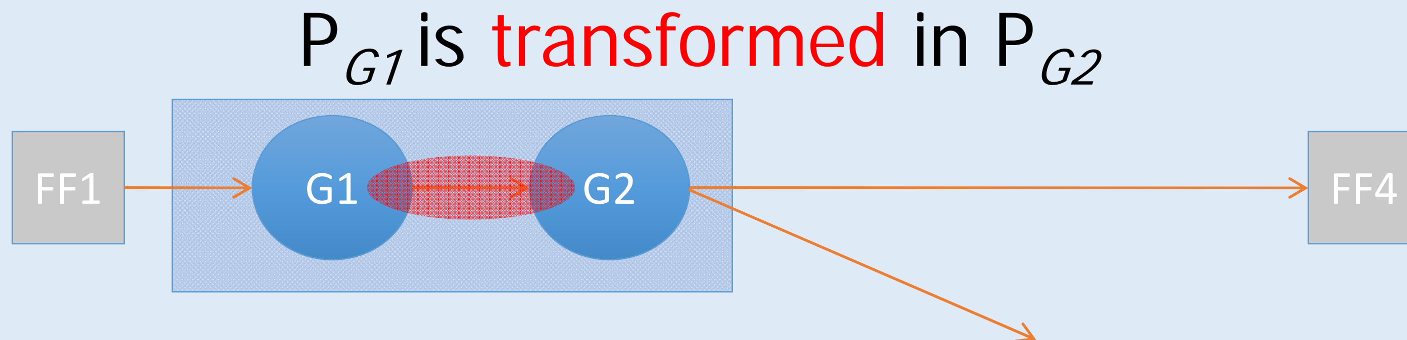
   3. For each dn

   Propagate p on (i, dn)

SETA tool

- The voltage array p is propagated through the logic element G1 to th next destination node
- A new voltage array P_{dn} is generated in the input of the destination node

P_{G1} is transformed in P_{G2}



- Computation of the broadening coefficient
  - Loading PIPB gate figure
  - Calculate the crossing-PIPB for a given couple of gate

SETA tool

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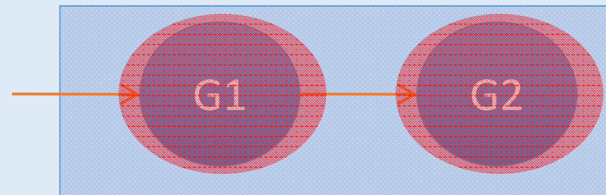
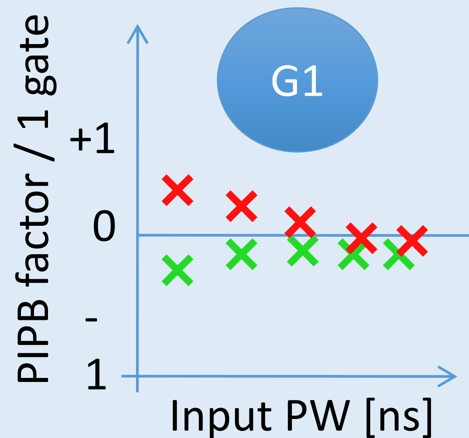
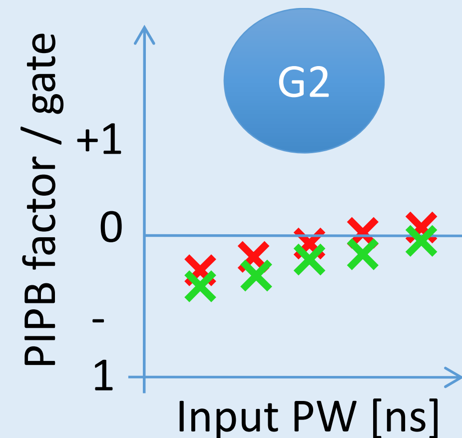
  - Loading PIPB gate figure
  - Calculate the crossing-PIPB for a given couple of gate







SETA tool

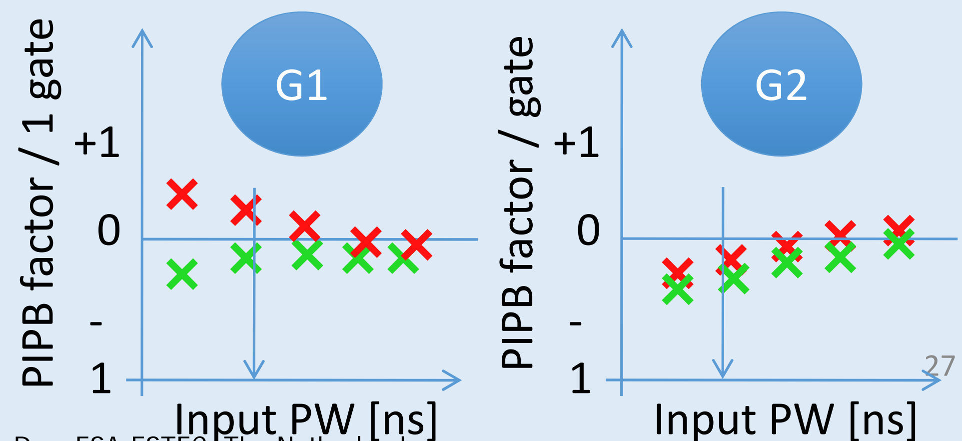
- The crossing-PIPB is calculated on the basis of the following routing parameter
  - τ= RC (sum of all the fan-out and fan-in contributions)
  - Logic gates manhattan distance
  - Size weight associated to destination gates

$$\text{Output Pulse Width} = \text{Input Pulse Width x } K_{broadening}$$

- Given the Source Gate input PW
- Identify the Drain Gate input PW
- Calculate the sum between the best and worst propagation condition PIPBBEST and PIPBWORST of the two gates:

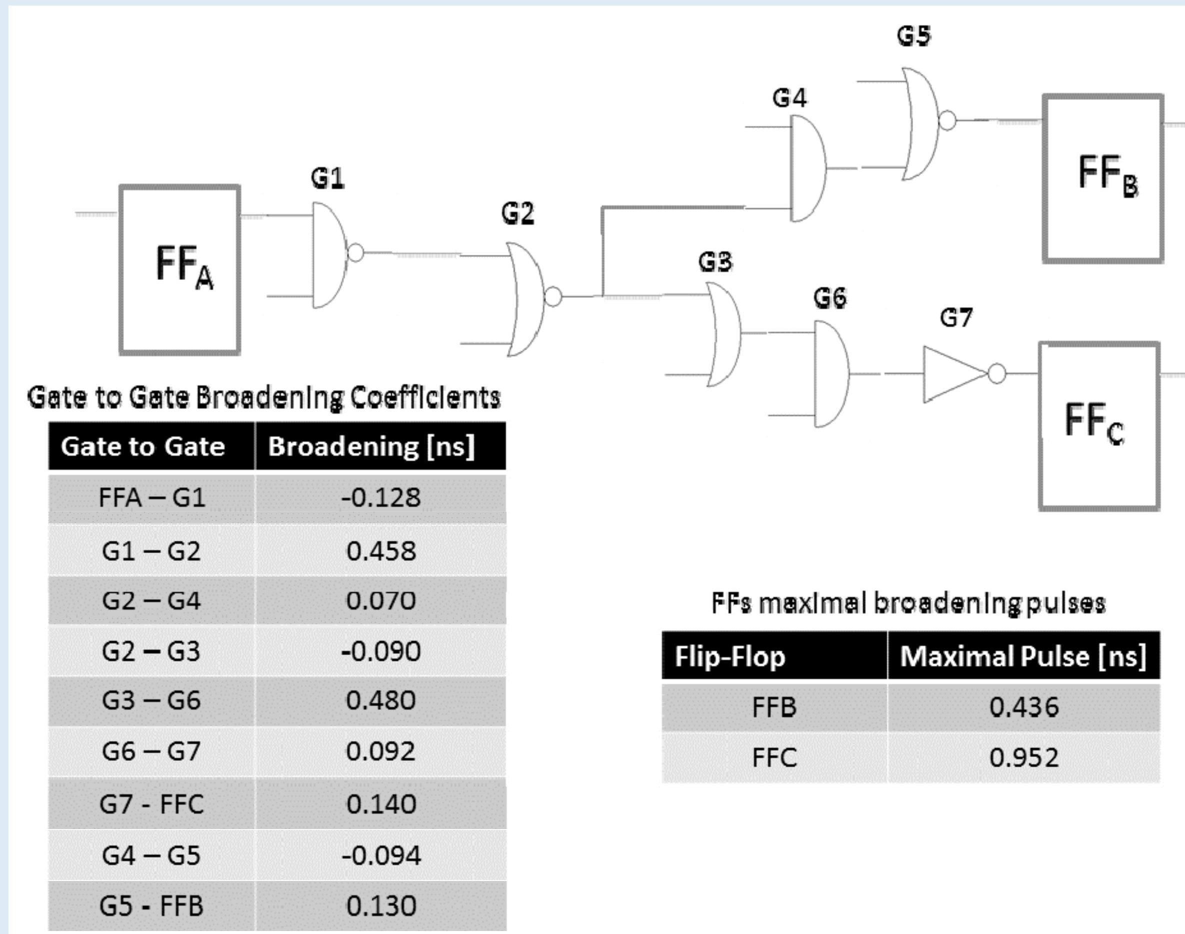
$\Sigma DPBEST = PIPB_{BEST_G1} + PIPB_{BEST_G2}$

$\Sigma DPWORST = PIPB_{WORST_G1} + PIPB_{WORST_G2}$



PDT_MITE

- PDT_MITE modifies a netlist according to the SETA report
  - Each Flip-Flop is classified on the basis of its maximal pulse broadening
  - Propagation of SET pulses between couple of gates



Gate to Gate Broadening Coefficients

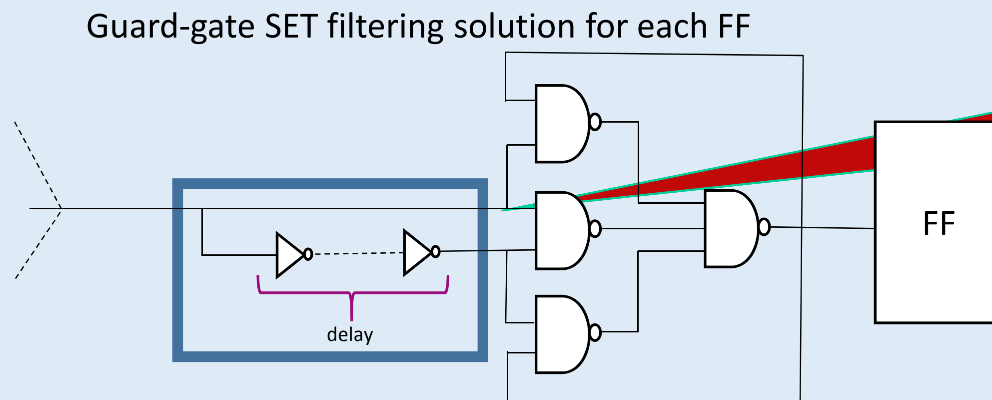
Gate to Gate	Broadening [ns]
FFA – G1	-0.128
G1 – G2	0.458
G2 – G4	0.070
G2 – G3	-0.090
G3 – G6	0.480
G6 – G7	0.092
G7 - FFC	0.140
G4 – G5	-0.094
G5 - FFB	0.130

FFs maximal broadening pulses

Flip-Flop	Maximal Pulse [ns]
FFB	0.436
FFC	0.952

PDT_MITE

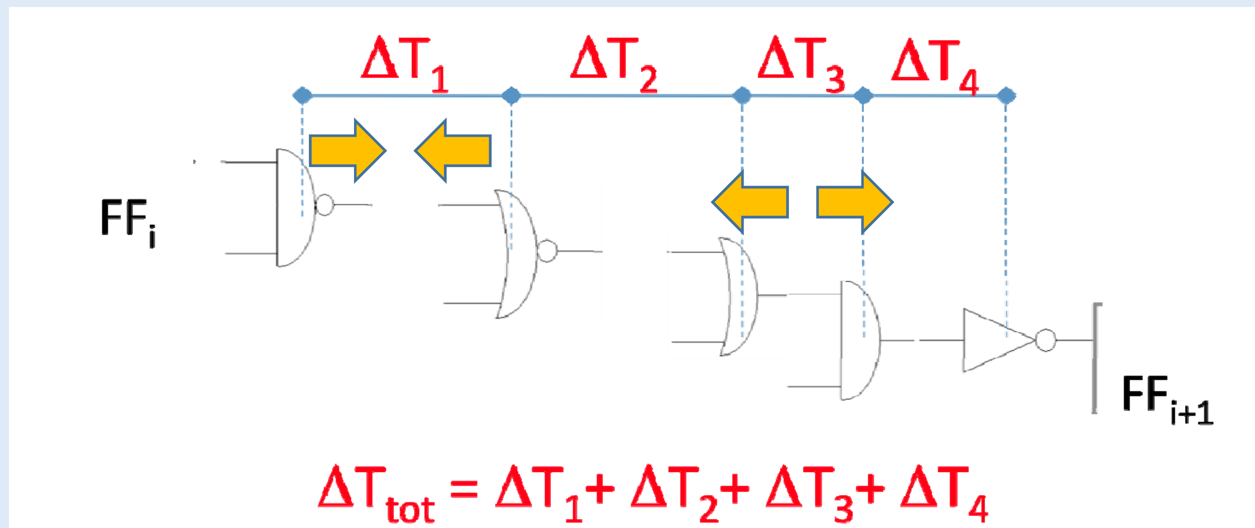
- PDT_MITE inserts a guard gate logic structure on the input of the selected Flip-Flop
- It acts on the critical path individuated by the SET analysis phase
- The overhead of each guard gate structure depends on the maximal pulse broadening



The filtering delay is estimated on the basis of the SET report

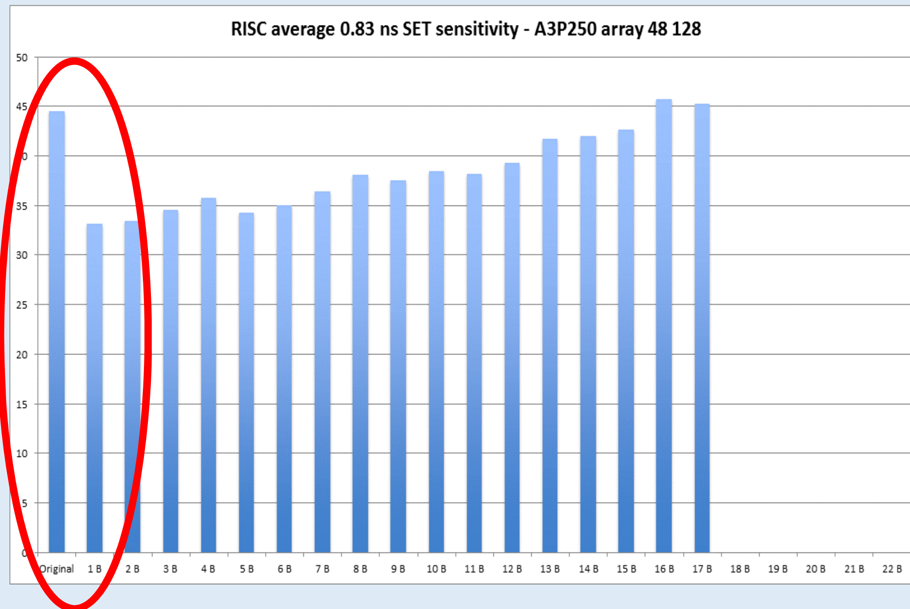
PDD_Place

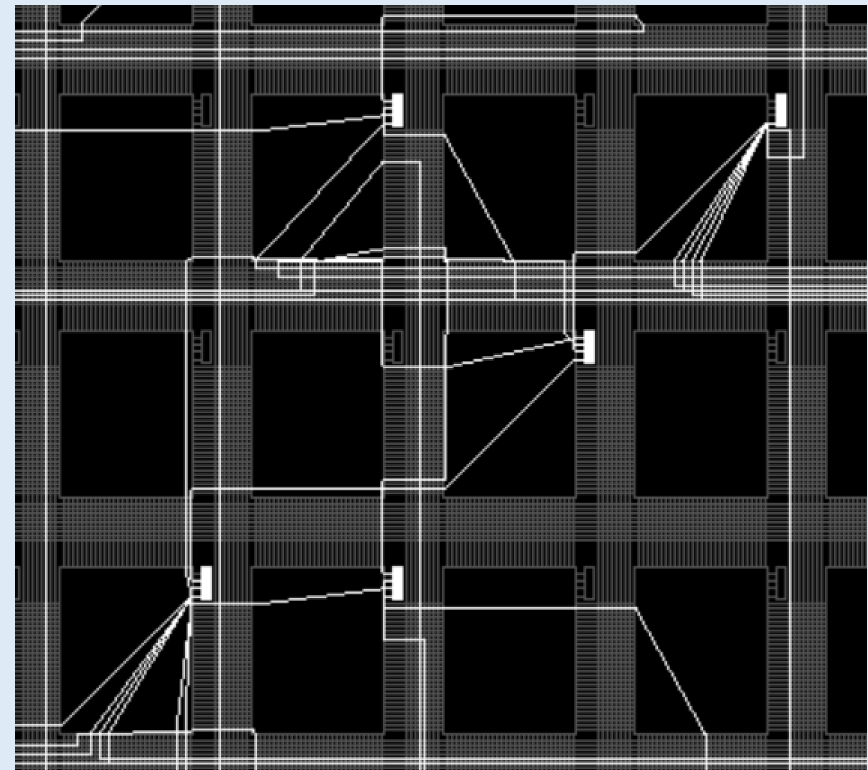
- PDD_Place acts on the critical gate paths modifying the placement position respecting the following rules
  - If a gate G and the next gate G+1 are inverting gates, the placement is perofrmed in the closest position
  - In the other cases the placement is performed in a longer distance



PDD_Place

- The PDD_Place algorithm is based on a FPGA model
  - Ad-hoc FPGA architecture layout
  - Placer algorithm



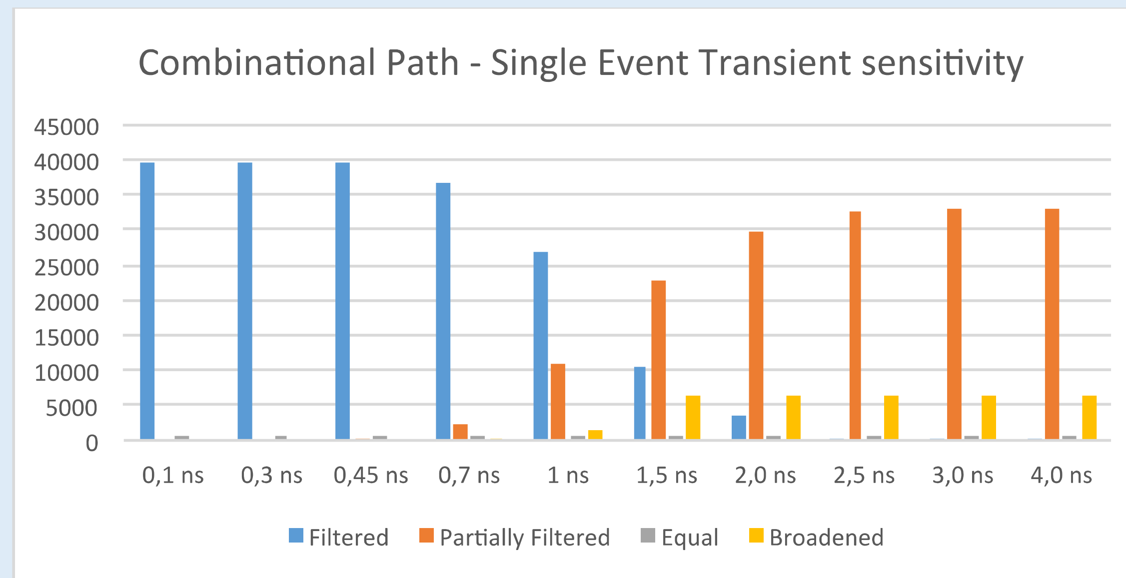


Experimental result

- The analysis and mitigation methods have been applied to the EUCLID space mission project
  - Implemented on Microsemi ProASIC3 A3P3000 Flash-based FPGAs
  - Nominal duration of mission: 6.25 years
  - 12 functional modules with four different clock domain
  - Longest estimated SET width 1.0 ns

Experimental result

- SET overall distribution among combinational path



Experimental result

- Propagation-induced Pulse Broadening coefficient

SET pulse [ns]	PIPB (inj_{width}/out_{width})	Max SET_{width} [ns]
0.10	0	0
0.30	0	0
0.45	0	0
0.70	1.17	0.82
1.00	1.17	1.17
1.50	1.20	1.80
2.00	1.15	2.30
2.50	1.12	2.80
3.00	1.10	3.30
4.00	1.08	4.30

Experimental result

- Netlist TMR v1

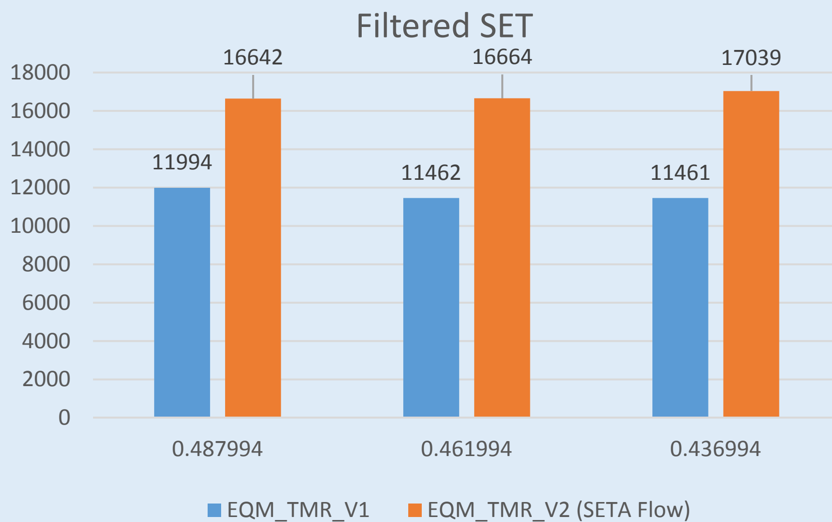
Type	Instances	Core Tiles [#]
Circuit Combinational gates	27,339	27,339
Sequential	17,806	17,806

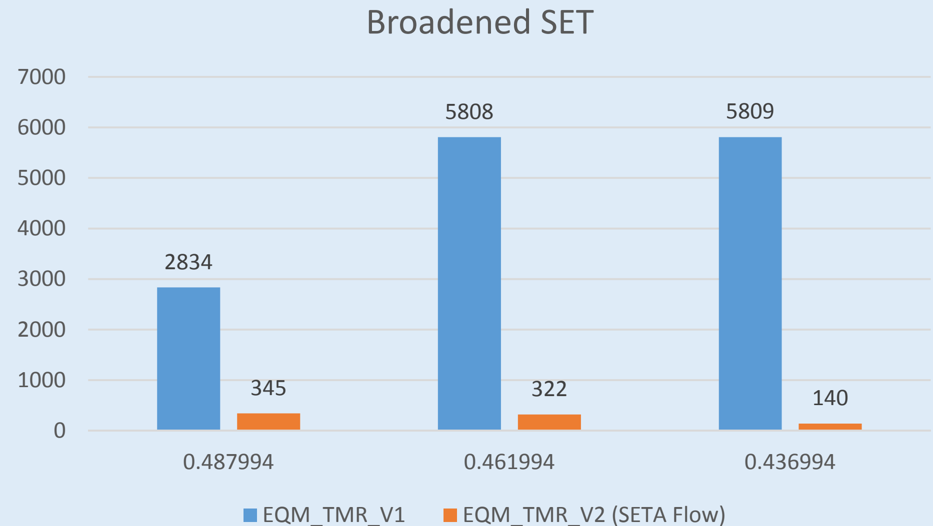
- Netlist TMR v2 (SETA flow)

Type	Instances	Core Tiles [#]
Circuit Combinational gates	27,339	27,339
INVD gates (GG structure)	6,678	6,678
NAND gates (GG structure)	11,778	11,778
Total Combinational gates	45,795	45,795
Sequential	17,806	17,806

Experimental result

Reference Name	Netlist TMR v1		Netlist TMR v2 PDT	
	Period [ns]	Frequency [MHz]	Period [ns]	Frequency [MHz]
CLK_60M	12.097	82.665	14.308	69.891
CLK_20M	30.156	33.161	34.387	29.081
SPW_CTRL0/space_wire1/c_rx/clk_rx	11.177	89.469	11.008	90.843
SPW_CTRL1/space_wire1/c_rx/clk_rx	13.437	74.421	12.207	81.920
clk_60M_buff	12.097	82.665	14.308	69.891
clk_30M	28.022	35.686	32.755	30.530





Cross-section comparison

- Global error rate calculation

Module	Exposed Area EQM_TMR_V1 [Cross-section]	[Cross-se[illegible]
SPW_CTRL_1	1,14E-06	1,37[illegible]
SPW_CTRL_0	1,33E-06	1,60E-[illegible]
UART_TMTC	6,49E-06	7,79E-06
DMA_B_0	6,54E-06	7,85E-06
[illegible]IDECAR_D	5,66E-06	6,79E-06
SD_CTRL	1,22E-06	1,46E-06
PROCES_B_0	2,23E-06	2,68E-06
SIDECAR_B	2,35E-06	2,82E-06
CONTROL_B	1,06E-07	1,27E-07
AHB_0	8,15E-09	9,78E-09
APB_0	9,32E-09	1,12E-08
CLOCK_H	8,28E-09	9,94E-09

Original LET obtained from CREME

Reference LET values are considered
SET source saturates at 0.7 ns

$\varepsilon_{absolute}$ = *Max_Peak_Integer_Flux x Plain_Circuit_CS x Tecnology_CS x #SET_events x (SET_length / Minimum Circuit Working Period)*

- SEU Rate comparison

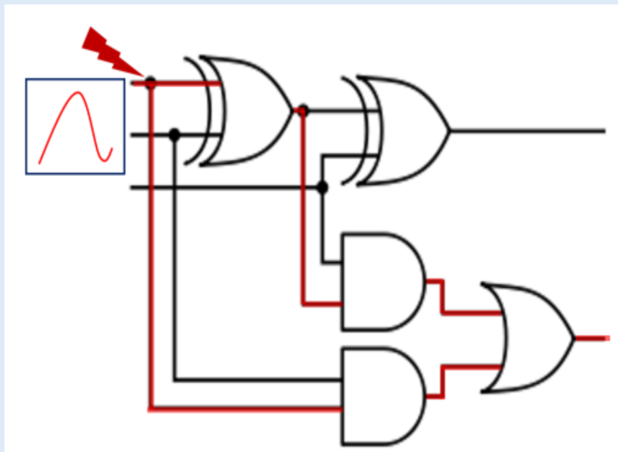
	Max Peak [ε_{SEU_RATE}]	Worst Day [ε_{SEU_RATE}]	Worst Week [ε_{SEU_RATE}]	Nominal [ε_{SEU_RATE}]
EQM_TMR_V1	2.79E-1	3.35E-2	2.51E-2	1.40E-7
EQM_TMR_V2	3.40E-2	4.08E-3	3.06E-3	1.70E-8

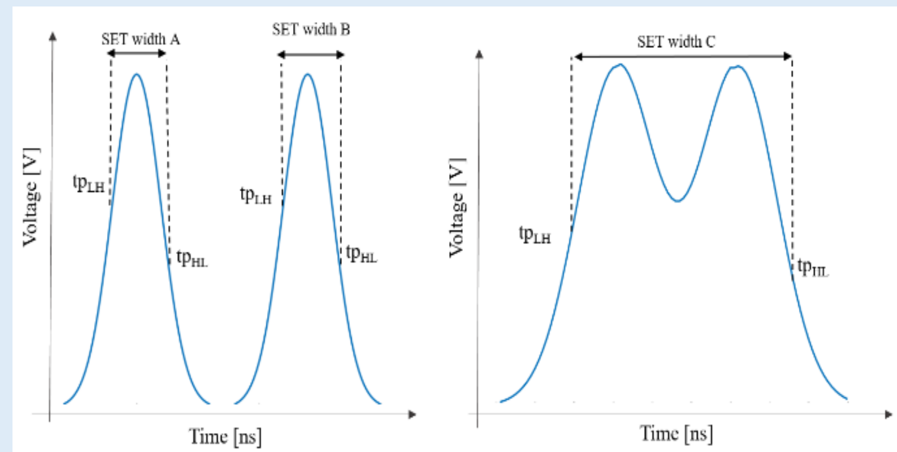
Conclusions

- An extended characterization method for the SET phenomenon has been developed
- The method has been applied on a realistic space-oriented SoC design (ESA-EUCLID space mission)
- Mitigation shows a reduction of three orders of magnitude of the relevant SET sensitivity
- Limited area overhead (less than 20%).

Future works

- Execution of radiation test experiments with proton or heavy-ions
- Extension of the SET model under analysis
  - Characterization of the Convergence-SET (C-SET)





- Study of the method applicability to ASIC or regular fabric technology

Thank you

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