TEC-ED & TEC-SW Final Presentation Days
May 2017

Activity Title:
Development of new place and Route Tools to improve set mitigation in ACTEL ProASIC FPGA – SETA tool improvement and application to Euclid Project
Presentation: SETA tool update: SETs in Flash-based FPGAs

Budget: 20 K€	Program Line: Euclid Development – Payload, CCN2 4000105142
Duration: 20 months	Kick Off Date: 1/April/2015
TO: David Merodio Codinachs (TEC-EDM)	
Prime: Politecnico di Torino (IT) Design provided by OHB-I (IT) (former CGS)	

CAD group

Main Objectives:
The Single Event Transient Analysis (SETA) tool performs analysis of SETs impact on circuits mapped on Flash-based ProASIC FPGAs. The main objectives of the CCN2 are:

- Preliminary analysis of the OHB-I design
- Implementation of new features in the tool (like automatic insertion of Guarding Gates)
- Perform the final analysis and mitigation of the OHB-I design