SETA Tool Update

Flash-based FPGAs are characterized by the main concern of radiation-induced voltage glitches or SETs in the combinational logic. Transient pulses can be sampled by a storage element and can propagate through the circuit up to the outputs and leading to an error. The presentation will focus on the methods for characterization, analysis and mitigation of Single Event Transients (SETs) on Flash-based FPGAs applied to the EUCLID project. The presentation will include a complete implementation flow including sensitivity analysis, fault tolerant mapping and fault tolerance-oriented place and route for the effective design of SET tolerant circuits on Flash-based FPGAs. The obtained results show an improvement of the total filtering capability of around 43 times with respect to the original netlist without affecting the timing constraints of the circuit.