HPDP: Architecture and Back-end Flow

The European Space Agency has initiated the development of the HPDP chip to address the need for a flexible and re-programmable high performance data processor. It is being implemented in the STM 65nm radiation hardened technology. In this presentation, the architecture of the HPDP device is presented in details. It is also shown the adopted back-end design flow for the physical implementation of the device with emphasis to synthesis, static timing analysis, formal equivalence check, place and route and sign-off checks