GSRIO – Serial RapidIO Logical Layer Ip Core

Kostas Marinis

09/05/2017

CONTRACT DETAILS

Budget + Program: GSTP - 300k

Planned Duration: 18

Actual Duration: 18 +10 months (closed in April 2017).

The main reasons for the delay were the additional complexity of developing and validating a SRIO PHY, along with the Logical layer. It has been proposed to use a 3rd party SRIO PHY IP core, and focus the development work on the Logical layer, and final integration with the PHY. An SRIO PHY by IDT (Canadian based) was selected, but the contractual aspects for the license agreement between CG-IDT, and also the necessary adaptations and integration of the PHY IP core, resulted in the additional delay in the activity

T.O.: Kostas Marinis

TRL initial = 2, final = 4

Contractors: Cobham Gaisler (prime), RUAG SE (sub).

CONTRACT DETAILS

- **Scope of the work**:

The architecture of new OBCs for high-performance platforms requires the use of a fast and reliable IPL interface between the main processor and other complex ICs as co-processors or enhanced memory controllers. The use of traditional low speed serial communication channels (e.g. RS422/485) is not sufficient in terms of speed and reliability, whilst parallel buses (like PCI) have the disadvantage of large pin counts. A previous trade-off analysis of the various possible options of this interprocessor link (IPL) interface has already been performed in the frame of the GSTP activity “Single Board Computer Core – Phase 1” (GSTP, RUAG SE). The conclusion from that study was that the most suitable candidate interface for such applications (IPL) is RapidIO.

The objective of this activity was to develop and validate a Serial RapidIO IP core implementing the SRIO Logical and Physical layers of the RapidIO specification v2.2, that can be used to implement SRIO endpoints.