GRSRIO - Serial RapidIO Logical Layer IP Core
Flexible DMA Engine for Serial RapidIO Endpoints

The Serial RapidIO Logical Layer IP core (GRSRIO) provides a link between the AMBA on-chip bus and a single-port Serial RapidIO endpoint. The IP core comprises a DMA engine that handles data transfers to/from memory via its generic bus master interface. It implements the full I/O Logical Specification and the Message Passing Logical Specification Version 2.2. The following I/O operations are supported: Read, Write, Write-with-response,, Streaming-Write, Atomic Transactions (set, clear, increment, decrement, swap, compare-and-swap, test-and-swap), and Maintenance.

The GRSRIO core offers an extensive two-level interrupt system and can easily be adapted to different SRIO end-point implementations and on-chip buses. The default AMBA DMA interface can be configured in terms of data path width and burst length.

The GRSRIO core is verified in simulation (with full code coverage) and validated in hardware. It comes with a top-level wrapper for a simple integration into Cobham Gaisler's GRLIB IP library, although stand-alone usage is supported as well. Extensive documentation including a user's manual and a verification report is available. The core was validated on a flash-based RTG4 and an SRAM-based Virtex-7 FPGA using a custom-built validation software that is executed by a LEON3 microprocessor.