SHyLoC: CCSDS Lossless Compression IP-Cores for Space Applications

High data rate multispectral and hyperspectral sensors and the limitations of the on-board storage and bandwidth make on-board data reduction mandatory. The CCSDS-123 and CCSDS-121 lossless standard for satellite data compression have demonstrated to provide a good compromise between compression efficiency and low-computational complexity that makes them very attractive to be integrated as part of many space missions in the near future. Currently, reference software implementations of the CCSDS-123 and CCSDS-121 are available. However, to endorse on-board compression presence in future space missions, it is essential to provide also hardware descriptions that can be efficiently mapped to the FPGA and ASIC technologies currently available on satellites.

In this work, commissioned by ESA ITT AO/1-8032/14/NL/AK, we have designed two reusable soft IP cores compliant with the CCSDS-123 and CCSDS-121, that can work as independent compressors as well as jointly (with the CCSDS-121 performing the entropy coding stage of the CCSDS-123). They are technology independent and fully parametrizable, in such a way that the users can adjust the parameters to find the compromise between complexity and compression efficiency that better meets the mission demands. Besides parametrization, the IP-cores also offer the possibility of selecting the different user-defined configuration values allowed by the CCSDS standards at runtime using standard AHB interfaces, allowing for their straightforward integration in an embedded system with other components such as a LEON processor.

We present descriptions of the IP-cores hardware architectures, which have been optimized in order to achieve a high throughput and keep complexity as low as possible. In particular, for the CCSDS-123 IP core, three different highly-optimized hardware architectures have been devised, one for each of the possible orders in which the hyperspectral image can be stored (BSQ, BIP and BIL), due to the different data dependencies and hardware resources requirements that each of them impose. As a result, each of the proposed architectures provides the highest possible throughput with the lowest possible complexity for each of the compression orders.

The outcome of this work is presented as synthesis results of the IP-cores with a relevant selection of configuration parameters on one-time reconfigurable FGPAs from Microsemi and commercial FPGAs from Xilinx and DARE 180nm ASIC technology; providing metrics such as FPGA occupancy, area, throughput and power consumption. Additionally, we present the validation of the IP-cores capabilities with the use of a COTS FPGA board that includes a Virtex-6 LX240T, and an EGSE based on the iSAFT Simulator that is connected to the board through a SpW link.