TEC-ED & TEC-SW Final Presentation Days
May 2017

Activity Title: SHyLoC: CCSDS Lossless Compression IP-COREs for Space applications	
Budget: 250 K€	Program Line: TRP EXPRO+ ESA AO/1-8032/14/NL/AK
Duration: 30 months	Kick Off Date: 3/Feb/2015
TO: David Merodio Codinachs (TEC-EDM) Handed over from Luca Fossati (currently TEC-EDD) With support from Raffaele Vitulli (TEC-EDP)	
Prime: Institute for Applied Microelectronics (IUMA) from the University of Las Palmas de Gran Canaria (ULPGC) (ES) Subcontractors: Teletel S.A. (GR) and Thales Alenia Space (ES)	

Main Objectives:

Design, verify and validate two lossless compression IP cores:

- Compliant with CCSDS 121 and CCSDS 123 standards
- Reusable IP cores to be included in the ESA's repository
- Compatible with technologies that are targeted by the space industry: one-time programmable FPGAs, re-configurable FPGAs and ASIC technology