SPACEWIRE NODE INTERFACE IP CORE

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CONTRACT DETAILS

Budget + Program: TRP STRIN
Planned Duration: 18 months
Actual Duration: 24 months
T.O.: Luca Fossati (TEC-EDD), Jorgen Ilstad (TEC-EDD)
Technical Support: David Jameux (TEC-EDP), Kostas Marinis (TEC-EDD) – THANKS TO BOTH

SCOPE OF THE WORK:

The objective of this activity is to design, develop and validate a configurable SpW node IP core supporting the following protocols and standards:

ECSS-E-ST-50-12C, SpaceWire links Nodes and Routers
ECSS-E-ST-50-51C, SpaceWire Protocol Identification
ECSS-E-ST-50-52C, SpaceWire - Remote Memory Access Protocol (target and initiator)
ECSS-E-ST-50-53C, SpaceWire - CCSDS Packet Transfer Protocol
SpaceWire – Time Distribution Protocol
SpaceWire – Plug and Play (basic subset)
SpaceWire – Deterministic Transfer Protocol (target only)

SpaceWire node interface IP core

Contractor(s): TELETEL SA (GR) **Sub-Contractors : ADS (FR), TAS (FR)**				**ESA Budget:**	**250 k€**
				TRP T701-305ED	
TRL	**Initial: 2**	**Current: 3**	**YoC: 2016**	**TO: L.Fossati, J. Ilstad (TEC-EDD)**	

Background and justification: The various SpaceWire IP's offered by ESA's IP core service are widely used in many ESA projects and typically implemented in rad-hard FPGAs.
Other important functions of a SpaceWire interface like time counter, configuration port and hardware support for protocols have still to be designed by the user.
To be developed in the frame of the activity, is an easily configurable SpW Node IP core that reduces the need for in-depth knowledge of SpaceWire protocols in order to implement required functions in a standard compliant way.

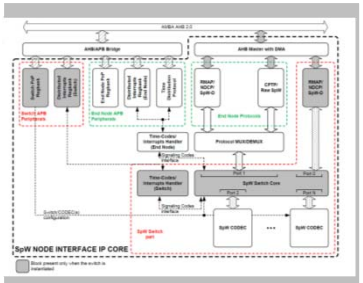
Objective(s): To develop a **easily configurable** Intellectual Property core for a complete SpaceWire node interface in order to facilitate SpW node implementation in ESA projects.

Achievements and status:
The various protocol engines have been implemented and proved functional. It is a configurable SpaceWire node IP core, **which integrates a number of existing IP cores** like the **SpaceWire codec**, **Remote Access Memory Protocol (RMAP) IP core**, **SpaceWire-D (target)** and **Network Discovery Protocol support**, **SpaceWire switch**; Parameters like the number of SpaceWire links, the level of support for the different protocols in hardware and the type of on chip interface are easily configurable for every instantiation of this IP core.

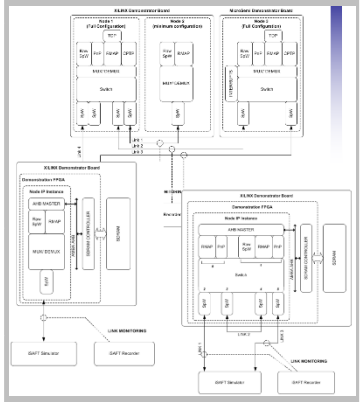
Benefits: Thanks to the development of the highly configurable IP core, tailor-made SpW node implementations in e.g. payload instrument interface, is now possible.

Next steps: to perform a complete code coverage verification of the IP-core and to optimize the design to require less FPGA resources.

Target TRL: 5
Date: ?



SpW Node IP core block diagram



Validation Set-up Example