ARQUIMEA

Passion for Technology

Cosmic Vision Technology Test Vehicle

Design and evaluation activities

08/05/2017

TEC-ED & TEC-SW Final presentation Days 2017

Agenda

- Introduction
- Objectives
- Programme of work
- Main results
- Conclusions

Introduction (1) – The projects

- Two parallel projects will be presented:
  - 4000101556/10/NL/AF: "Front-end readout ASIC technology study and development test vehicles for front-end readout ASICs" (also referred to as Cosmic Vision MF as it evaluates the technology for frequencies up to 10MHz)
  - 4000101621/10/NL/AF "Radiation Tolerant analogue/mixed signal technology survey and test vehicle design" (also known as Cosmic Vision HF as it explores the use of the technology for instrumentation applications for signal frequencies above 10MHz)
- They will be referred as Cosmic Vision Project in the rest of the presentation.

Introduction (2) – The projects

- The projects were conceived in the frame of ESA's Cosmic Vision programme related to the interplanetary mission to Jupiter named Juice.
- In the radiation environment envisaged for that mission, the electronic equipment would be required to withstand up to 300krad of Total Ionization Dose.
- The availability of high performance components that could cope with that requirement was low or non-existent and hence ESA decided to initiate two TRP activities to create radiation tolerant high-performance mixed-signal components for instrumentation.

Introduction (3) – Side or related projects

- The following projects will be mentioned in the presentation as well since they had interactions with the Cosmic Vision project:
  - 4000111457/14/NL/KML: ESA contract with SARL TRAD “Radiation Characterization of Front-End readout ASIC”(also referred to as Radiation Cosmic Vision HF)
  - 4000109670/14/NL/HB: ESTEC contract with Thales Alenia Space España “Scalable Sensor Data Processor”” (also referred as SSDP)

Introduction (4) – The team

- Integration, common blocks design and test

- ADC and DAC MF design

- ADC and DAC HF design

- LNA and PA (MF & HF) design

- Digital design

Introduction (5) - Main subcontractors

- Digital backend, fabrication and package services

- Filter design (MF and HF)

- HF electrical validation

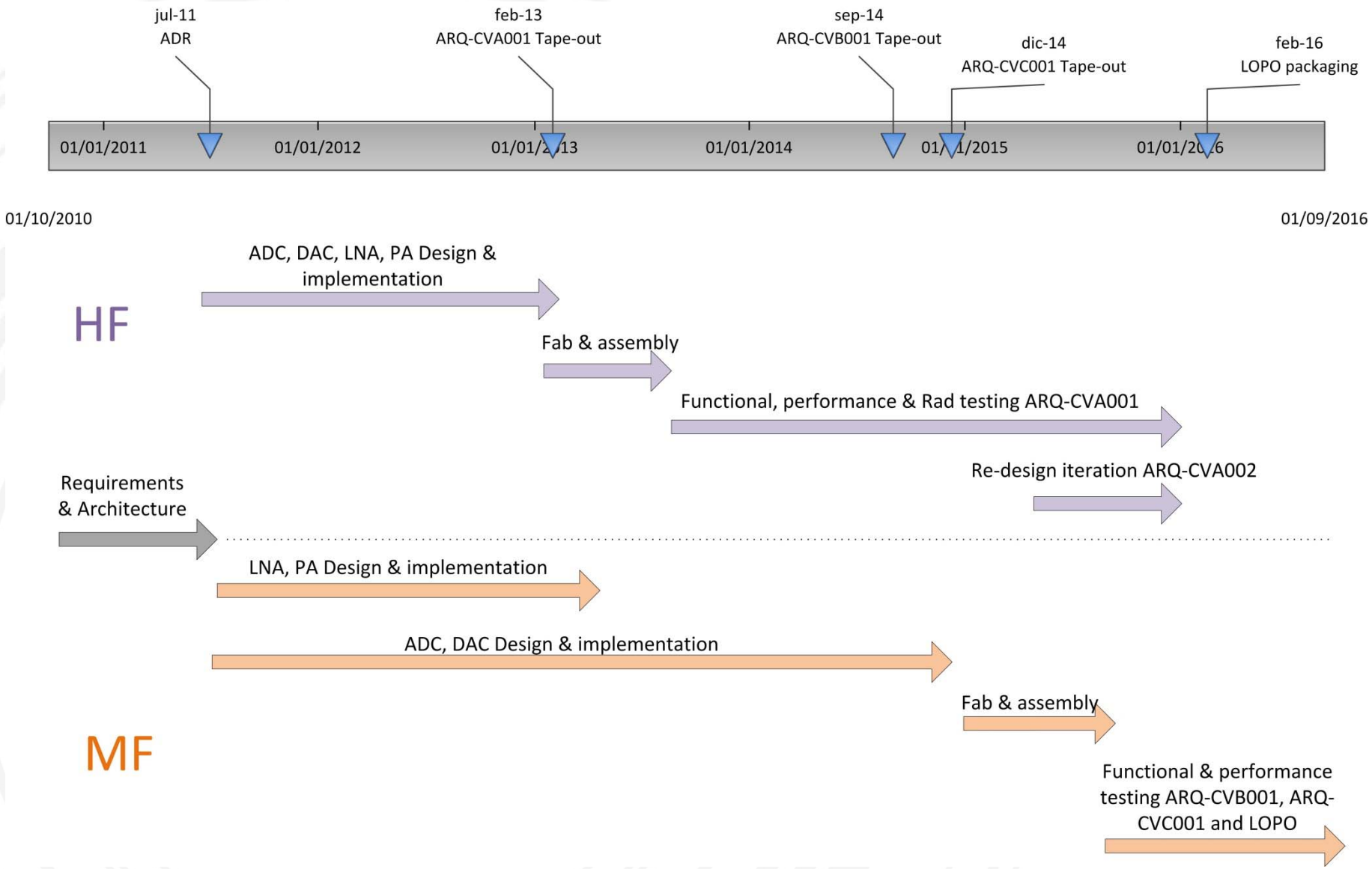
Objectives

- The main objective was the evaluation of the radiation tolerant technology for the implementation of high performance instrumentation IP blocks and provide test vehicles to prove the concept.
- Two frequency ranges of operation were selected:
  - Up to 10 MHz (referred as MF)
  - Above 10 MHz (referred as HF)
- The high performance IP blocks chosen were: ADC, DAC, LNA and PA, for both MF and HF operation.
- All IPs targeted state of the art performance, that is one of the main reasons why this activity was conceived in collaboration with academia.
- Also the mixed signal flow of the selected technology was to be investigated and proved.

Programme of Work (1) - Overall timeline

- The activity was conceived to last 24 months, the evolution of the project was such that it finally took 72 months.
- The state of the art performance was the main driver for this extension both at the design stage and the testing stage
- Several CCNs were signed to cope with the project changes
- A great amount of hours from the project team and ESA were spent to come to a successful project conclusion

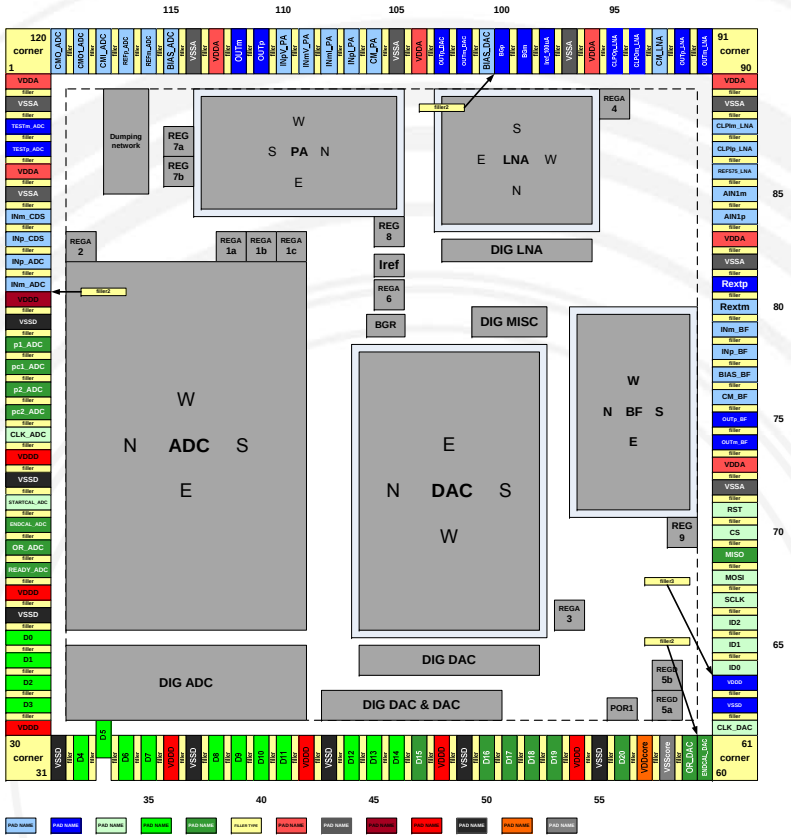
Programme of Work (2) - Summary



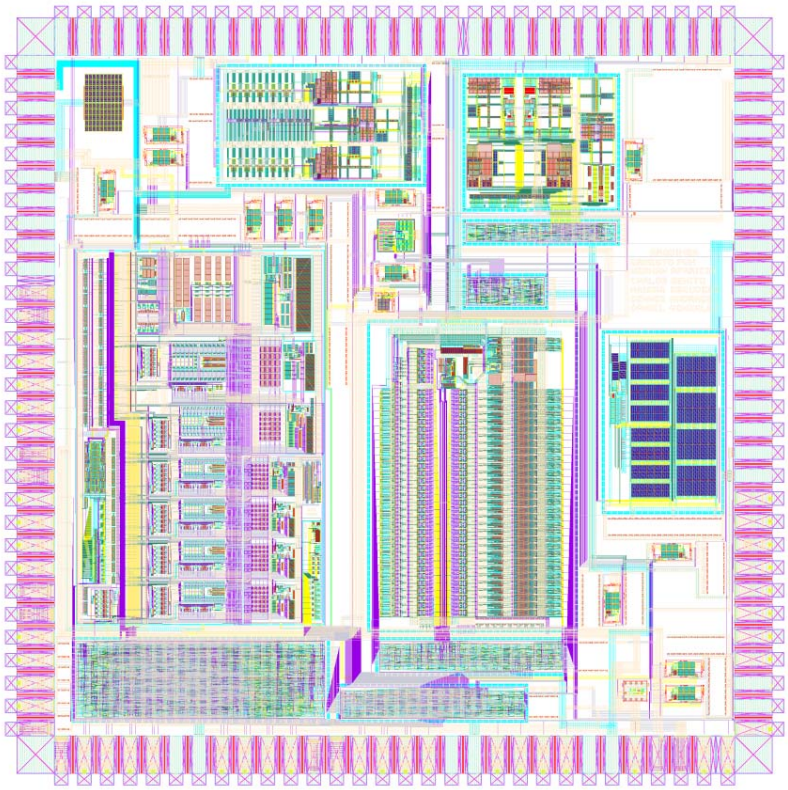
Programme of Work (3) – Design and fabrication phases

- The following ASICs were finally implemented:
  - ARQ-CVA001: HF ADC, LNA, PA, DAC, BF and common blocks
  - ARQ-CVB001: MF ADC (four $\sum\Delta$ modulators)
  - ARQ-CVC001: MF LNA, PA, DAC, BF and common blocks.
- An additional ASIC was packaged in the frame of the project that contained only the MF LLSB modulator (LOPO ASIC)
- The DARE mixed-signal flow required a complex interaction which was cleared along the way.
- Most of the radiation mitigation techniques were applied at layout level.

Programme of Work (4) – Design and fabrication phases

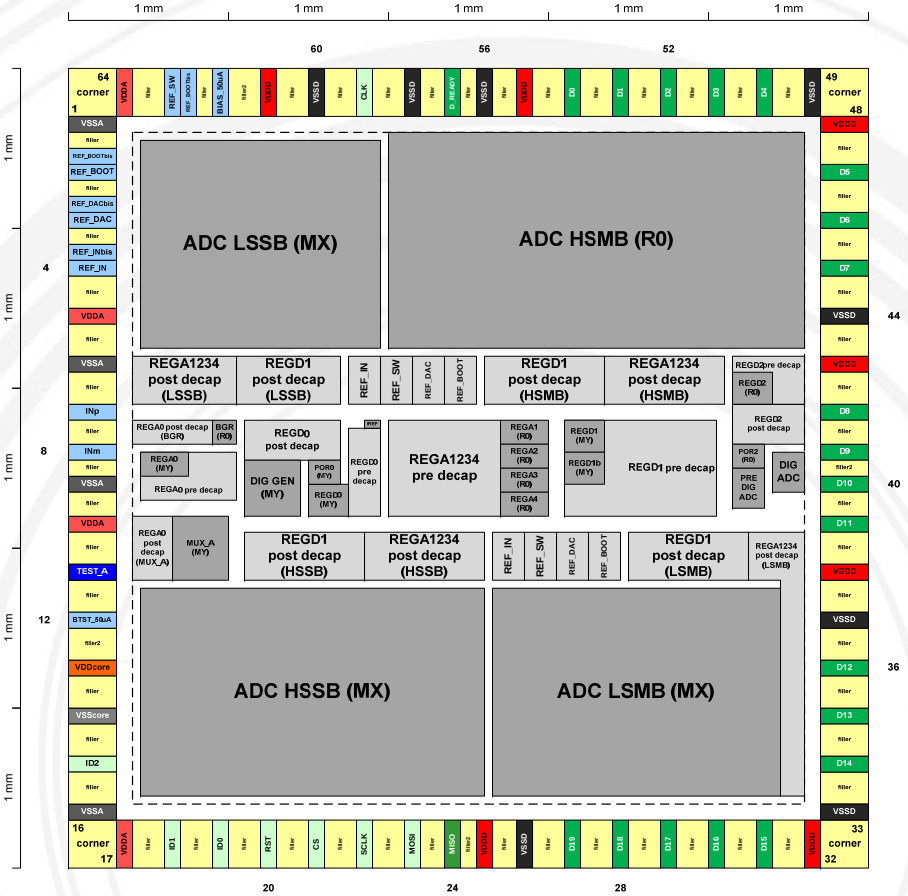


ARQ-CVA001 Floorplan

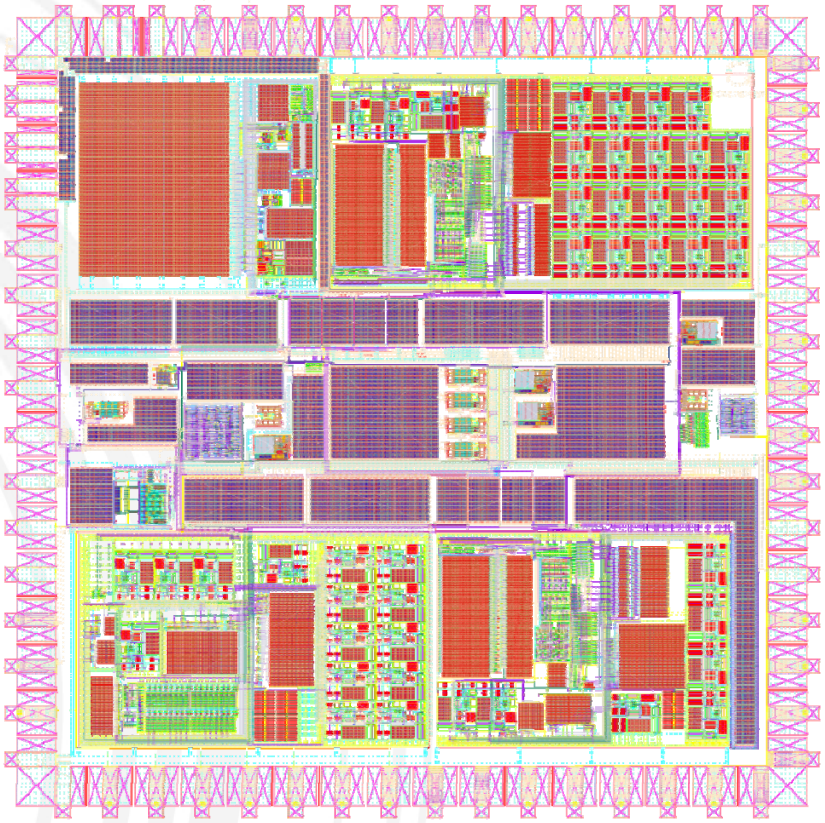


ARQ-CVA001 Layout

Programme of Work (5) – Design and fabrication phases

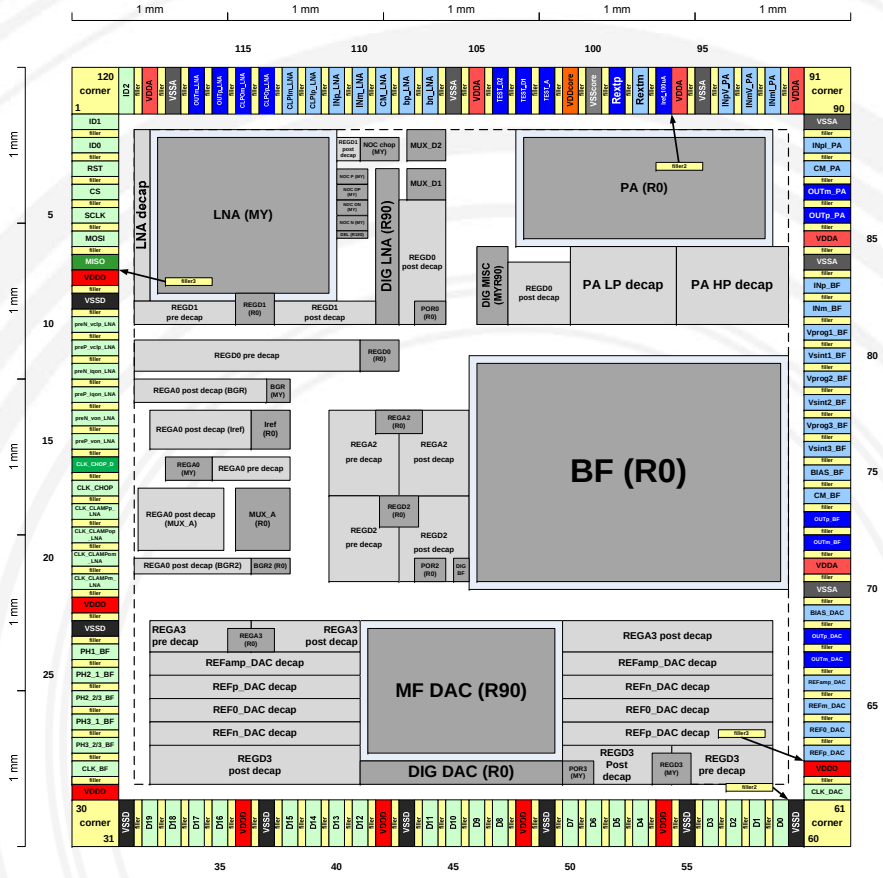


ARQ-CVB001 Floorplan

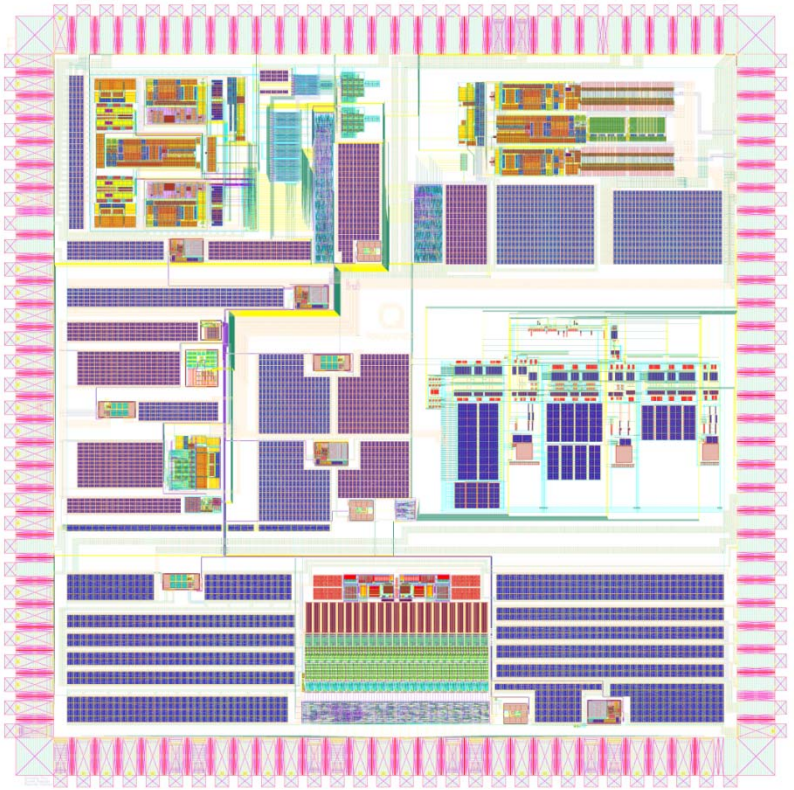


ARQ-CVB001 Layout

Programme of Work (6) – Design and fabrication phases

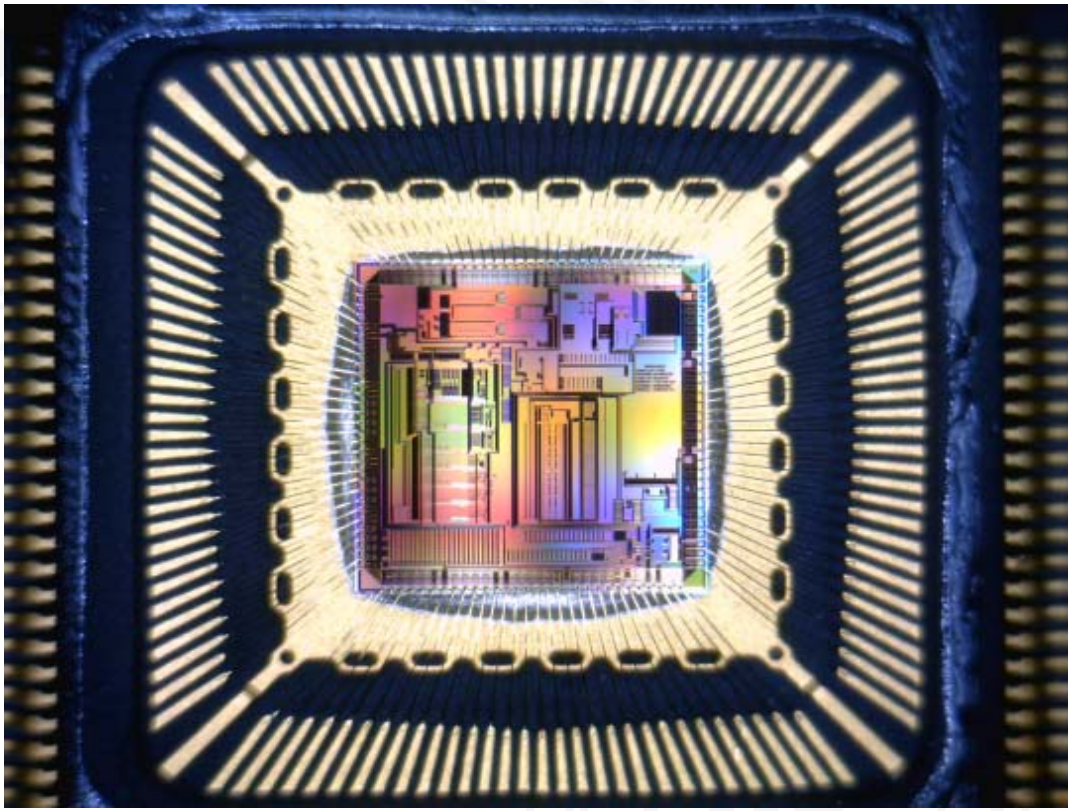


ARQ-CVC001 Floorplan



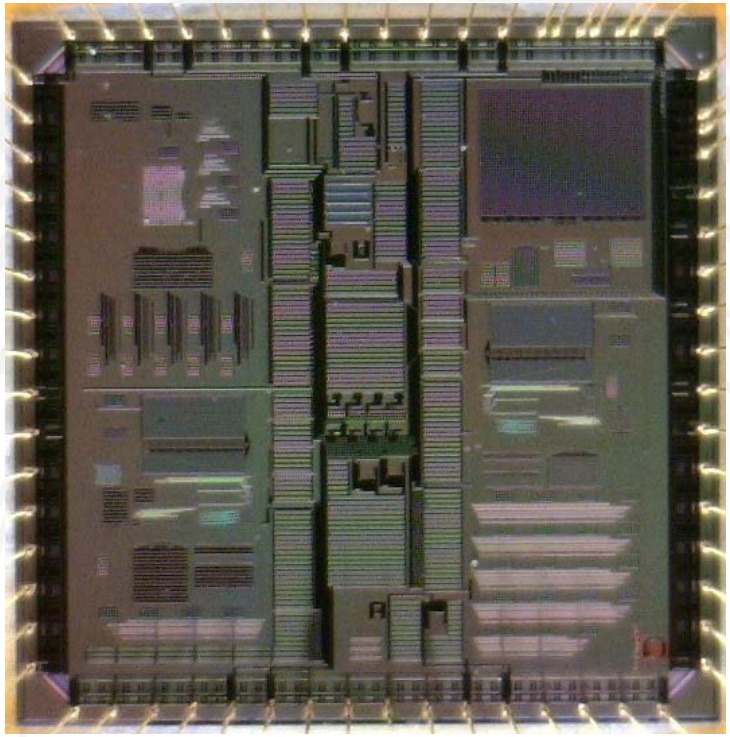
ARQ-CVC001 Layout

Programme of Work (7) – Design and fabrication phases

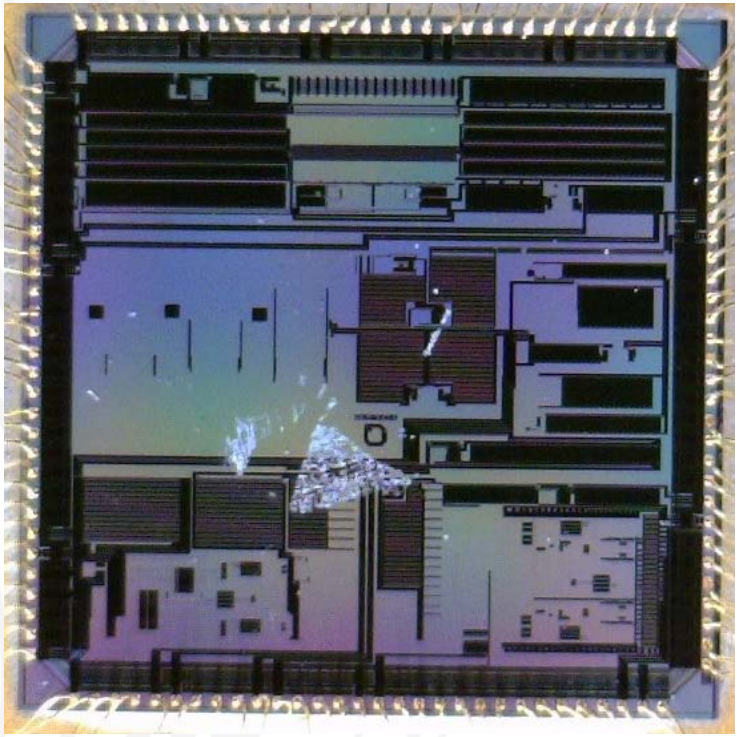


ARQ-CVA001 on a LQFP120 package

Programme of Work (8) – Design and fabrication phases



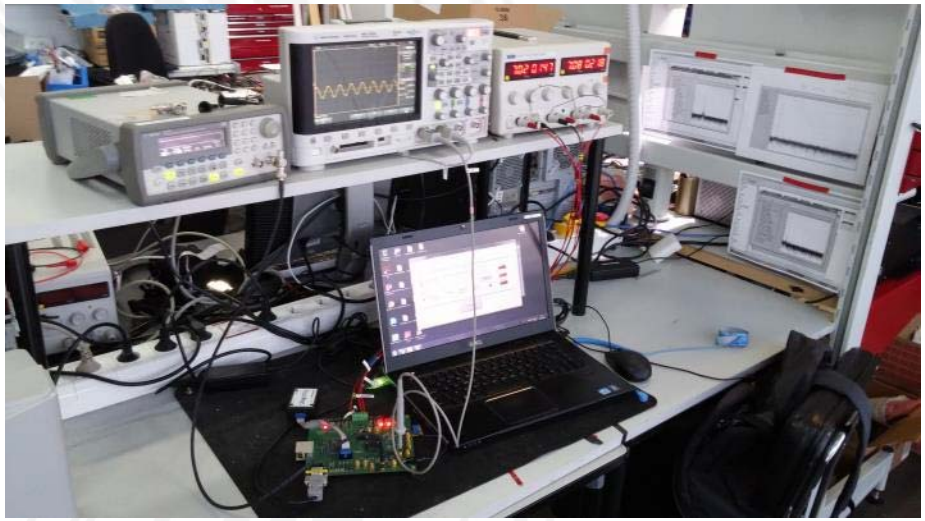
ARQ-CVB001 on a QFN64 package



ARQ-CVC001 on a LQFP120 package

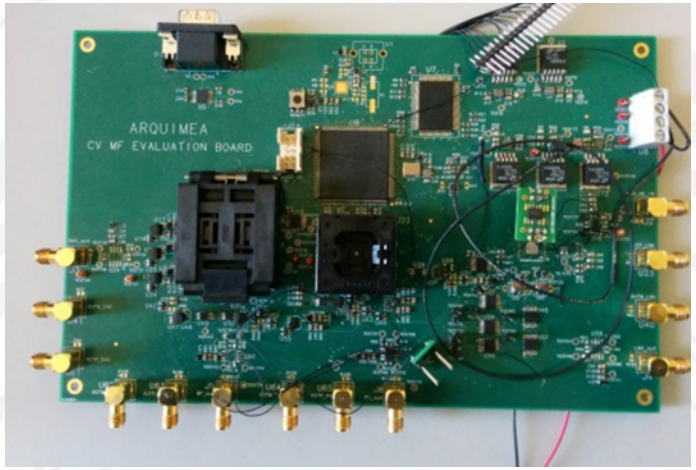
Programme of Work (9) – Blocks and ASIC validation

- Apart from the electrical validation of the ASICS, ARQ-CVA001 was radiation tested in the parallel activity led by TRAD
- At this stage the HF ADC IP was selected to be included in the SSDP project

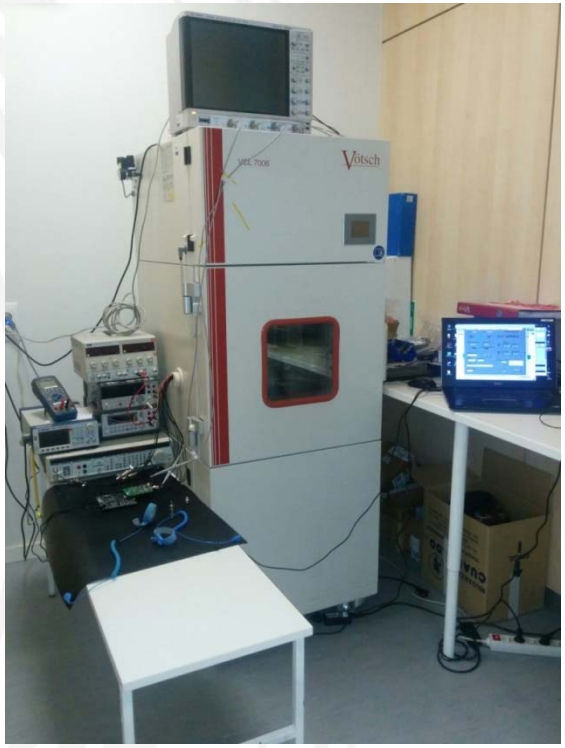


ARQ-CVA001 functional test board and setup at ARQ facilities

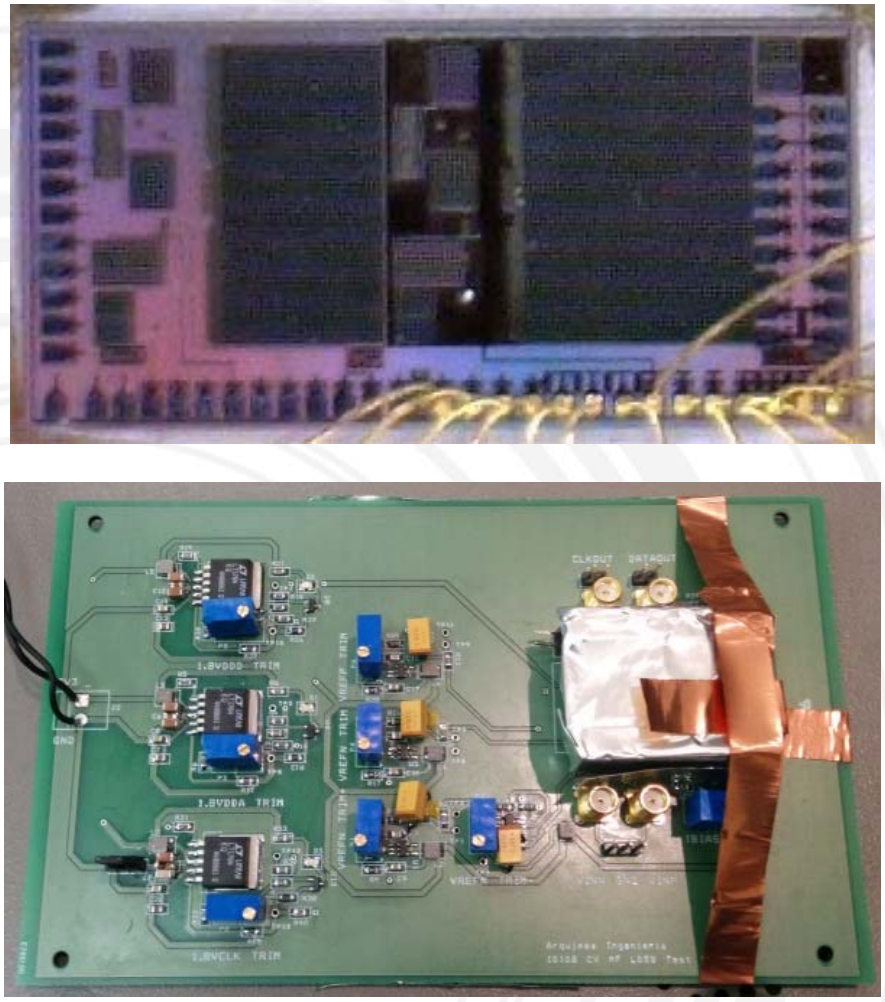
Programme of Work (10) – Blocks and ASIC validation



ARQ-CVB00, ARQ-CVC001 functional test boards and setup at ARQ facilities



Programme of Work (11) – Blocks and ASIC validation

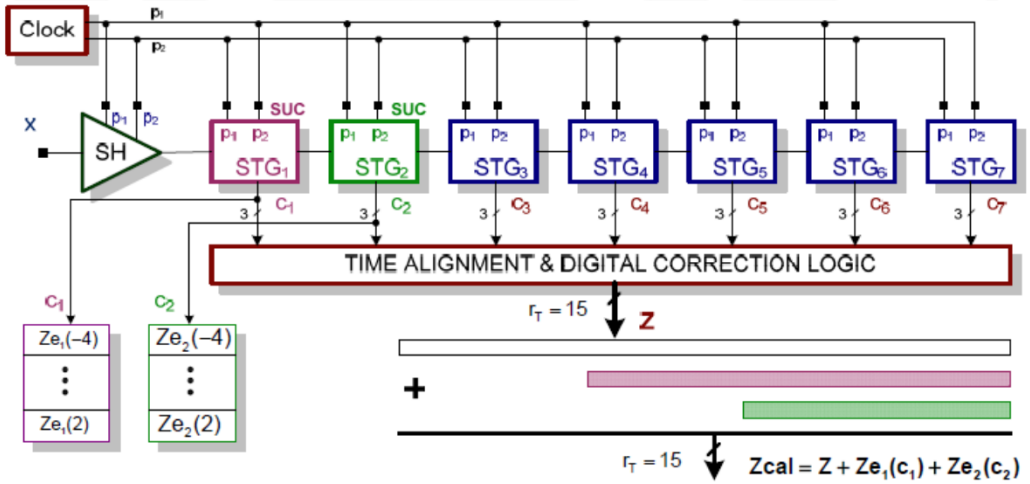


LOPO ASIC packaged die and test board

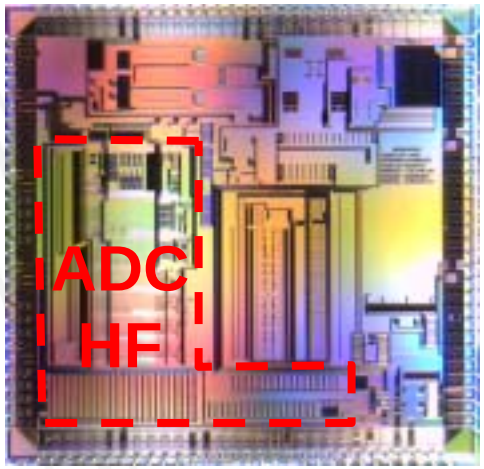
Main results discussion (1)

- Given the large number of IPs developed in the frame of the project special dedication was taken to test those that were considered more attractive from the user level perspective, which where:
  1. ADC HF
  2. DAC HF
  3. LNA HF and MF
  4. PA HF and MF
  5. LSSB MF
  6. Common blocks

Main results discussion (2)
ADC HF - Architecture



ADC HF (pipeline) block diagram



CVA001 µ-photo

Main results discussion (3)
ADC HF - Electrical performances

- The ADC was conceived considering the need of a specially designed package to tackle with the inductance constraints of the refn and refp signals. Since the final package was a standard one degradation on the performances of this block was expected.
- ENOB obtained at block simulation level was 12.5 at 100 Msps (target spec)
- Top level simulations (considering pads and package inductance) show ac degradation of 5 effective bits.
- Validation also shows the same degradation.
- Another issue observed at top level simulations and at validation is that full scale was reduced from 2Vppd to 400 mVppd.

Main results discussion (4)
ADC HF - Electrical performances

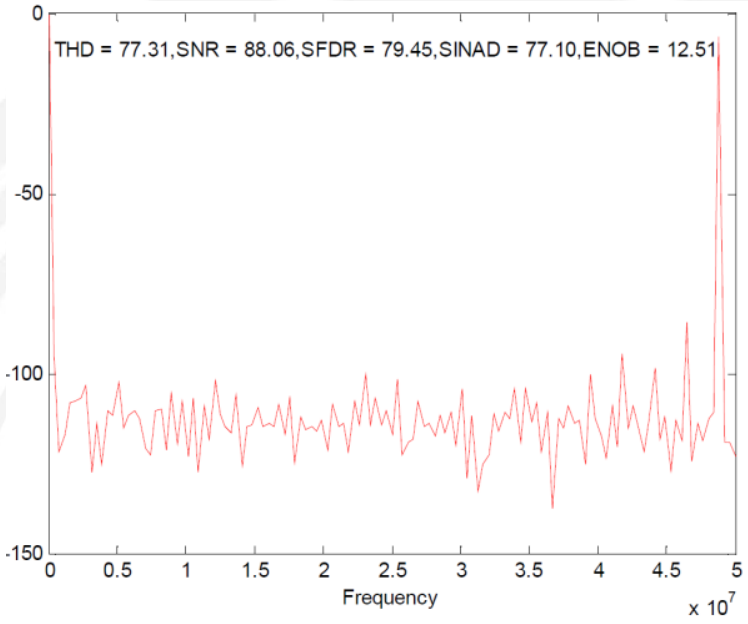
- A voltage drop produced by the combination of the impedance of the DARE INALOG pad and the high current produced the full scale reduction.
- In the second iteration of the chip CVA-002 IANALOG pads where replaced by OANALOG for refn and refp pins. Top level simulations with this change showed that the ENOB degradation was reduced to 3 effective bits and the full scale range was preserved (9 ENOB performance)
- The effect of package inductance is confined then to 3 effective bits
- The signal spectrum shows that the third harmonic dominates the noise floor which remains at the expected level (SNR is around 65dB)

- *Currently in the SSDP project, the IP with DARE PADs and some additional buffers has reached 10ENOB at 50MHz*

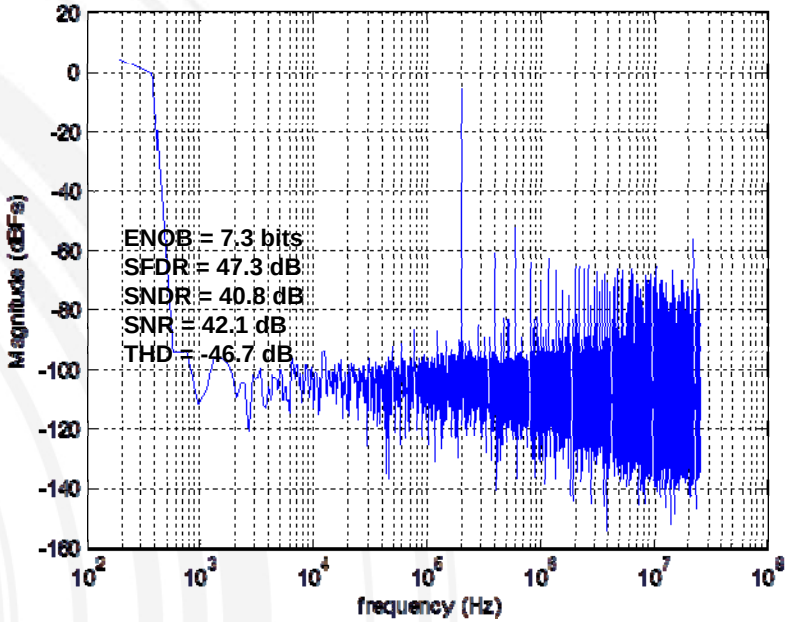
Main results discussion (5)
ADC HF - Electrical performances

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVA spec	CVA001 val	CVA002 ver	Comments
1	ADC_SPLR_MAX	Maximum sampling rate (at least)	MS/s	100	100	100	100	50	50	
2	ADC_NB_MAX	Number of bits @ADC_SPLR_MIN (at least)	bits	15	15	15	15	15	15	
3	ADC_ENOB_MIN	Minimum Effective number of bits @ADC_SPLR_MAX (at least)	bits	10	11	12,56	10	5,5	9,3	ENOB was reduced in ARQ-CVA001 due to the voltage ringing in REFp and REFm references. The performances were enhanced replacing IANALOG pads with OANALOG pads which reduces the impedance of the path.
4	ADC_THD_MIN	Total Harmonic Distortion @ADC_SPLR_MAX (at most)	dB	-70	-80	-	-64	-44	58,53	THD was reduced in ARQ-CVA001 due to the voltage ringing in REFp and REFm references. The performances were enhanced replacing IANALOG pads with OANALOG pads which reduces the impedance of the path. HD3 is the dominant harmonic.
5	ADC_IDD_MAX	Overall current consumption @ADC_SPLR_MAX (at most)	mA	150	250	-	250	155	143	
6	ADC_SEE_SCS	SEU and SET saturation cross section	cm^2	-	-			< 2E-04		
7	ADC_SEE_LETTH	SEU and SET LET threshold	$MeV \cdot cm^2/mg$	-	-			< 18,5		
8	ADC_TID	Maximum TID	krad(Si)	300	-	-	-	> 505	-	

Main results discussion (6)
ADC HF - Electrical performances



Simulated FFT



Measured FFT

Main results discussion (7)
ADC HF - Radiation performances

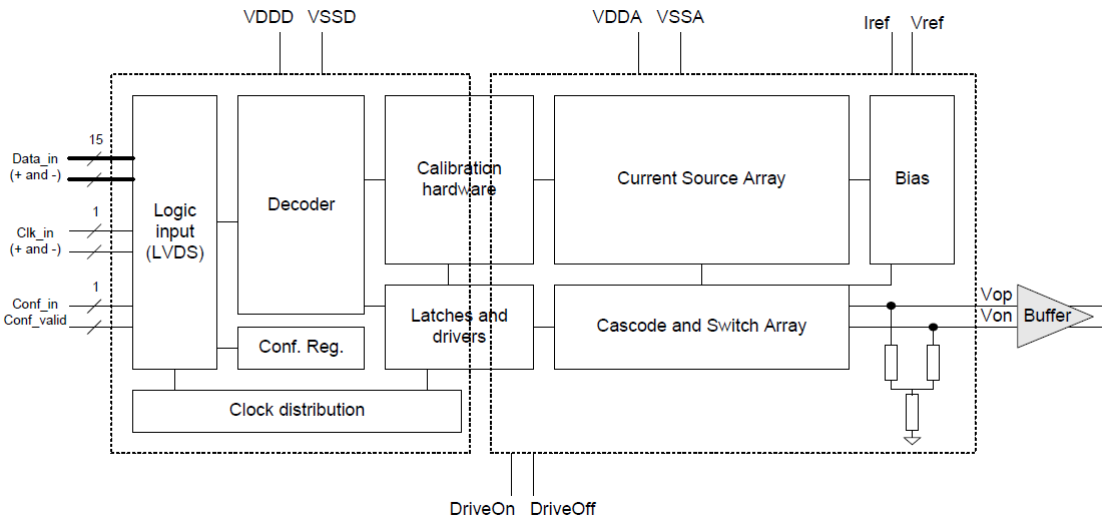
- TID: no degradation observed.
- SEL: no SEL at room temperature.
- SEUs: Detected. Since DARE cells are insensitive to SEUs the potential candidates for SEUs are a few full-custom RS latches and latch comparators.
- SETs: Detected.

Main results discussion (8)
ADC HF - Future/current use

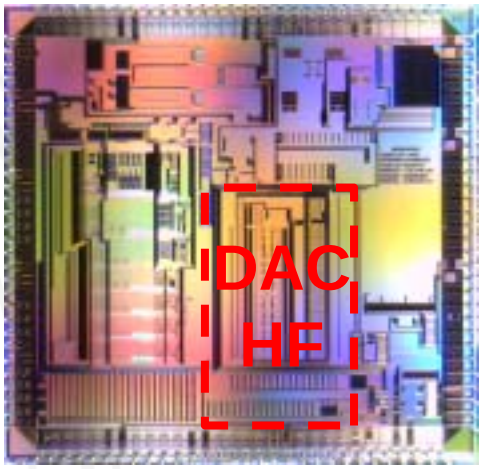
- Interest from the space community.
- Re-used at the Scalable Sensor Data Processor (SSDP) project.
- Further updates for SET and SEU tolerance.

- *To be upgraded on a new ESA project that has just started (by IMSE)*

Main results discussion (9)
DAC HF - Architecture



DAC HF (current steering) block diagram



CVA001 µ-photo

Main results discussion (10)
DAC HF - Electrical performances

- ENOB obtained at block level simulation was 11.4 at 100 Msps for a 50MHz bandwidth and 12.3 at 100Msps for a 5MHz bandwidth (spec was 12 ENOB).
- Top level simulations (considering pads and package model reached 10.5 ENOB all over the bandwidth.
- This bandwidth was confirmed at validation.

Main results discussion (11)
DAC HF - Electrical performances summary

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVA spec	CVA001 val	CVA002 ver
1	DAC_SPLR_MAX	Maximum sampling rate (at least)	MS/s	100	100	100	100	100	100
2	DAC_NB_MAX	Number of bits @DAC_SPLR_MIN (at least)	bits	15	15	15	15	15	15
3	DAC_ENOB_MIN	Effective number of bits @DAC_SPLR_MAX (at least)	bits	10	13 @5MHz 10 @50MHz	12,3 @5MHz 11,4 @50MHz	9	7,8	10,38 @5MHz 10,52 @50MHz
4	DAC_THD_MIN	Total Harmonic Distortion @DAC_SPLR_MAX (at most)	dB	-70	-78 @5MHz -63 @50MHz	-66	-57	-64,43@5MHz	-
5	DAC_IDD_MAX	Current consumption @DAC_SPLR_MAX (at most)	mA	60	60	-	60	52	38
6	DAC_SET_SCS	SET saturation cross section	cm^2	-	-			< 7E-05	
7	DAC_SET_LETTH	SET LET threshold	$MeV \cdot cm^2/mg$	-	-			< 18,5	
8	DAC_TID	Maximum TID	krad(Si)	300	-	-	-	> 505	-

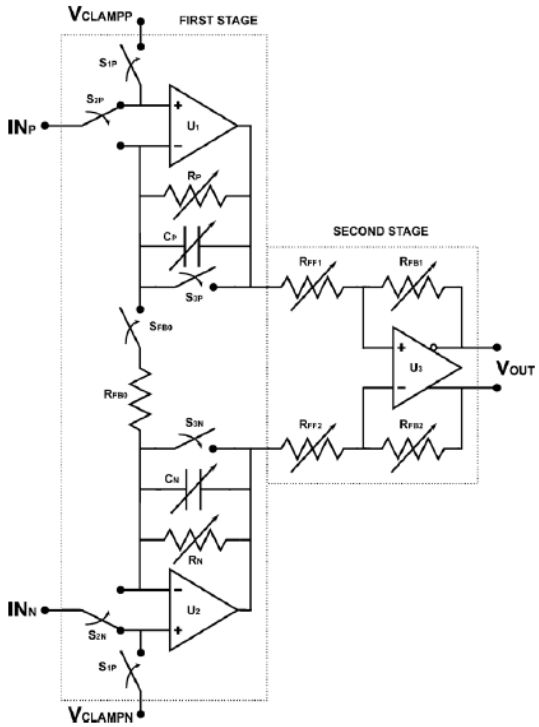
Main results discussion (12)
DAC HF - Radiation performances

- TID: no degradation observed.
- SEL: no SEL at room temperature.
- SEUs: No SEUs detected.
- SETs: Detected.

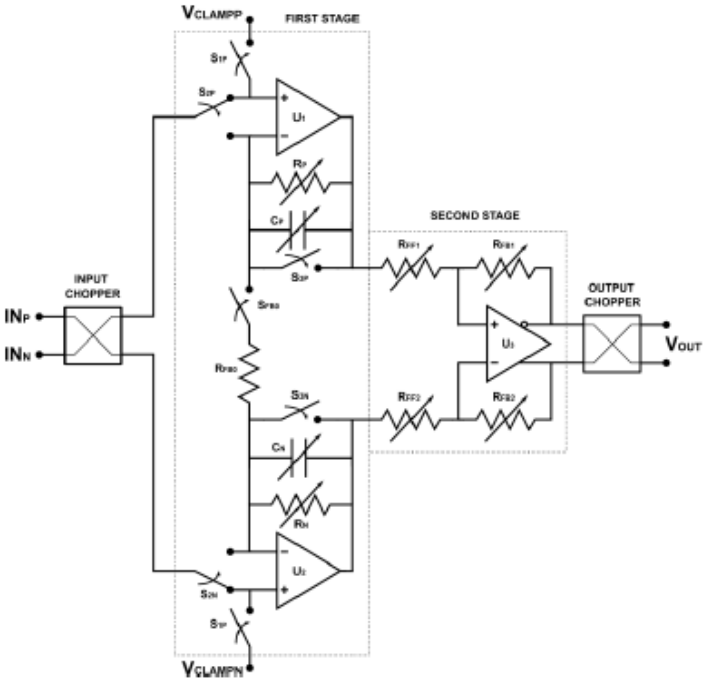
Main results discussion (13)
DAC HF - Future use

- Interest from the space community.
- Further updates for SET tolerance.
- If SET tolerance is to be updated a recommendation would be to harden the net handling the bias voltage of the MSB current sources.

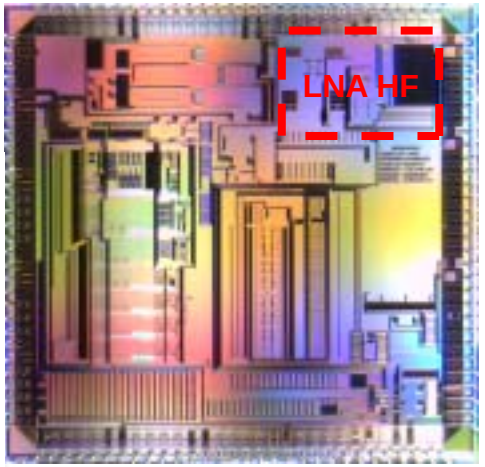
Main results discussion (14)
LNA HF and MF - Architecture



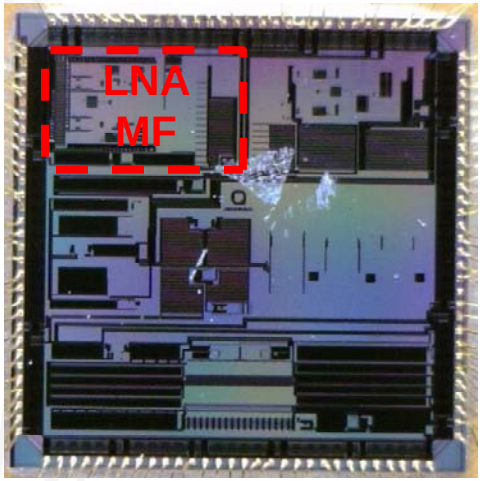
LNA HF
block diagram



LNA MF
block diagram



CVA001 µ-photo



CVC001 µ-photo

Main results discussion (15)
LNA HF and MF - Electrical performances

- These blocks had a great number of configuration options and switches.
- From the IP point of view the designs were correctly verified at block level reaching the agreed performances. As examples:
  - HF: the noise density reached is between 3.7 and 6.5 nv/√Hz
  - MF: The noise density reached is between 5.9 and 9.2 nv/√Hz
- Top level simulations showed also good results in line with the block level ones with the only exception of the noise density obtained at low gain configurations (in HF) which is one order of magnitude above (up to 30 nv/√Hz)
- The validation did not cover all parameters however the tested modes show good results as expected
- Performance is maintained over the whole operational temperature range.

Main results discussion (16)
LNA HF - Electrical performances summary

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVA spec	CVA001 val	CVA002 ver
1	LNA_VV_GF	Voltage mode: gain flatness between LNA_FMIN and LNA_FMAX for G=21dB (at most)	dBc	0,2	0,4	0,4	0,4	2,2	0,62
2	LNA_VV_N	Voltage mode: noise density at most	nV/√Hz	2	6.5	6.5	5.9	-	5
3	LNA_VV_THD_DIF_TYP	Voltage mode: Typical Total Harmonic Distortion for differential input (0dB gain, 1kΩ//1pF load, 800mV common mode in, 900mV common mode out)	dB@MHz	-	AC off: -102@1 -91@3 -74@10 -66@20 -46@50 AC on: -70@1 -71@3 -75@10 -68@20 -47@50	AC off: -102@1 -91@3 -74@10 -66@20 -46@50 AC on: -70@1 -71@3 -75@10 -68@20 -47@50	-102@1	AC on: -28@25	AC on: 52@25
4	LNA_VV_IDD_MAX	Voltage mode: Current consumption @LNA_VV_GMAX	mA	15	42 (AC off) 49 (AC on)	42 (AC off) 49 (AC on)	50	40	-
5	LNA_VI_GF	Trans-impedance mode: gain flatness in -0.4dB bandwidth (at most)	dB(Ω)	0,2			0,4	-	-
6	LNA_VI_THD_DIF_TYP	Trans-impedance mode: Total Harmonic Distortion (660uA input amplitude, 3kΩ gain, 1kΩ//1pF load, 0V common mode in, 900mV common mode out)	dB	-	-69@1 -70@3 -70@10 -64@20 -45@50	-69@1 -70@3 -70@10 -64@20 -45@50	-70	-32@20MHz	
7	LNA_VI_IDD_MAX	Trans impedance mode: Current consumption	mA	-	42 (AC off) 49 (AC on)	42 (AC off) 49 (AC on)	50	40	
8	LNA_SET_SCS	SET saturation cross section	cm²	-				< 2E-04	
9	LNA_SET_LETTH	SET LET threshold	MeV·cm²/mg	-				< 18,5	
10	LNA_TID	Maximum TID	krad(Si)	300				> 505	

Main results discussion (17)
LNA MF - Electrical performances summary

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVC spec	CVC-001 ver	CVC-001 val
1	LNA_VV_GF	Voltage mode: gain flatness between LNA_FMIN and LNA_FMAX for G=21dB (at most)	dBc	0,2	0,4	0,4	0,4	-	1,284
2	LNA_VV_N_TYP	Voltage mode: typical noise density	nV/√Hz@KHz	-	6.6@1	6.6@1	-	7.13@3	289,4@100
3	LNA_VV_THD_DIF_TYP	Voltage mode: Typical Total Harmonic Distortion for differential input (2Vpp tone, 0dB gain, 1kΩ//1pF load, 1,5V common mode in, 900mV common mode out)	dB@MHz	-	-110@0,1 -103@0,3 -94@1 -89@2 -76@5	-110@0,1 -103@0,3 -94@1 -89@2 -76@5	-	-	-80,14@0,1 -72,81@0,3 -71,03@1 -70,54@2
4	LNA_VV_IDD_MAX	Voltage mode: Current consumption @LNA_VV_GMAX	mA	4	24	24	20	-	20,15
5	Operational temperature range	Temperature range where performance is maintained	ºC	-10 to 85	-10 to 85	-10 to 85	-10 to 85	-	-10 to 85

Main results discussion (18)
LNA HF - Radiation performances

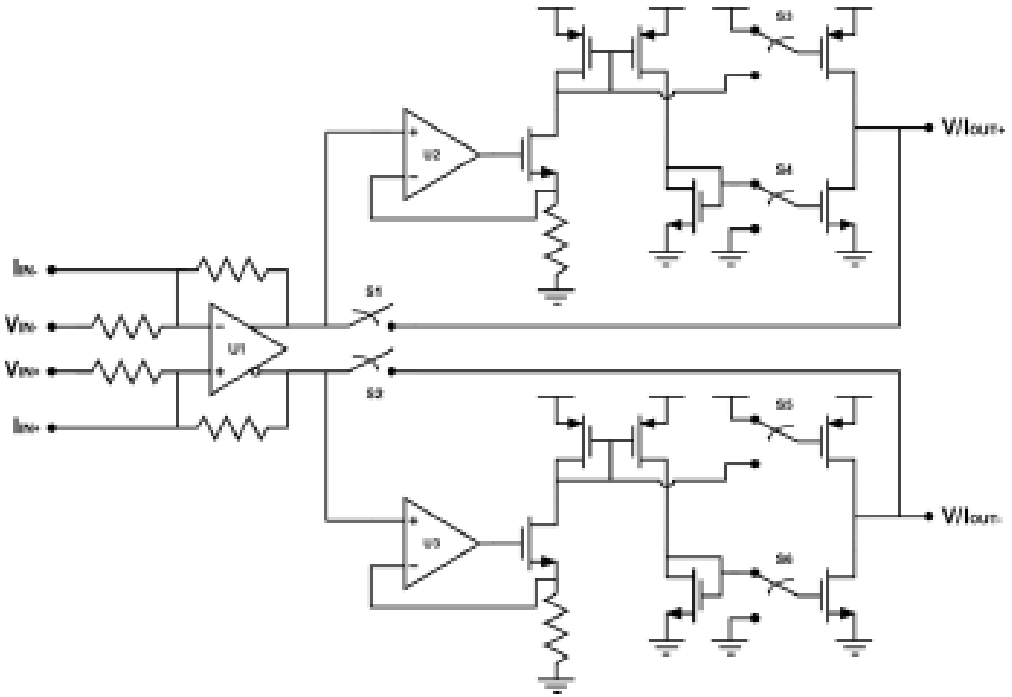
- TID: no degradation observed.
- SEL: no SEL at room temperature.
- SEUs: No SEUs detected.
- SETs: Detected.

- *LNA MF not tested under radiation.*

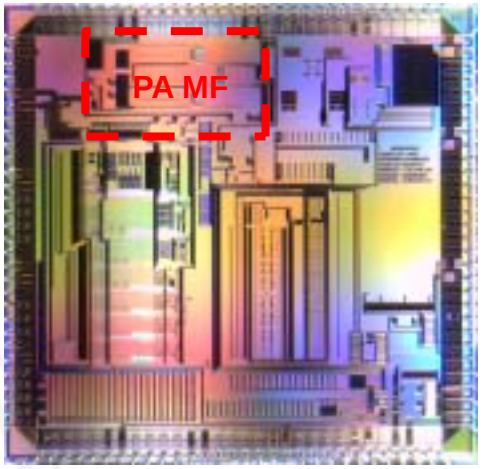
Main results discussion (19)
LNA HF and MF - Future use

- The future use of the IPs are still open. Although very good results have been obtained it still has to be analysed how the blocks can be re-used in the future since no feedback from potential users has been received so far.
- Further updates for SET tolerance for HF would be interesting.
- If SET tolerance is to be updated a recommendation would be to pay special attention to the input net of the output stage.
- It would be nice to know the behavior of the MF block under radiation but similar results to the HF blocks are expected.

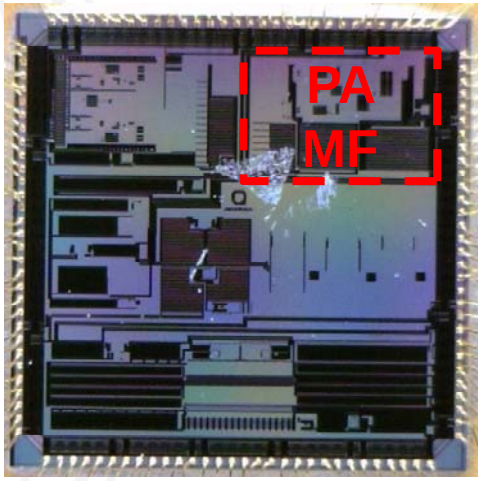
Main results discussion (20)
PA HF and MF – Architecture



PA MF and HF block diagram



CVA001 µ-photo



CVC001 µ-photo

Main results discussion (21)
PA HF and MF – Electrical performances

- These blocks had a great number of configuration options and switches.
- From the IP point of view the design was correctly verified at block level reaching the agreed performances. As remarkable examples:
  - HF: The output current reached was 80 mA, the differential output voltage range was 2Vpp, the PSRR worst case was 32dB (50MHz) and the THD was 74dB (at 1MHz) and 56dB (20Mhz)
  - MF: the output current reached in voltage mode was 160 mA and the THD was 84dB (at 0.3MHz) and 74dB (1MHz) in voltage output mode.
- The top level simulations run showed better PSRR results in HF w.r.t simulation (50 dB) –improvement related to the presence of a voltage regulator- and similar THD results.

Main results discussion (22)
PA HF and MF – Electrical performances

- The validation of this block did not cover all parameters due to the high number of configuration options. As an example, The THD measured at 25 MHz was 52dB (HF) and at 0.3MHz was 73.4 dB (MF) which are in line with the expected results.
- Performance is maintained over the whole operational temperature range.

Main results discussion (23)
PA HF – Electrical performances summary

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVA spec	CVA001 val	CVA002 ver
1	PA_VX_F_MAX	Voltage output mode: maximum input frequency (at least)	MHz	100	57 @-0.4dB 93 @-3dB		57 @-0.4dB 93 @-3dB		-
2	PA_VX_THD_TYP	Voltage output mode: Total Harmonic Distortion (at most)	dB	-	-74 @1MHz -74 @3MHz -66 @10MHz -56 @20MHz -44 @50MHz		-74 @1MHz -74 @3MHz -66 @10MHz -56 @20MHz -44 @50MHz	-52 @25MHz	-75,9
3	PA_VX_PSRR_TYP	Voltage output mode: power supply rejection ratio (at most)	dB	-	-56 @0.1MHz -46 @50MHz		-56 @0.1MHz -46 @50MHz		-67,8 @0.1MHz -58,2 @50MHz
4	PA_IX_F_MAX	Voltage output mode: maximum input frequency (at least)	MHz	100	51 @-0.4dB 120 @-3dB		51 @-0.4dB 120 @-3dB		-
5	PA_IX_THD_TYP	Current output mode: Total Harmonic Distortion (at most)	dB	-	-68 @1MHz -59 @3MHz -47 @10MHz -42 @20MHz -41 @50MHz		-68 @1MHz -59 @3MHz -47 @10MHz -42 @20MHz -41 @50MHz	-24 @25MHz	-
6	PA_IX_PSRR_TYP	Current output mode: power supply rejection ratio (at most)	dB	-	-81 @0.1MHz -65 @50MHz		-81 @0.1MHz -65 @50MHz		-
7	PA_SET_SCS	SET saturation cross section	cm^2	-				< 3E-05	
8	PA_SET_LETTH	SET LET threshold	$MeV \cdot cm^2/mg$	-				< 18,5	
9	PA_TID	Maximum TID	krad(Si)	300				> 505	
10	PA_IX_OUT_RD	Current output mode: output full-scale peak-to-peak differential current (at most)	mA	80				36	

Main results discussion (24)
PA MF – Electrical performances summary

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVC-001 spec	CVC-001 ver	CVC-001 val
1	PA_VX_F_MAX	Voltage output mode: maximum input frequency (at least)	MHz	10	17@-0,4dB 27@-3dB	17@-0,4dB 27@-3dB	17@-0,4dB 28@-3dB	19,65@-3dB	>2
2	PA_VX_THD_TYP	Voltage output mode: Typical Total Harmonic Distortion (at most)	dB	-	-87@0,1MHz -84@0,3MHz -74@1MHz -79@2MHz -48@5MHz	-87@0,1MHz -84@0,3MHz -74@1MHz -79@2MHz -48@5MHz	-87@0,1MHz -84@0,3MHz -74@1MHz -79@2MHz -48@5MHz	-67,72@1MHz	-75,5@01MHz - 73,4@0,3MHz -66,6@1MHz 64,2@2MHz
3	PA_VX_IDD_MAX	Voltage output mode: maximum current consumption for single-ended 50Ω load (at most)	mA	-	160	160	160	-	100
4	PA_TID	Maximum TID	krad(Si)	300				> 505	
5	Operational temperature range	Temperature range where performance is maintained	ºC	-10 to 85	-10 to 85	-10 to 85	-10 to 85	-	-10 to 85

Main results discussion (25)
PA HF – Radiation performances

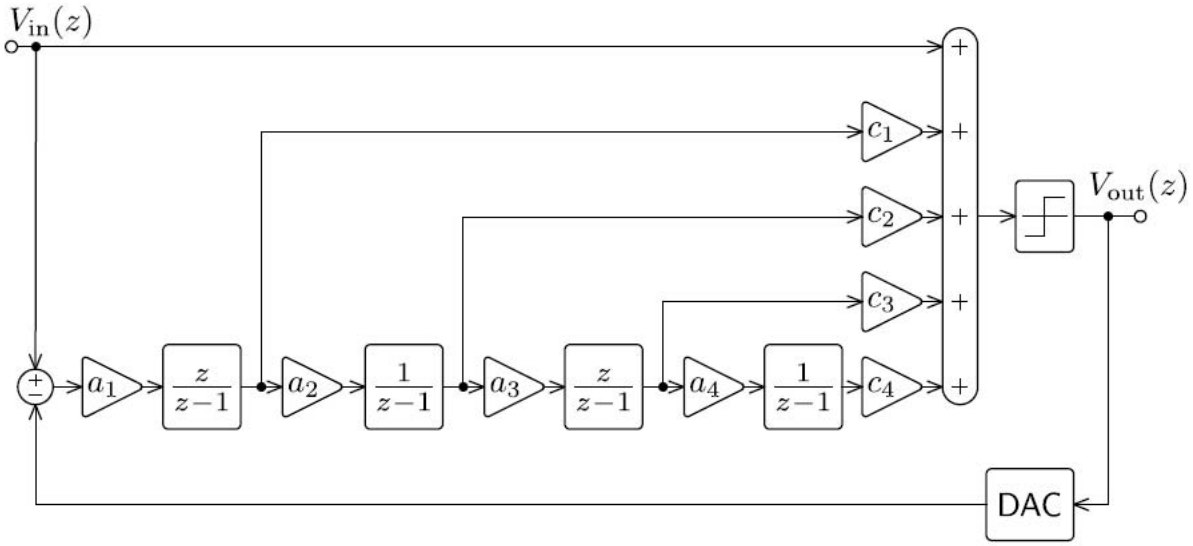
- TID: no degradation observed.
- SEL: no SEL at room temperature.
- SEUs: No SEUs detected.
- SETs: Detected.

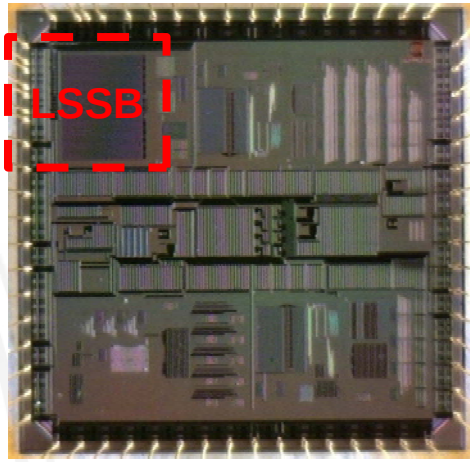
- *PA MF not tested under radiation.*

Main results discussion (26)
PA HF and MF – Future use

- The future use of these IPs is still open. Although very good results have been obtained it still has to be analysed how the block can be re-used in the future since no feedback from potential users has been received so far.
- Further updates for SET tolerance on HF would be interesting .
- If SET tolerance is to be updated in HF a recommendation would be to pay special attention to the input net of the output stage.
- It would be nice to know the behavior of the MF block under radiation but similar results to the HF blocks are expected.

Main results discussion (27)
ADC MF - Architecture





Coefficient	a_1	a_2	a_3	a_4	c_1	c_2	c_3	c_4
Value	0.2	0.4	0.1	0.1	1	1	1	2

Main results discussion (28)
ADC MF - Architecture

- The converter was divided into four modules
  - Low-speed single-bit (LSSB): a ΣΔ modulator designed for the [50; 150] kHz signal frequency range and with the highest resolution
  - High-speed single-bit (HSSB: a) ΣΔ modulator designed for the [150; 500] kHz signal frequency range.
  - Low-speed multi-bit (LSMB): a ΣΔ modulator, designed for the [0.5; 2] MHz signal frequency range.
  - High-speed multi-bit (HSMB): a ΣΔ modulator, designed for the [2; 5] MHz frequency range and the lowest resolution.
- The four modulators were implemented on the ARQ-CVB001 chip with their inputs interconnected.
- The LSSB modulator was also integrated on the LOPO ASIC.

Main results discussion (29)
ADC MF - Verification

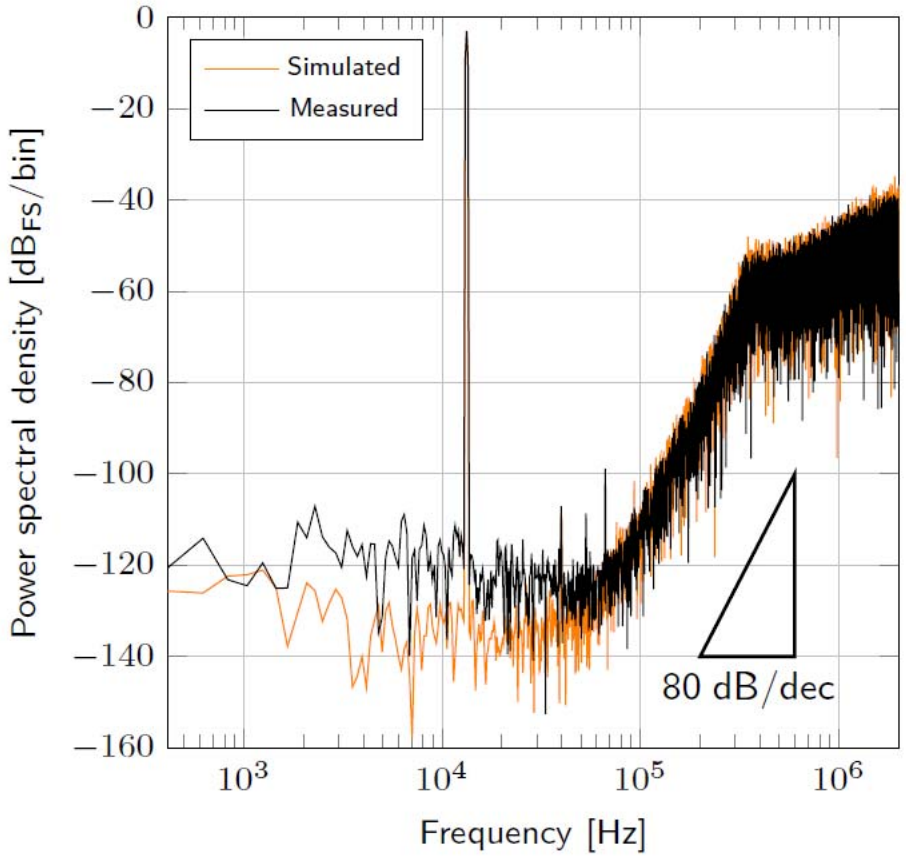
- The promising results of the LSSB modulator made clear that the focus should be put on this block validation wise speaking.
- Including the four modulators on the same die had major drawbacks in terms of performance. Additionally the fact that the ADC input was the same for all modulators reduced the performance even more.

Main results discussion (30)
LSSB MF – Electrical performance summary

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVB spec	CVB ver	CVB val	LOPO val	Comments
1	ADC_SPLR	Minimum Nyquist sampling rate (at most)	MS/s	0,1	0,1	0,1	0,1	0,1	0,1	0,1	
2	ADC_ENOB_MAX	Maximum Effective number of bits @ADC_SPLR_MIN (at least)	bits	19	18	18	17	-	9,47	14,57	Top level simulations of the LSSB module were not conclusive since the simulations could not complete the required number of cycles for a proper FFT. Performances of the LOPO ASIC were limited by the input source noise.
3	ADC_SFDR_MAX	Spurious Free Dynamic Range @ADC_SPLR_MIN (at least)	dBc	130	110	-	104	-	81,7	95,3	
4	ADC_IDD_MIN	Overall current consumption @ADC_SPLR_MIN (at most)	mA	1	2	9,07	2	-	10	7	
5	Operational temperature range	Temperature range where performance is maintained	°C	-10 to 85	-10 to 85	-10 to 85	-10 to 85	-	-10 to 85	-10 to 85	

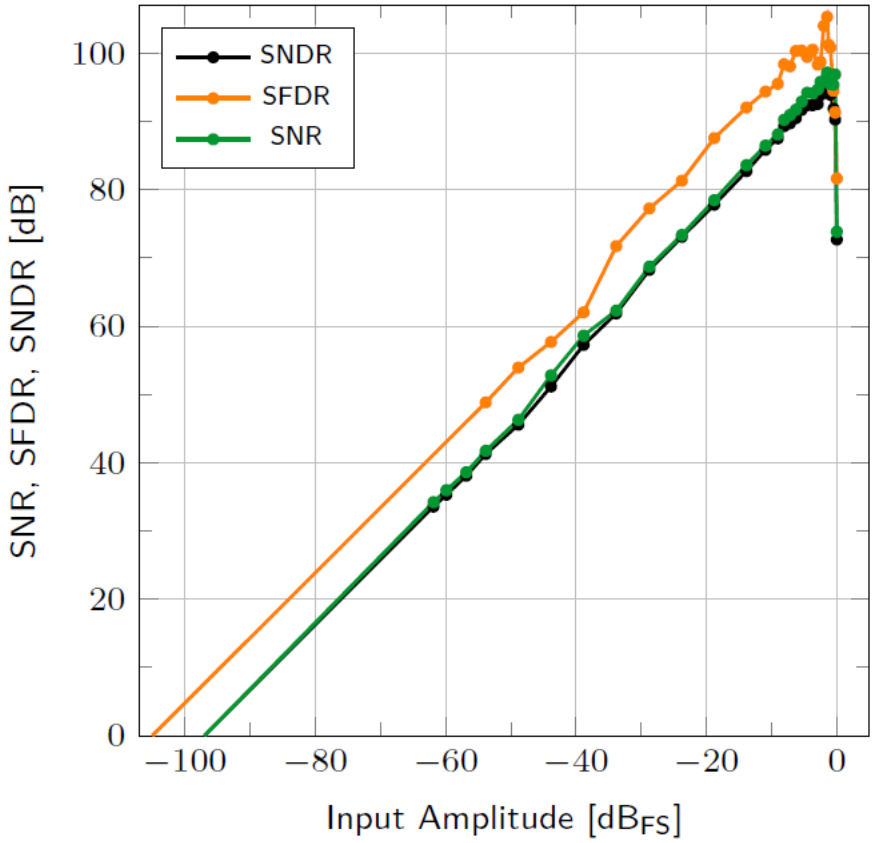
Main results discussion (31)
LSSB MF – Electrical performance

- 2.4-Vpp differential full scale
- -2-dB_{FS} input amplitude
- 80-dB/decade noise-shaping slope observed

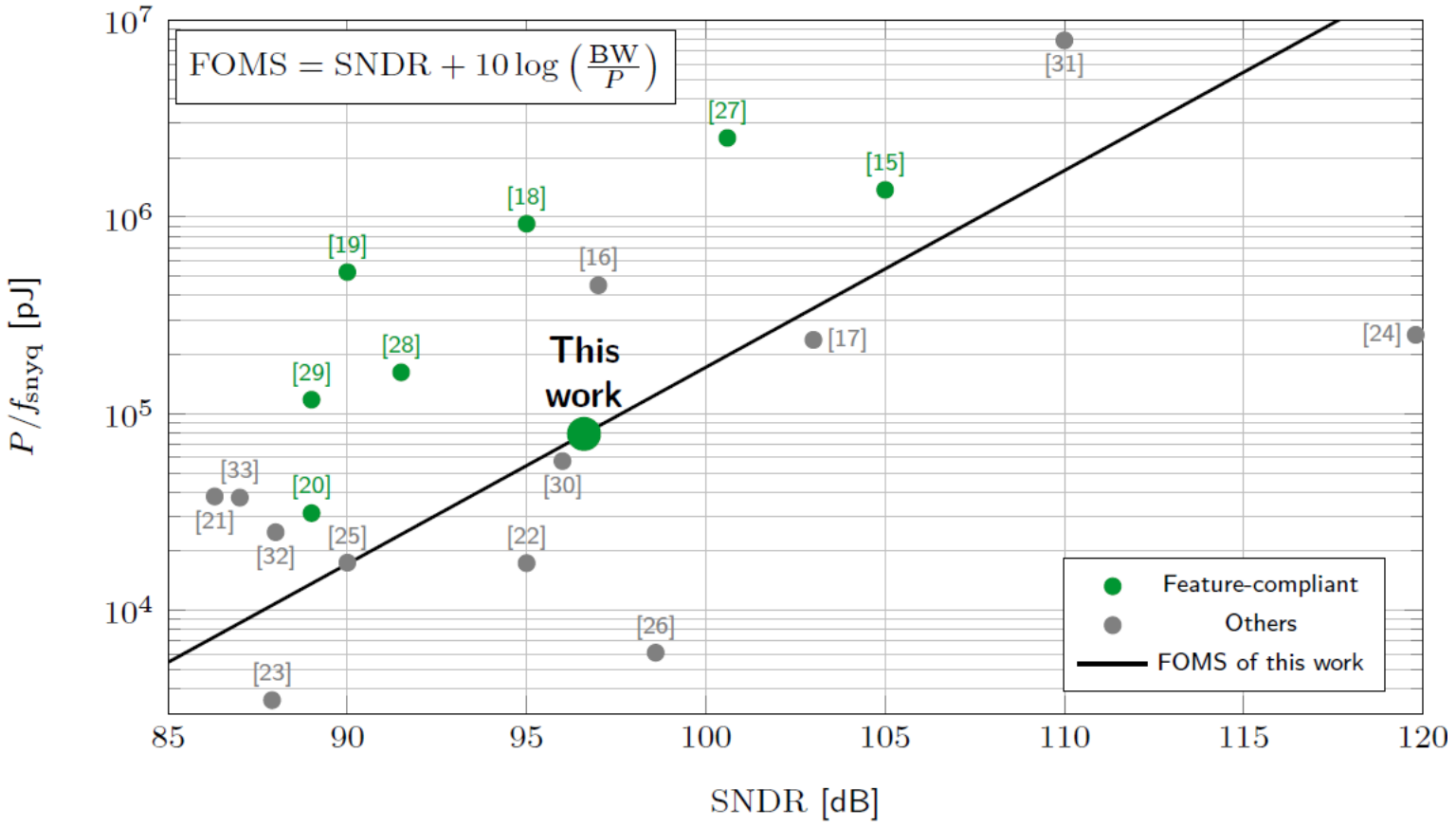


Main results discussion (32)
LSSB MF – Electrical performance

- 96.6-dB SNDR
- 105.3-dB SFDR
- 97-dB DR
- SNDR degradation at high amplitudes is avoided



Main results discussion (33)
LSSB MF – Electrical performance



Main results discussion (34)
LSSB MF – Electrical performance

Figures from slides 50, 51 and 52 extracted from Stepan Sutula “Low-Power High-Resolution CMOS Switched-Capacitor Delta-Sigma Analog-to-Digital Converters for Sensor Applications

Additional references:

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Main results discussion (35)
ADC MF – Future use

- Its future seems promising giving the good electrical results obtained.

- It would be interesting to perform radiations tests on this IP
- *This IP has been selected as baseline for a new ASIC development led by CRISA & ARQUIMEA*

Main results discussion (36)
Common blocks - Performances

- Several common blocks designed: a first-order bandgap reference, a high power linear regulator (suitable to supply analogue circuitry) and a set of register banks to be programmed through SPI
- The bandgap reference was designed to have 0.3mV variation over the temperature range and was measured at validation to have 30mV variation among different components and the temperature range.
- The regulator performances have not been exhaustively validated but functional tests show its correct operation
- The SPI register banks were designed and validated up to 10 MHz.

Main results discussion (37)
Common block – Future use

- The common block IPs could be reused in the future as building blocks of bigger ASICs or test vehicles.

Conclusions

- With a single tape-out most of the objectives were reached
- From the complexity and specifications point of view it was a quite challenging project.
- A quite steep learning curve was produced at integration and validation level
- Interesting IPs are made available to the space community and they could be made available in a future ASIC with minimum risk
- A good example of industry and academia working together.
- A good knowledge is gained in the system integration of IPs

Thank you for your time!

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