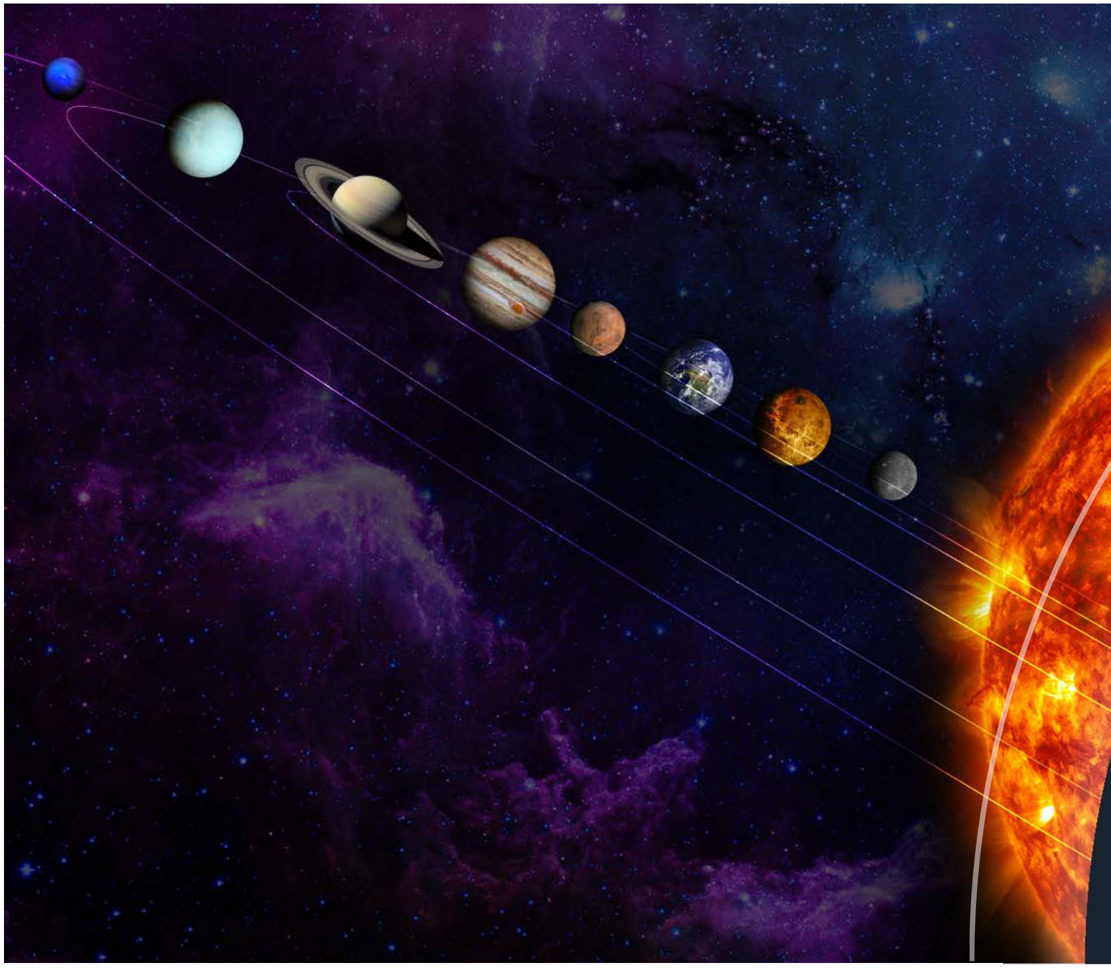
Prototyping of Space Protocol(s) for SPI

TEC-EDD

TOs: Giorgio Magistrati and Carlos Urbina Ortega

Contract Details

- Program: **TRP** (with two parallel contracts)
- Budget: **400 k€**
- Prime + Subco: **TAS-I + TELETEL S.A.**
- Duration: **20 months** (12 + 8)
- Main Objectives:
  - Detailed definition and **analysis of use cases** for SPI bus in space
  - **Build a draft specification** based on space application use cases
  - Propose and prototype appropriate **signal integrity techniques**
  - Development of a **demonstrator** for SPI
  - Create general **simulation models** for SPI and validate them on the demonstrator



Prototyping of space protocol(s) for SPI

ESA Data Systems Division Final Presentation Day

A.Tramutola, D.Rolfo/A. Tavoularis

Table of contents

SPI protocol for space applications

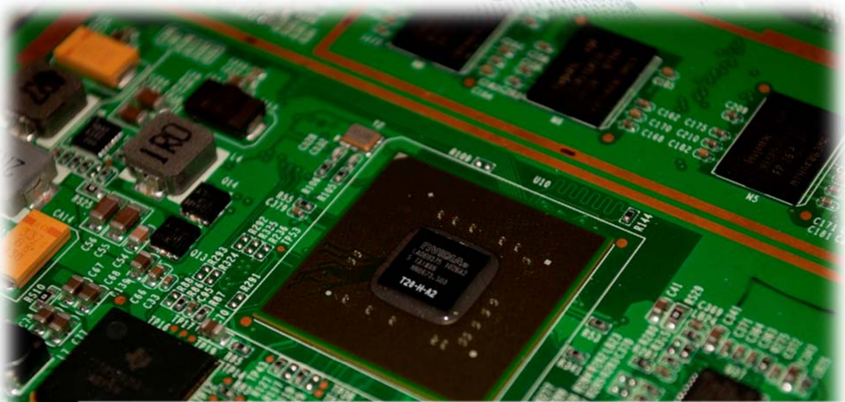
SPI protocol specification

- Physical layer
- Protocol layer

Demonstrator requirements and design

- Bus termination analysis and implementation
- Crosstalk analysis

Demonstrator verification and feedback to specification



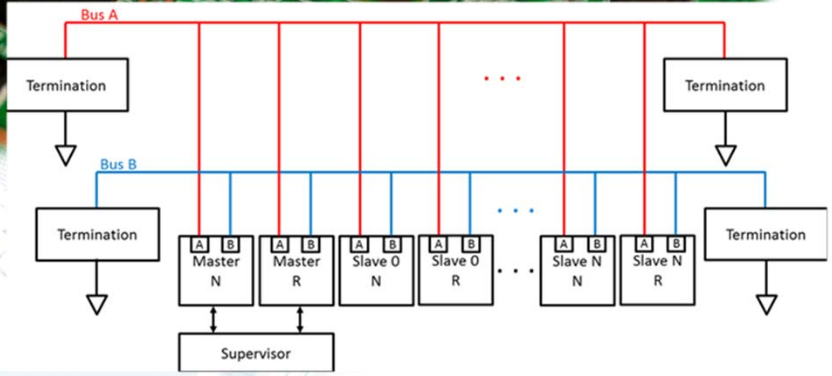


Table of contents

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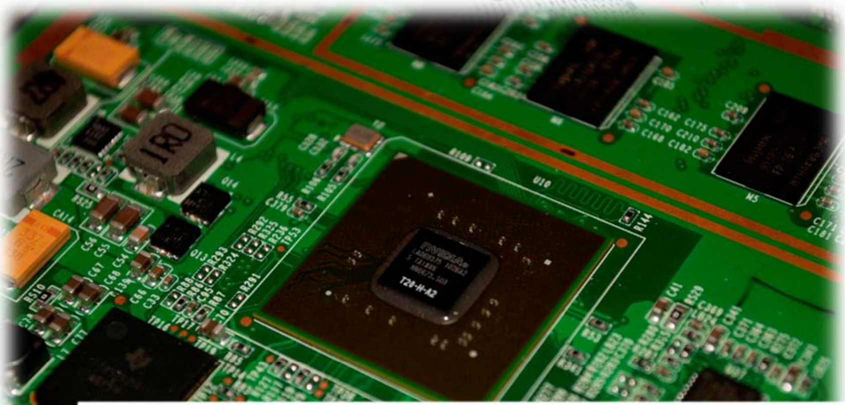
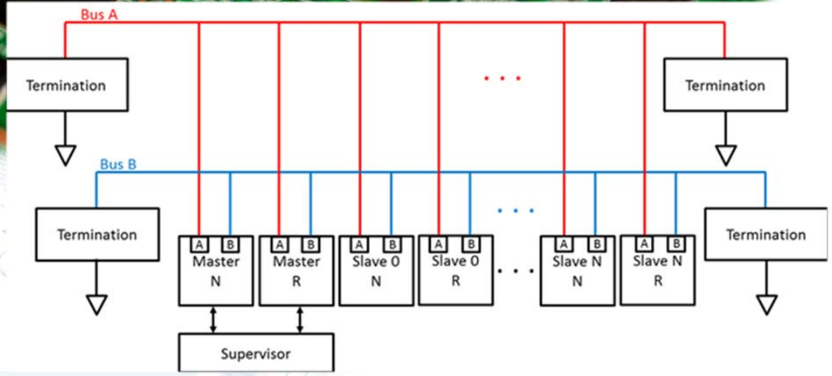




SPI Protocol for Space Application

Serial communication protocol industrial trend

- evolution of sensors acquisition and actuator systems (Temperature, Pressure , Encoders, Accelerometers)
- enhancement of data handling systems reconfiguration capability (reconfigurable FPGA, non-volatile memories (EEPROM, MRAM, FRAM, FLASH))

Road map of ESA studies and R&D

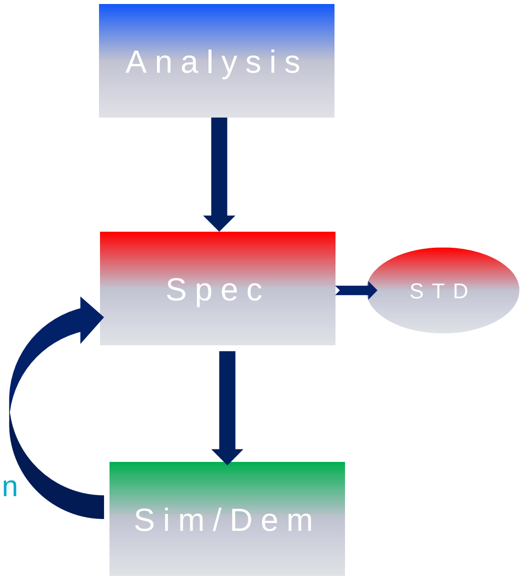
- CAN bus for space application (CABCOM)
- Sensor network (I2C, one Wire), SDI (I2C, SPI), SPI4SPACE (SPI)

Why SPI protocol for space applications?

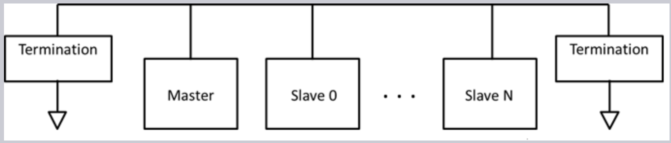
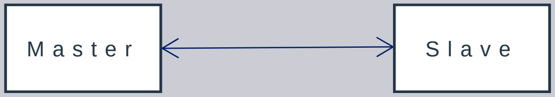
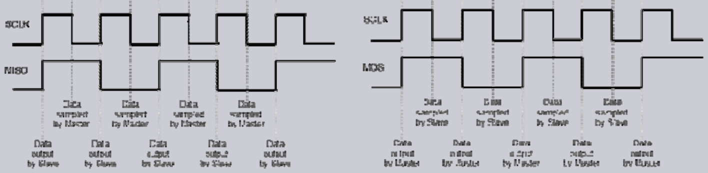
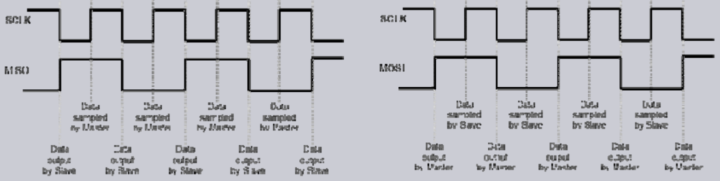
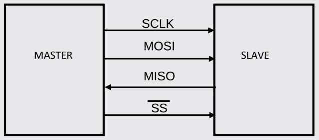
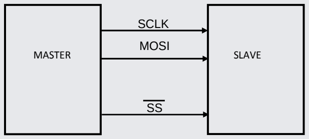
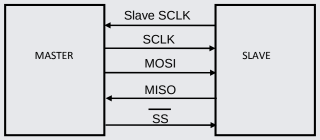
- Widely adopted for commercial devices
- High throughput, low power consumption, simple implementation of interface architecture

SPI4SPACE objectives and workflow

- Target applications: internal module bus, external point to point communication
- challenging performances (30MHz, 1m bus, 10m point to point)
- Analysis , Specification, feedback from Simulation and Demonstrator



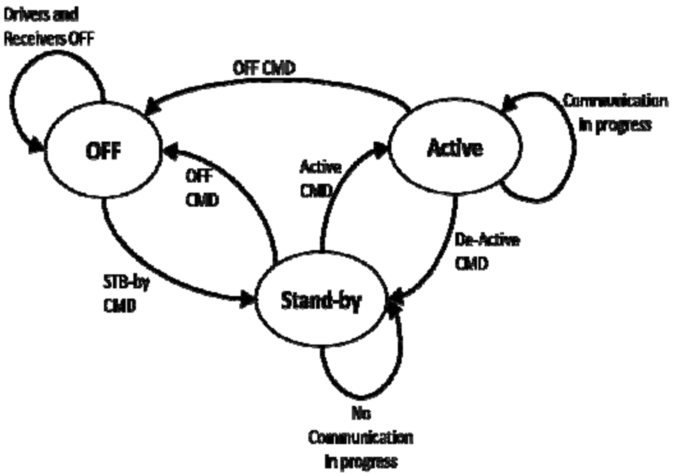
SPI Protocol Specification : physical layer

	Internal bus	External Point to Point
Topology	 Termination Master Slave 0 . . . Slave N Termination	
Electrical family	**3.3V LVCMOS :** • Backward compatibility with existing space grade components • Low power consumption • timing performances better than similar families (AHCMOS)	**LVDS :** • Standard de facto for high-speed serial link in space application
Signal Timing	**CPOL= 0, CPHA=1 (or CPOL=1, CPHA=0)** 	**CPOL=CPHA= 1 (or CPOL=CPHA= 0)** 
Bus Signals	**Conf.1**  **Conf.2** 	**Conf.3** 

SPI Protocol Specification : protocol layer

For both SPI Internal bus and SPI point to point topologies the defined protocol states are:

- OFF state :
  - when all drivers and receivers of the units linked (Master and Slaves) are not powered
- STAND-BY state :
  - when drivers and receivers of the Master and at least of one Slave are powered but no communication is taking place
    - (no Chip Select is activated)
- ACTIVE state :
  - when the drivers and receivers of the Master and at least of one Slave are powered and communication is in progress
    - (the relevant Chip Select is activated)


Drivers and Receivers OFF
OFF CMD
Communication In progress
OFF
Active
OFF CMD
Active CMD
De-Active CMD
STB-by CMD
Stand-by
No Communication In progress

Three different protocol Layers have been defined to cover different needs in terms of communication capability :

- SPI0, provides backward compatibility to existing space-qualified units/components equipped with SPI I/F
- SPI1, implements mechanisms to verify correctness of the communication and to allow messages transmission
- SPI2, offers a more robust communication structure defining commands to activate device's internal functions

SPI Protocol Specification : protocol layer SPI0

SPI0 is an OPEN Protocol Layer providing a wide degree of freedom to implementers

- It has been included to provide backward compatibility to existing space-qualified components

SPI0 provides maximum flexibility in message content, format, length and type

- They can be defined according to the implementer's needs
- 8 bits is considered as preferred message word width

SPI0 word bit transmission order is fixed as MSB first

- This is in agreement with all existing space-qualified components

ICs	Interface purpose	I/Fs role	SPI signals	Data Sampling edge	Data Output Edge	CS activation level	Data word length	Voltage Level
ADC128S102QML	Configuration	Slave	4-wire	Rising	Falling	Low	24	1.9V CMOS
ADC12D1600QML	Configuration	Slave	4-wire	Rising	Falling	Low	24	1.9V CMOS
ADC128S102QML	Data/command	Slave	4-wire	Rising	Falling	Low	16	3.3V LVCMOS
CDCM7005-SP	Configuration	Slave	3-wire	Rising	N/A	Low	32	3.3V LVCMOS
DAC121S101QML	Data	Slave	3-wire	Falling	N/A	Low	16	3.3V LVCMOS
LX7730	Data/command	Slave	4-wire	Falling	Rising	Low	15	3.3V LVCMOS
LM98640QML-SP	Configuration	Slave	4-wire	Rising	Rising	Low	16	3.3V LVCMOS (V_{OH} except.)
SMV320C6727B-SP	Data/command	Master/ Slave	4-wire/ 5-wire	User definable	User definable	Low	Up to 256	3.3V LVCMOS
SPI4SPACE	User definable	Master/ Slave	3-wire/ 4-wire	User definable	User definable	Low	SPI0 User definable	3.3V LVCMOS

COTS NVRAM components equipped with SPI interfaces

Part Name	Type	Producer	Footprint
MR25H10	MRAM	Everspin	DFN8
CY15B102Q-SXE	FRAM	Cypress	SOIC-8
M25P05-AVMN6P	nvRAM	Micron	SO8
AT25256B	EEPROM	Atmel	SOIC-8
MB85RS256A	FRAM	Fujitsu	SOP-8
LE25U40CMC-AH	Serial Flash	ON Semiconductor	SOIC-8
MR45V256A	FRAM	LAPIS/ROHM	SOP-8
FM25W256-G	FRAM	Cypress	SOIC-8
SST25VF080B	NAND	Microchip	SOIC-8
SST25VF020B	NOR	Microchip	SOIC-8

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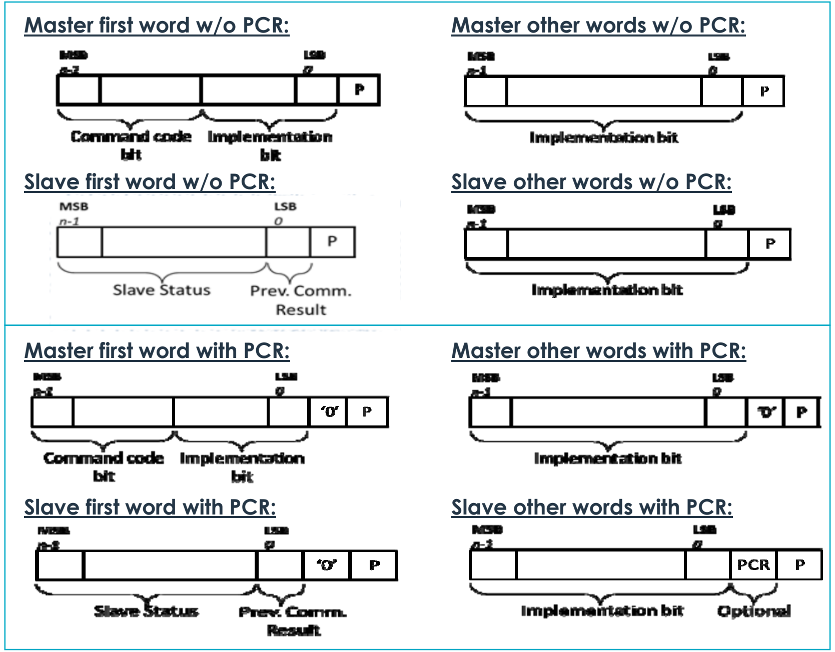
SPI Protocol Specification : protocol layer SPI1

Data Link Layer

- Word width : 8,16,24,32 bit + Parity bit (odd) => default 8 bit
  - Slaves can be configured to use one of the above word width
  - Master shall support all slaves connected to the SPI interface
  - MSB is transferred first, LSB last
- Parity Check Report (PCR) in the slave messages can be optionally supported
  - Master messages shall include dummy bit to have the same word width



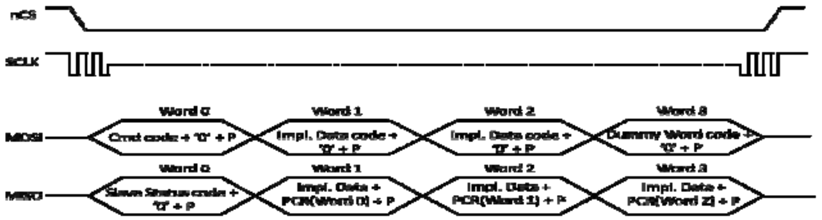
Network Layer

- Support three types of transfers :
  - WORD Transfer
  - BLOCK Transfer
  - BLOCK Transfer with Error Detection

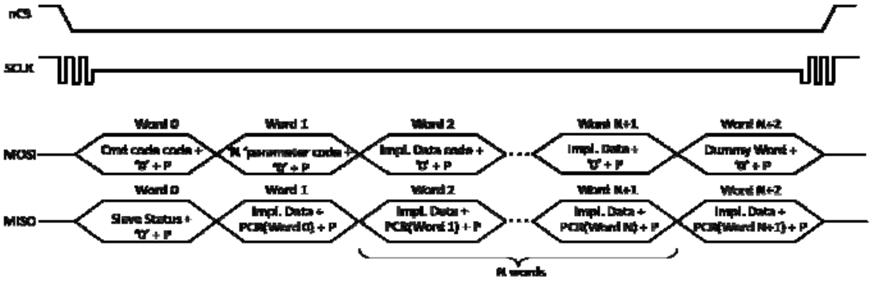
SPI Protocol Specification : protocol layer SPI1

WORD Transfer

- Messages size : Min 2 words, max 4 words
- First word sent by Master is a *Command code*
- First word sent by Slave includes its *Status code*
- Other words include implementation data
- Communication is closed by the *Dummy word code*
- Master starts and completes/aborts communication activating/deactivating nCS signal of selected Slave



nCS
SCLK
MOSI
MISO
Word 0
Cmd code + '0' + P
Word 1
Impl. Data code + '0' + P
Word 2
Impl. Data code + '0' + P
Word 3
Dummy Word code + '0' + P
Word 0
Slave Status code + '0' + P
Word 1
Impl. Data + PCR(Word 0) + P
Word 2
Impl. Data + PCR(Word 1) + P
Word 3
Impl. Data + PCR(Word 2) + P

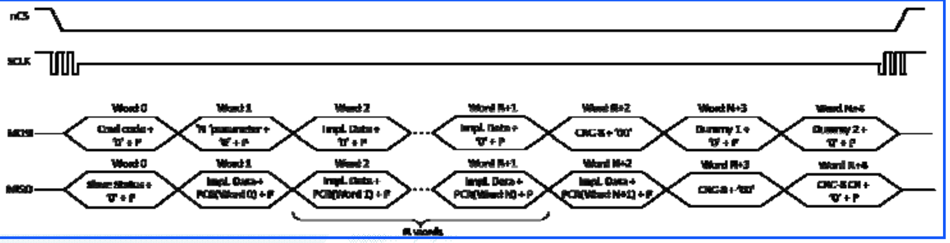


BLOCK Transfer

- Message size : N words + 3; (N = 0 ÷ 255)
- Second word sent by the Master includes the N value
- Content and functions of the other words is the same of WORD Transfer layer
- Master starts and completes/aborts communication activating/deactivating nCS signal of selected Slave

BLOCK Transfer with Error Detection

- Message size : same of BLOCK transfer + 2 words
- CRC-8 detection code is computed by Master on words from 0 to N+1 and included in word N+2
- Additional Dummy word is used to allow the acquisition of the CRC-8 Check Report from Slave



SPI Protocol Specification : protocol layer SPI2

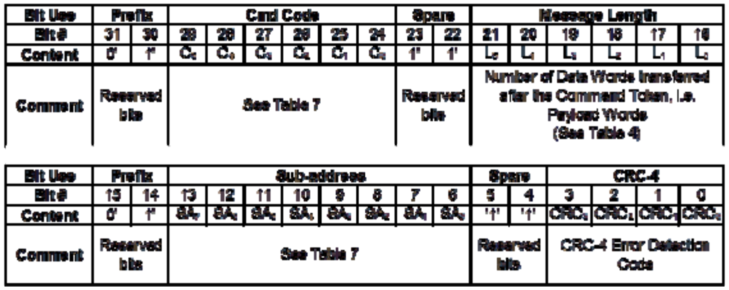
Data Link Layer

- Word width : 32 bit + Parity bit (odd), MSB is transferred first
- Parity Check Report (PCR) in the slave messages can be optionally supported , Master messages shall include dummy bit

Network Layer

- Master / Slave implements capability to:
  - Transmit/receive *Command Token*
  - Transmit/receive optional *Data Word* according to the command code
  - Receive/transmit *Response Token*
  - Receive/Transmit optional *Data Word* according to the command code
- SPI2 fixes the command code to be used to provide standardization
  - some examples : DO_BIT_SPI (do built in test), READ_BIT_SPI (retrieve BIT results), SYNCH + Payload word (synchronize internal registers), TICK (to increment time registers), GET_RESP_TOKEN (request Response Token), READ_SA (read content of Slave sub-address), WRITE_SA (write into a Slave sub-address), etc…
- SPI2 defines also status of the previous transmission in the Response Token :
  - SPI_TERMINAL_FAULT, MESSAGE_ERROR, ADDRESS_ERROR, ILLEGAL_COMMAND

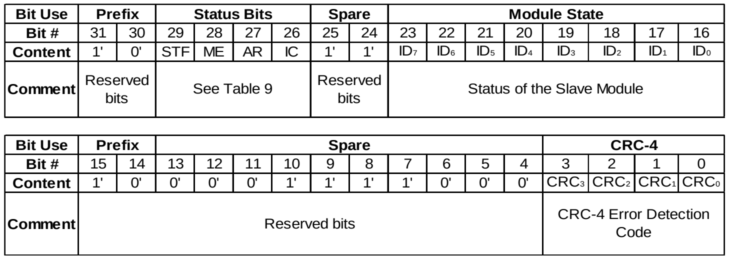
Command Token bit fields



Bit Use	Prefix		Cmd Code						Spare		Message Length					
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Content	0'	1'	C_5	C_4	C_3	C_2	C_1	C_0	1'	1'	L_5	L_4	L_3	L_2	L_1	L_0
Comment	Reserved bits		See Table 7						Reserved bits		Number of Data Words transferred after the Command Token, i.e. Payload Words (See Table 4)					

Bit Use	Prefix		Sub-address								Spare		CRC-4			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	0'	1'	SA_7	SA_6	SA_5	SA_4	SA_3	SA_2	SA_1	SA_0	'1'	'1'	CRC_3	CRC_2	CRC_1	CRC_0
Comment	Reserved bits		See Table 7								Reserved bits		CRC-4 Error Detection Code			

Response Token bit fields

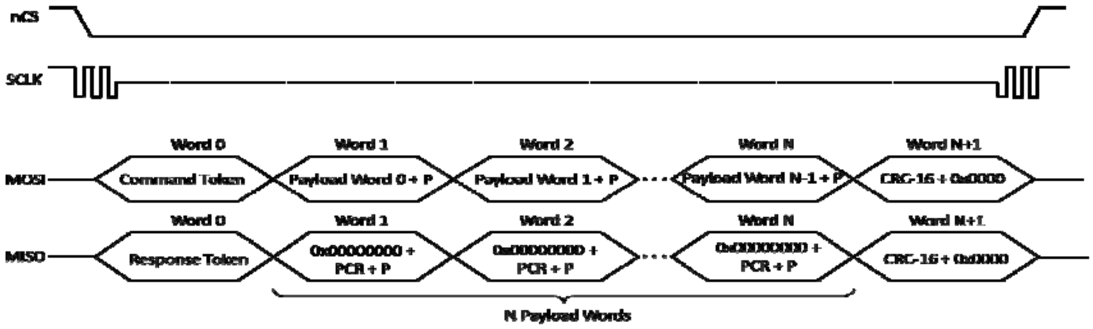


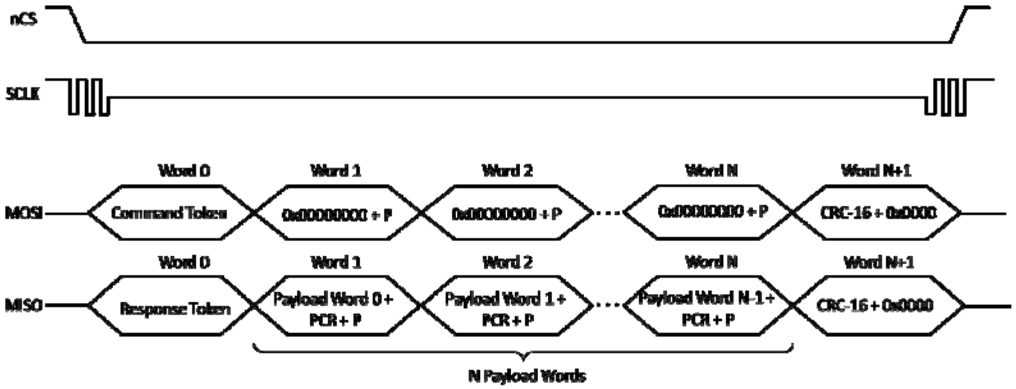
Bit Use	Prefix		Status Bits				Spare		Module State							
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Content	1'	0'	STF	ME	AR	IC	1'	1'	ID_7	ID_6	ID_5	ID_4	ID_3	ID_2	ID_1	ID_0
Comment	Reserved bits		See Table 9				Reserved bits		Status of the Slave Module							

Bit Use	Prefix		Spare										CRC-4			
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Content	1'	0'	0'	0'	0'	1'	1'	1'	1'	0'	0'	0'	CRC_3	CRC_2	CRC_1	CRC_0
Comment	Reserved bits												CRC-4 Error Detection Code			

SPI Protocol Specification : protocol layer SPI2

SPI2 example of Command Code WRITE





SPI2 example of Command Code READ

Table of contents

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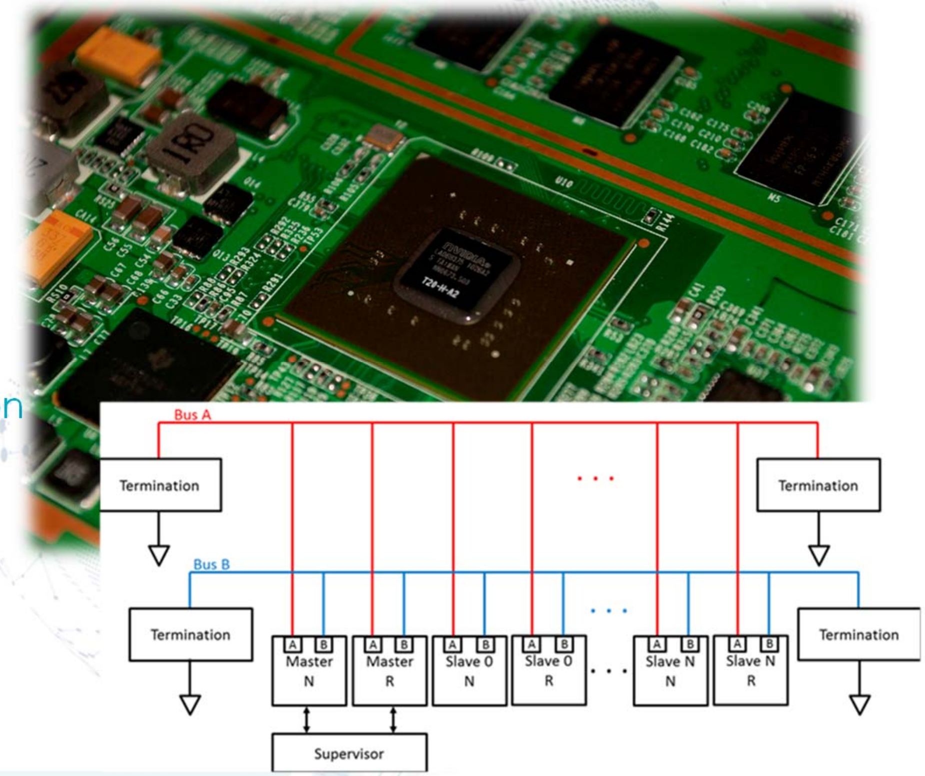


Demonstrator Requirements

Electrical Verification

- Compare simulations and physical implementation data of
  - bus (LVCMOS)
  - point to point topologies (LVDS)

Protocol Verification

- SPI protocol variants (SPI0/1/2)
- Configuration modes 1 & 3
- IP core
- Communication with COTS devices
- SPI Flash application
- FPGA dynamic reconfiguration
- Simulation of SPI-based High Priority Command (ECSS-14C) interfaces

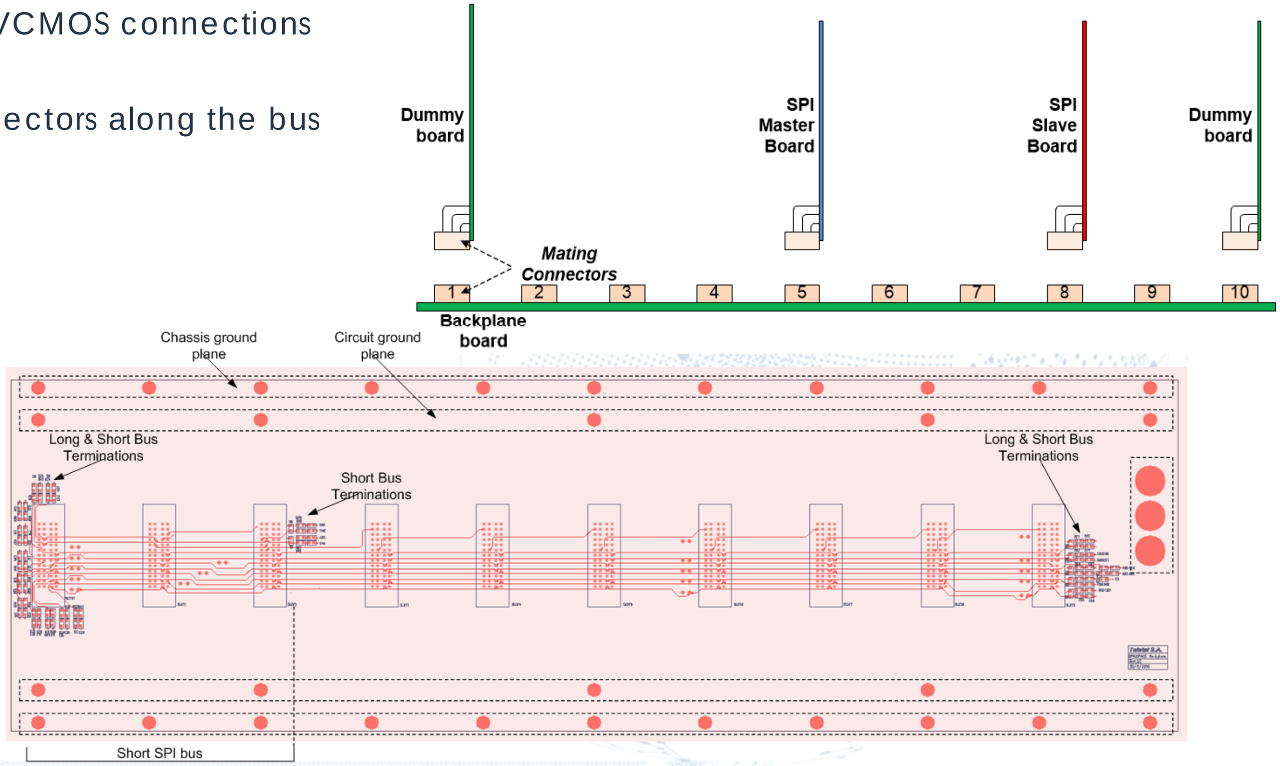
SPI Demonstrator – Overall Design

Backplane architecture for LVCMOS connections

Boards plugged on any connectors along the bus

Board types:

- Master board
- Slave board
- Dummy load board



SPI Demonstrator – Master/Slave Design

FPGA-based board

- SPI Master/Slave
- Applications
- SpW/RMAP for remote commanding

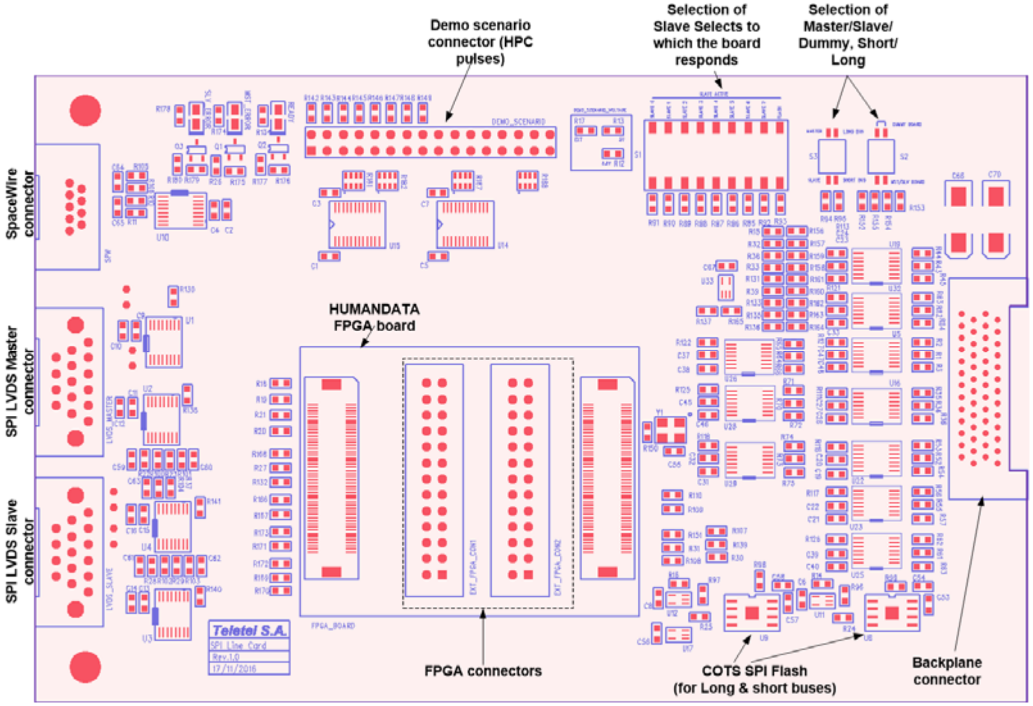
SPI LVCMOS Interface

SPI LVDS Interface

Demo Scenario connector

SPI flash memory

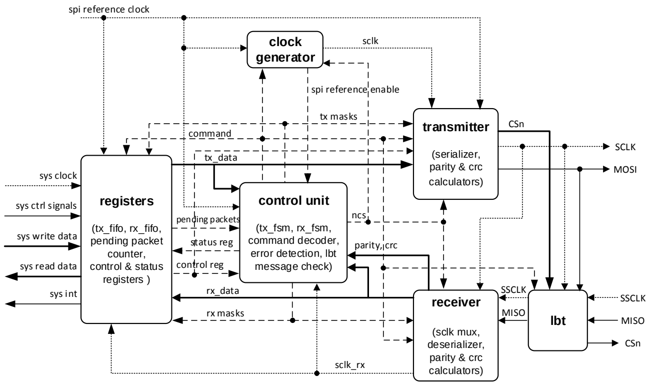
Configuration switches (DIP switches for Master/Slave selection, Slave Selects allocation etc.)


Demo scenario connector (HPC pulses)
Selection of Slave Selects to which the board responds
Selection of Master/Slave/ Dummy, Short/ Long
SpaceWire connector
SPI LVDS Master connector
SPI LVDS Slave connector
HUMANDATA FPGA board
Teletel S.A.
SPI Line Card
Rev.1.0
17/11/2016
FPGA_BOARD
FPGA connectors
COTS SPI Flash (for Long & short buses)
Backplane connector

SPI Demonstrator – Master/Slave Design

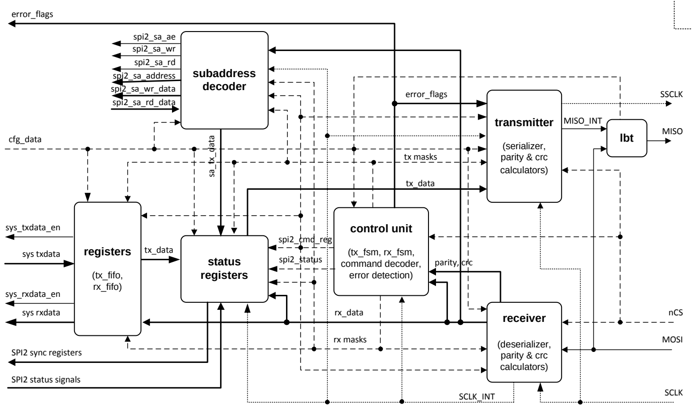
MASTER:

- SPI Handling up to 32 slaves
- Simultaneous support of SPI-0/1/2, Configurations 1/2/3
- Message length up to 256 bytes
- Command parameters in the command structure (Transaction length, SCLK frequency, protocol version, configuration, …)
- Loopback (near/far end)



SLAVE:

- Static configuration
- SPI-0/1/2
- Word width
- Message length



LVDS & LVCMOS

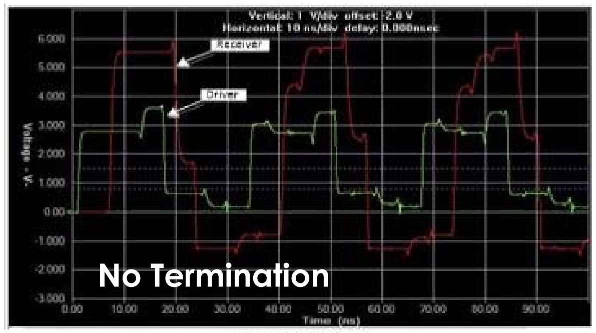
LVDS implementation is point to point and SpW-like. Signal integrity problems not foreseen.

LVCMOS for multipoint connections.

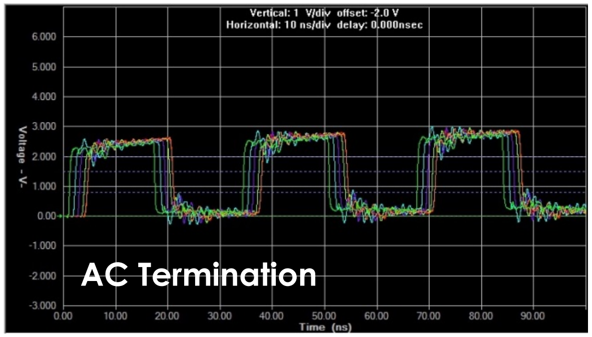
Long bus & fast rise/fall times likely to result in signal integrity issues.

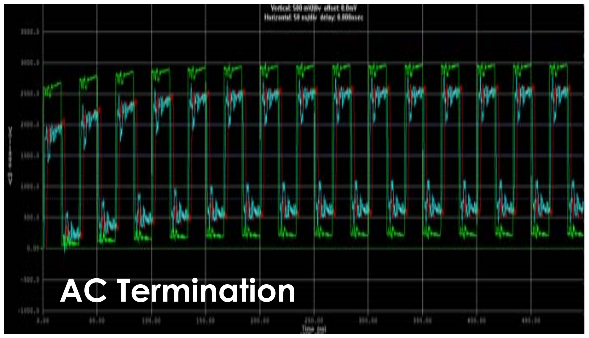
LVCMOS Termination	Candidate ?
No termination	√
Series	√
Parallel	X A termination of between 75 and 120 Ohms draws too much driver current
AC	√
Thevenin	X Will permanently bias the signal at the receiver
Thevenin with capacitor on “low leg”	√
Thevenin with capacitors on both legs	√

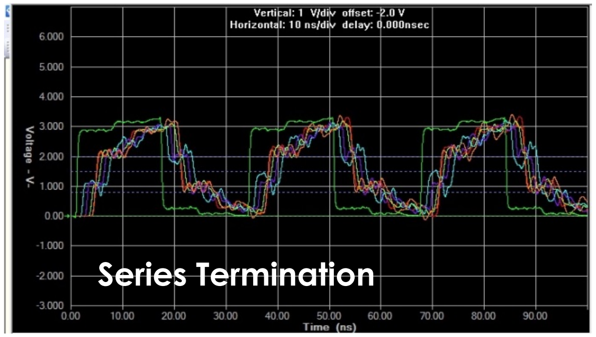
LVCMOS – Termination trade-off

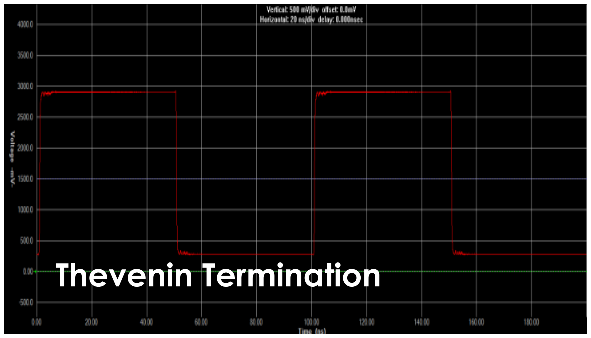

No Termination

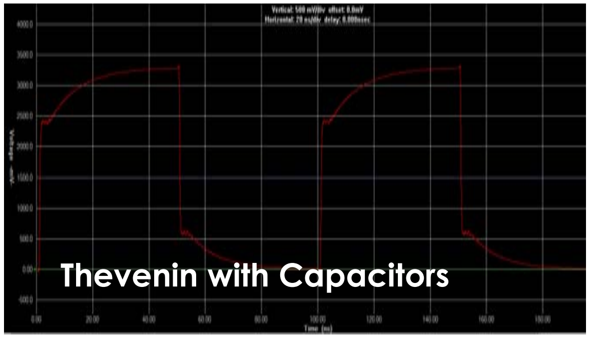
Voltage waveform


AC Termination


AC Termination


Series Termination


Thevenin Termination


Thevenin with Capacitors

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LVCMOS – Termination Summary

	Bus edge					
	No termination	Series Termination	AC Termination	***Thevenin (Reference)***	Thevenin with one Capacitor	Thevenin with two Capacitors
Signal quality (Reflections)	Unacceptable	Unacceptable	Good	*Best*	Good	Good
Voltage at the receiver	Doubles	Depends on distance from bus edge	Good	*Swing less than full*	Good	Good
Driver current	Within limits	Good	Within limits, gets better with damping resistor	*Within limits, but has constant DC consumption*	Good on IDLE, within limits when driver = 0	Best
Swing	Outside IC limits	Full	Vcc ok, Does not reach GND	*Not full swing*	Vcc ok, Does not reach GND	Full

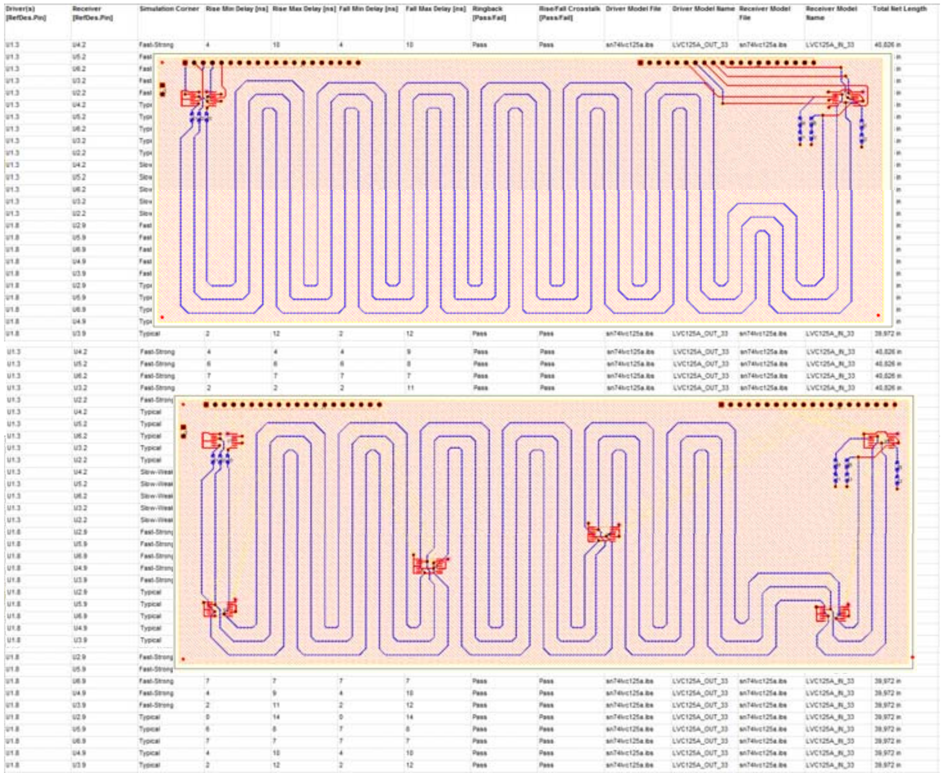
Crosstalk analysis

Inputs:

- Initial requirement for 1 m backplane bus, later reduced to 47 cm backplane (Modular RTU)
- Requirement for -30dB between nets (SPI4SPACE specification)

Analysis:

- Crosstalk analysis to define minimum distance between signal traces
- Crosstalk threshold 100mV
- Backplane nets length 1 meter
- Single/multiple receivers
- Driver on bus edge/bus middle

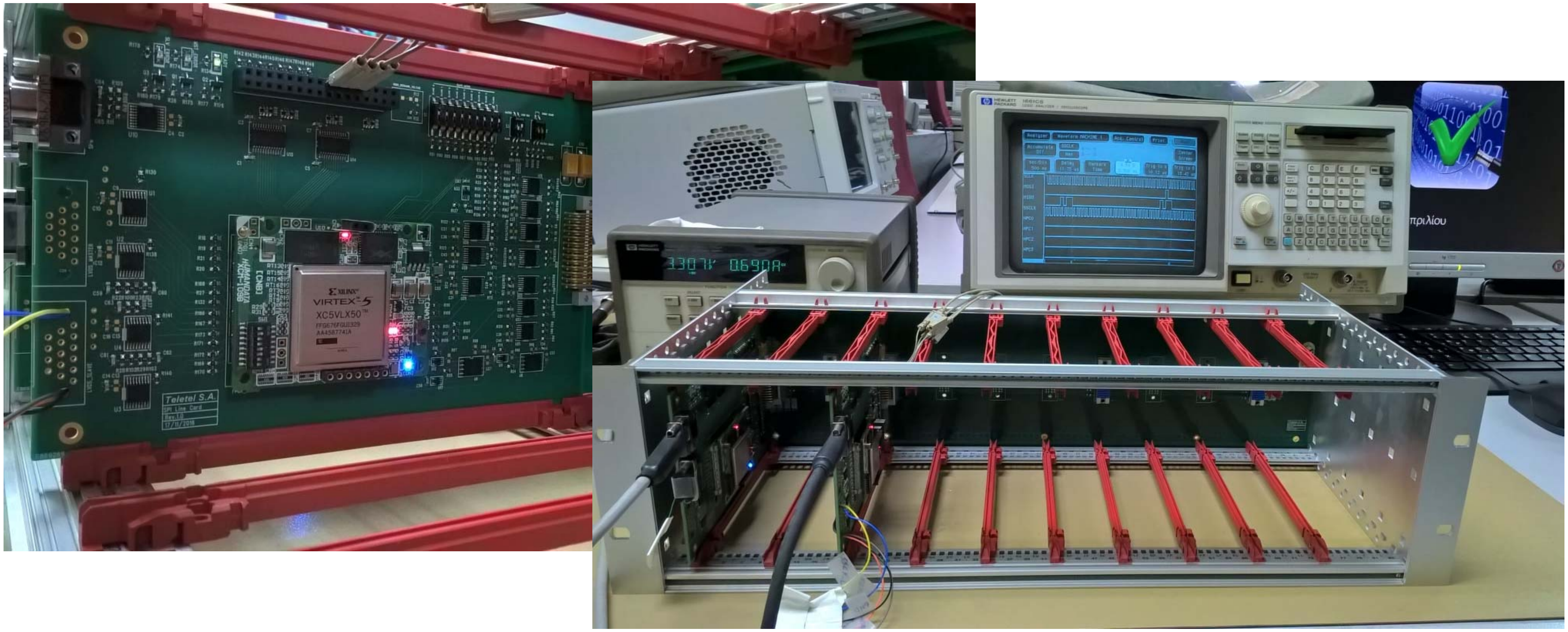


Driver(s) [RefDes.Pin]	Receiver [RefDes.Pin]	Simulation Corner	Rise Min Delay [ns]	Rise Max Delay [ns]	Fall Min Delay [ns]	Fall Max Delay [ns]	Ringback [Pass/Fail]	Rise/Fall Crosstalk [Pass/Fail]	Driver Model File	Driver Model Name	Receiver Model File	Receiver Model Name	Total Net Length
U1.3	U4.2	Fast-Strong	4	10	4	10	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	40.826 in
U1.3	U5.2	Fast											in
U1.3	U6.2	Fast											in
U1.3	U3.2	Fast											in
U1.3	U2.2	Fast											in
U1.3	U4.2	Typ											in
U1.3	U5.2	Typ											in
U1.3	U6.2	Typ											in
U1.3	U3.2	Typ											in
U1.3	U2.2	Typ											in
U1.3	U4.2	Slow											in
U1.3	U5.2	Slow											in
U1.3	U6.2	Slow											in
U1.3	U3.2	Slow											in
U1.3	U2.2	Slow											in
U1.8	U2.9	Fast											in
U1.8	U5.9	Fast											in
U1.8	U6.9	Fast											in
U1.8	U4.9	Fast											in
U1.8	U3.9	Fast											in
U1.8	U2.9	Typ											in
U1.8	U5.9	Typ											in
U1.8	U6.9	Typ											in
U1.8	U4.9	Typ											in
U1.8	U3.9	Typical	2	12	2	12	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	39.972 in
U1.3	U4.2	Fast-Strong	4	4	4	9	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	40.826 in
U1.3	U5.2	Fast-Strong	6	6	6	8	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	40.826 in
U1.3	U6.2	Fast-Strong	7	7	7	7	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	40.826 in
U1.3	U3.2	Fast-Strong	2	2	2	11	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	40.826 in
U1.3	U2.2	Fast-Strong											
U1.3	U4.2	Typical											
U1.3	U5.2	Typical											
U1.3	U6.2	Typical											
U1.3	U3.2	Typical											
U1.3	U2.2	Typical											
U1.3	U4.2	Slow-Weak											
U1.3	U5.2	Slow-Weak											
U1.3	U6.2	Slow-Weak											
U1.3	U3.2	Slow-Weak											
U1.3	U2.2	Slow-Weak											
U1.8	U2.9	Fast-Strong											
U1.8	U5.9	Fast-Strong											
U1.8	U6.9	Fast-Strong											
U1.8	U4.9	Fast-Strong											
U1.8	U3.9	Fast-Strong											
U1.8	U2.9	Typical											
U1.8	U5.9	Typical											
U1.8	U6.9	Typical											
U1.8	U4.9	Typical											
U1.8	U3.9	Typical											
U1.8	U2.9	Fast-Strong											
U1.8	U5.9	Fast-Strong											
U1.8	U6.9	Fast-Strong	7	7	7	7	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	39.972 in
U1.8	U4.9	Fast-Strong	4	9	4	10	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	39.972 in
U1.8	U3.9	Fast-Strong	2	11	2	12	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	39.972 in
U1.8	U2.9	Typical	0	14	0	14	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	39.972 in
U1.8	U5.9	Typical	6	8	7	8	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	39.972 in
U1.8	U6.9	Typical	7	7	7	7	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	39.972 in
U1.8	U4.9	Typical	4	10	4	10	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	39.972 in
U1.8	U3.9	Typical	2	12	2	12	Pass	Pass	sn74lvc125a.ibs	LVC125A_OUT_33	sn74lvc125a.ibs	LVC125A_IN_33	39.972 in

Crosstalk analysis – Results

Configuration	Series Termination	RC Termination	RC Termination with damping resistor
#1. Single driver, 1 receiver, 150 mils clearance, driver at the edge of the bus	PASS	PASS	PASS
#2. Single driver, 5 receivers,150 mils clearance, driver at the edge of the bus	PASS	PASS	PASS
#3. Single driver, 5 receivers, 150 mils clearance, driver in the middle of the bus	PASS	PASS	PASS
#4. Single driver, 5 receivers, 100 mils clearance with guard traces, routed in striplines, driver at the edge of the bus	PASS	PASS	PASS

SPI Demonstrator - Verification

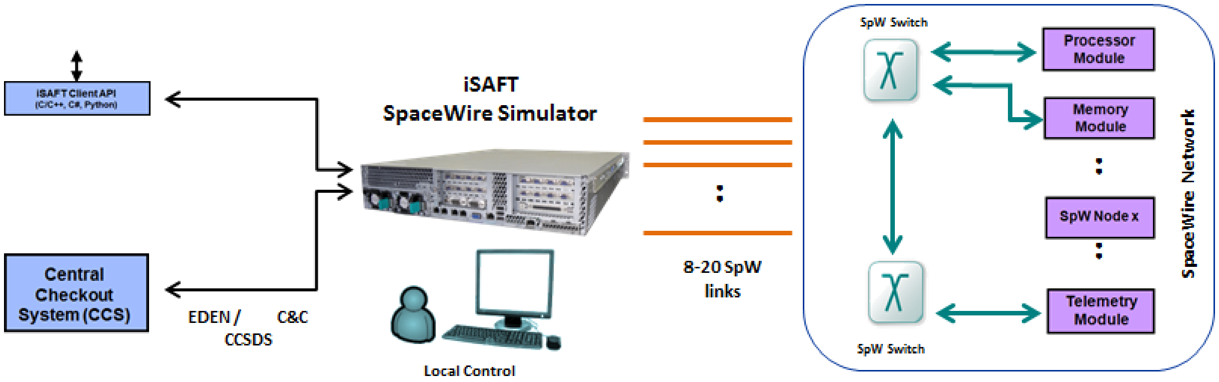


iSAFT SpaceWire Simulator

Advanced EGSE platform with traffic generation capabilities that simulates SpaceWire devices or instruments, enabling S/C integration tests before the availability of Flight Models.

Provides an 8 – 20 port SpaceWire interface with advanced traffic generation and asynchronous transmission capabilities.

Suitable for the verification of new protocols and protocol variations.



Data Bus Front End

Instrument Simulation

OBC Simulation (PLM EGSE)

Suitable for various EGSEs

AIT/AIV, FMEA, CE

SPI FPGA

Control through SpW/RMAP

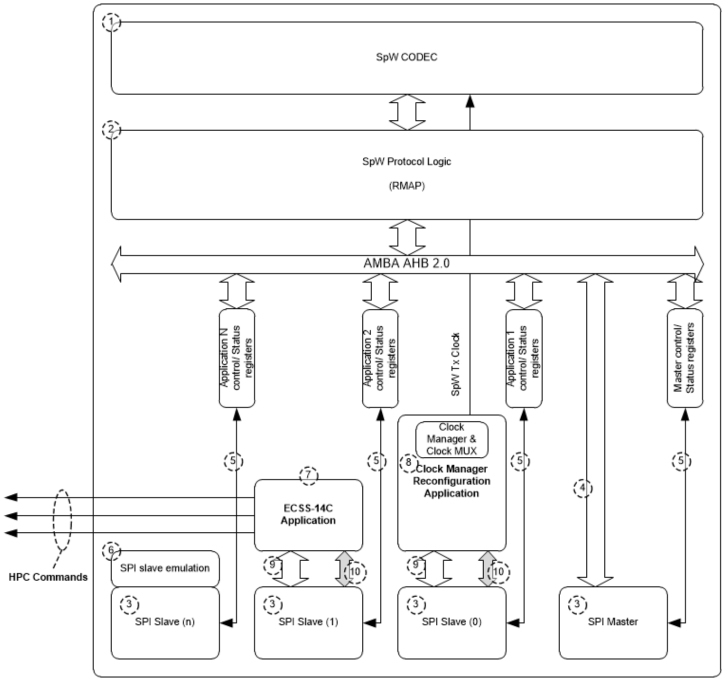
SPI Master/Slave Core

AMBA AHB 2.0

ECSS-14C, FPGA dynamic reconfiguration, Register file applications (accessed through SPI0/1/2

Demo applications:

- Access to COTS SPI Memory (SPI-0)
- FPGA Dynamic Reconfiguration (SPI-1)
- Asynchronous/Scheduled HPC generation (SPI-2)
- Register File (SPI-0/1/2)


1
SpW CODEC
2
SpW Protocol Logic
(RMAP)
AMBA AHB 2.0
Application N control/ Status registers
Application 2 control/ Status registers
SpW Tx Clock
Application 1 control/ Status registers
Master control/ Status registers
5
5
5
5
4
7
ECSS-14C Application
Clock Manager & Clock MUX
8
Clock Manager Reconfiguration Application
HPC Commands
6
SPI slave emulation
9
10
9
10
3
SPI Slave (n)
3
SPI Slave (1)
3
SPI Slave (0)
3
SPI Master

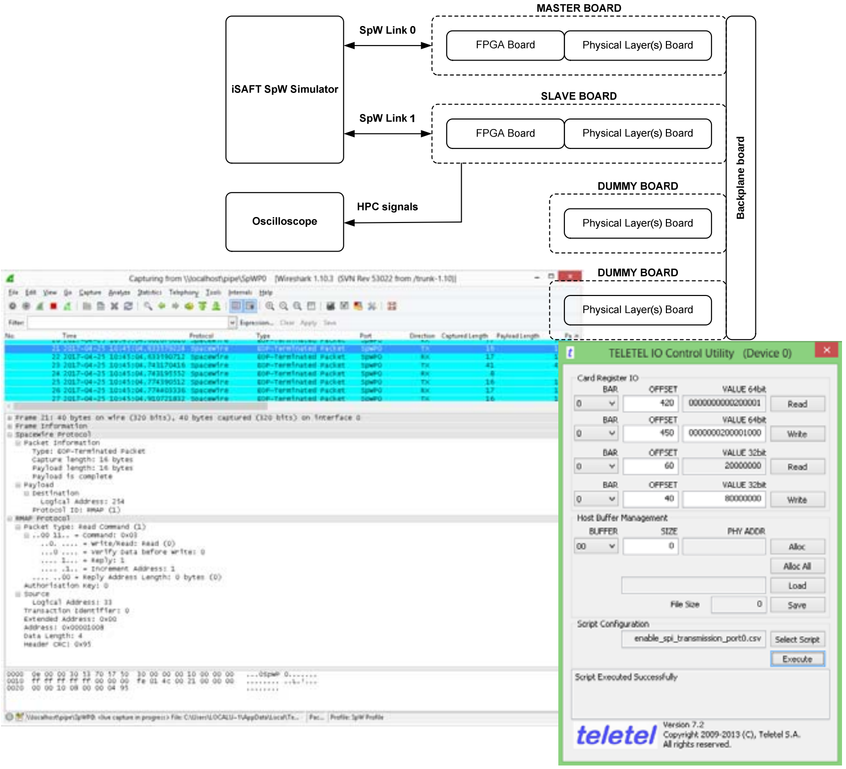
Verification tests

Electrical Verification:

- Verification of Thevenin and Thevenin with capacitors
- Short/Long bus tests
- Verification of SS/SCLK/SSCLK timings
- Measurement of PCB/IC delays

Functional/Performance verification:

- RMAP controlled FPGA
- Incremental verification – tests initially performed with low level SW
- Verification with different SCLK frequencies
- Configurations 1/2/3
- SPI SCLK/SSCLK 100 KHz - 30 MHz



Capturing from \\localhost\pipe\SpWP0 [Wireshark 1.10.3 (SVN Rev 53022 from /trunk-1.10)]

```
No.  Time                           Protocol    Type                  Port   Direction  Captured Length
21 2017-04-25 10:45:04.633179034  Spacewire   EOP-Terminated Packet  SpWP0  TX         16
22 2017-04-25 10:45:04.633190712  Spacewire   EOP-Terminated Packet  SpWP0  RX         17
23 2017-04-25 10:45:04.743170416  Spacewire   EOP-Terminated Packet  SpWP0  TX         41
24 2017-04-25 10:45:04.743195552  Spacewire   EOP-Terminated Packet  SpWP0  RX         8
25 2017-04-25 10:45:04.774390512  Spacewire   EOP-Terminated Packet  SpWP0  TX         16
26 2017-04-25 10:45:04.774403336  Spacewire   EOP-Terminated Packet  SpWP0  RX         17
27 2017-04-25 10:45:04.910721832  Spacewire   EOP-Terminated Packet  SpWP0  TX         16

⊞ Frame 21: 40 bytes on wire (320 bits), 40 bytes captured (320 bits) on interface 0
⊞ Frame Information
⊟ Spacewire Protocol
  ⊟ Packet Information
      Type: EOP-Terminated Packet
      Capture length: 16 bytes
      Payload length: 16 bytes
      Payload is complete
  ⊟ Payload
    ⊟ Destination
        Logical Address: 254
      Protocol ID: RMAP (1)
⊟ RMAP Protocol
  ⊟ Packet type: Read Command (1)
    ⊟ ..00 11.. = Command: 0x03
        ..0. .... = Write/Read: Read (0)
        ...0 .... = Verify Data before write: 0
        .... 1... = Reply: 1
        .... .1.. = Increment Address: 1
      .... ..00 = Reply Address Length: 0 bytes (0)
    Authorisation Key: 0
  ⊟ Source
      Logical Address: 33
    Transaction Identifier: 0
    Extended Address: 0x00
    Address: 0x00001008
    Data Length: 4
    Header CRC: 0x95

0000  0e 00 00 30 33 70 57 50  30 00 00 00 10 00 00 00   ...03pWP 0.......
0010  ff ff ff ff ff 00 00 00  fe 01 4c 00 21 00 00 00   ........ ..L.!...
0020  00 00 10 08 00 00 04 95                            ........

\\localhost\pipe\SpWP0: <live capture in progress> File: C:\Users\LOCALU~1\AppData\Local\Te...  Pac...  Profile: SpW Profile
```

TELETEL IO Control Utility (Device 0)

Card Register IO

BAR	OFFSET	VALUE 64bit	
0	420	0000000000200001	Read
0	450	0000000200001000	Write

BAR	OFFSET	VALUE 32bit	
0	60	20000000	Read
0	40	80000000	Write

Host Buffer Management

BUFFER	SIZE	PHY ADDR
00	0	

File Size 0

Script Configuration

enable_spi_transmission_port0.csv

Script Executed Successfully

Version 7.2
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THALES ALENIA SPACE OPEN

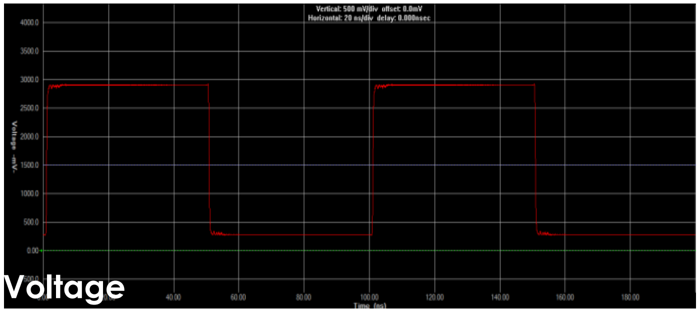
LVCMOS – Thevenin Termination

Measurements on all bus slots

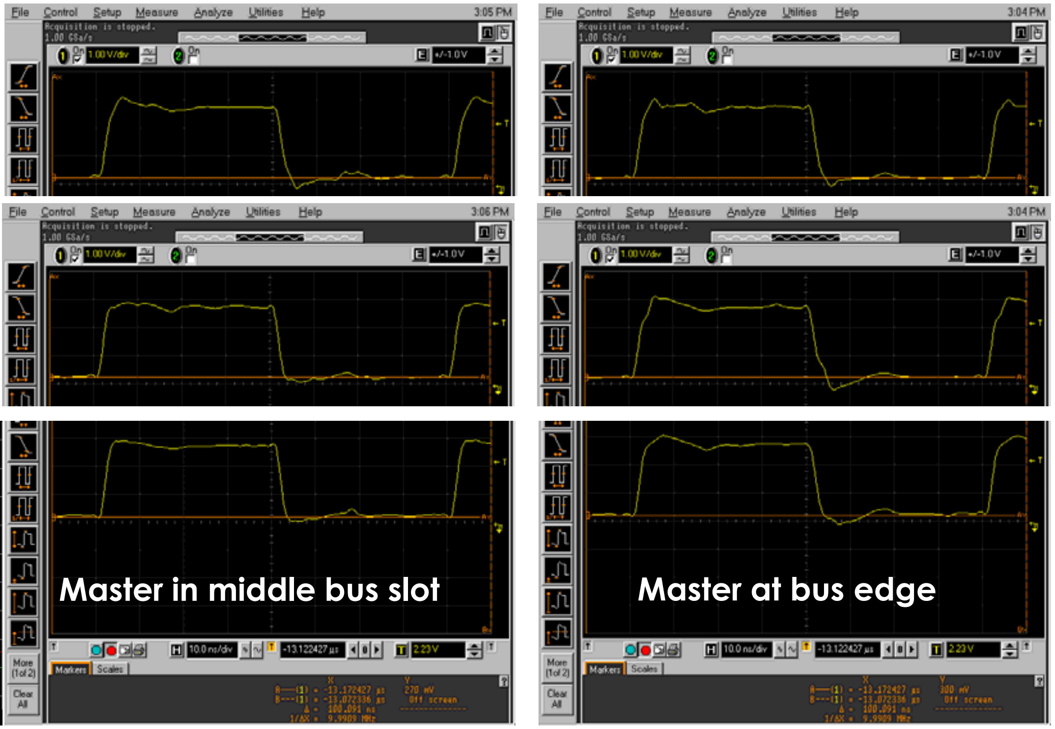
LVCMOS "Driver" board placed in different slots

Measurements with resistor values 150 – 200 Ohms (Z0 = 75 – 100 Ohms)

Results close to the simulated ones



Voltage



Master in middle bus slot

Master at bus edge

LVCMOS – Thevenin termination with capacitors

Thevenin Termination showed that 90 Ohms provides the best quality for the specific implementation

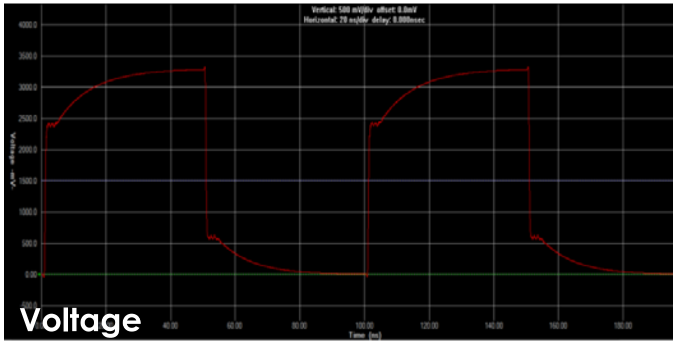
Full swing

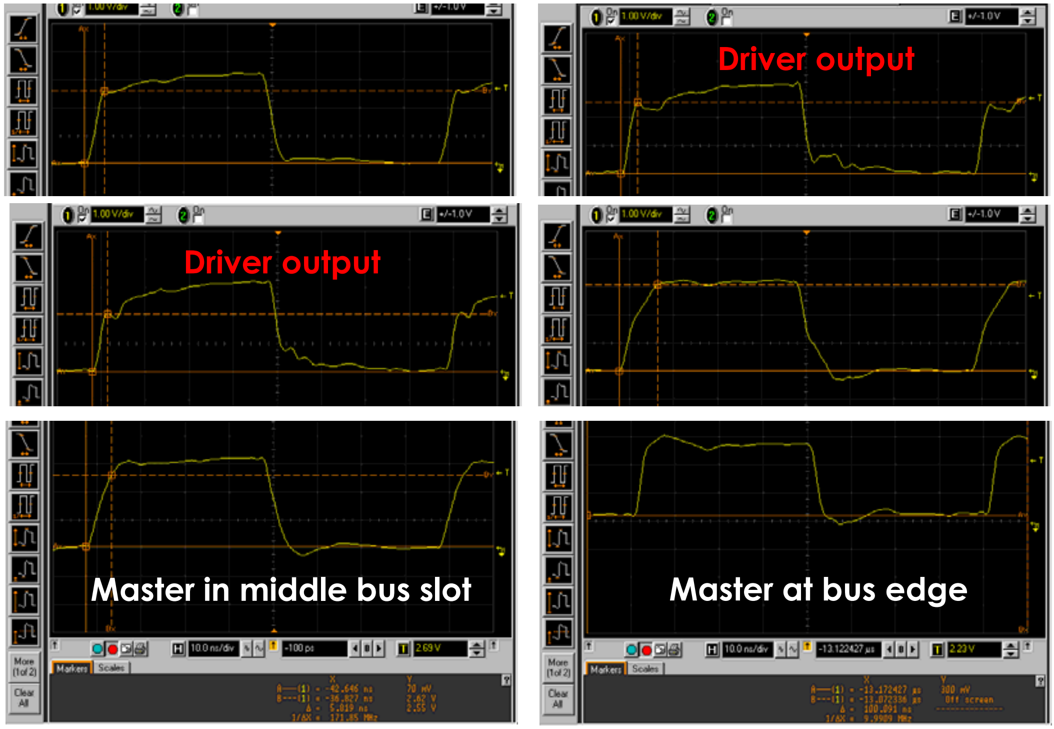
Capacitor smoothed transitions

No false transitions

Results close to the simulated ones

Distortion on each driver output (no effect)

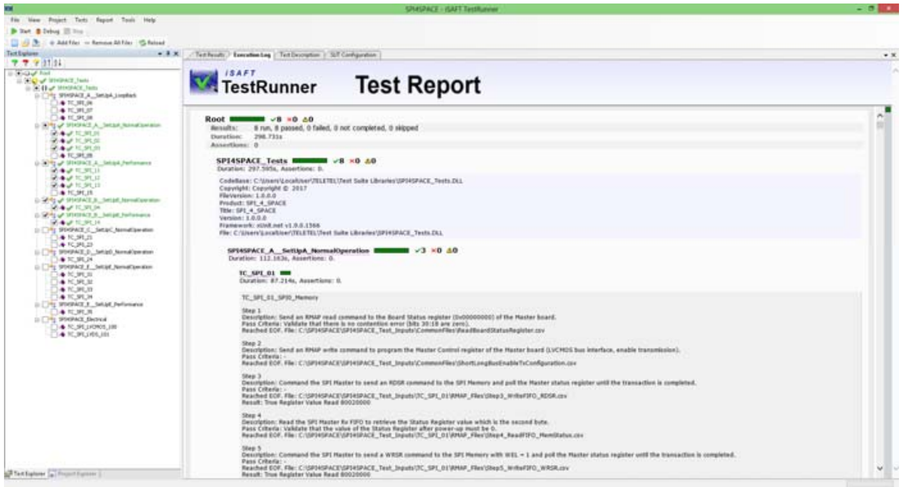




Demonstrator SW & Comments to the spec.

Demonstrator SW:

- Execution on iSAFT TestRunner
- 23 functional/performance Test Cases
- Test cases for all, except for 2, requirements
- Error injection tests:
  - SPI-0 used to generate erroneous SPI-1 commands
  - SPI-1 used to generate erroneous SPI-2 command

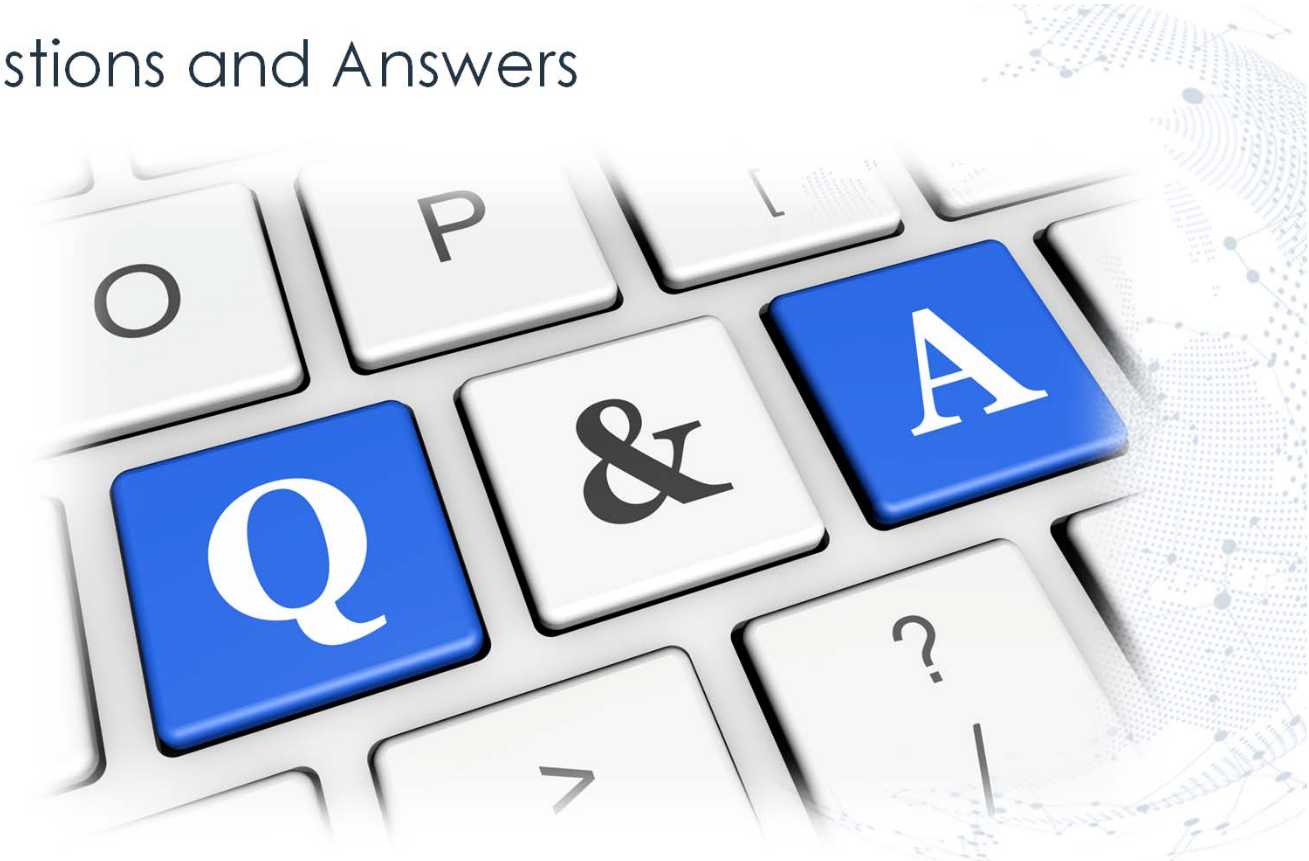


```
Root ✓8 ×0 ⚠0
  Results:    8 run, 8 passed, 0 failed, 0 not completed, 0 skipped
  Duration:   298.731s
  Assertions: 0

  SPI4SPACE_Tests ✓8 ×0 ⚠0
  Duration: 297.595s, Assertions: 0.

    CodeBase: C:\Users\LocalUser\TELETEL\Test Suite Libraries\SPI4SPACE_Tests.DLL
    Copyright: Copyright © 2017
    FileVersion: 1.0.0.0
    Product: SPI_4_SPACE
    Title: SPI_4_SPACE
    Version: 1.0.0.0
    Framework: xUnit.net v1.9.0.1566
    File: C:\Users\LocalUser\TELETEL\Test Suite Libraries\SPI4SPACE_Tests.DLL

    SPI4SPACE_A__SetUpA_NormalOperation ✓3 ×0 ⚠0
    Duration: 112.163s, Assertions: 0.

      TC_SPI_01
      Duration: 87.214s, Assertions: 0.

        TC_SPI_01_SPI0_Memory

        Step 1
        Description: Send an RMAP read command to the Board Status register (0x00000000) of the Master board.
        Pass Criteria: Validate that there is no contention error (bits 30:18 are zero).
        Reached EOF. File: C:\SPI4SPACE\SPI4SPACE_Test_Inputs\CommonFiles\ReadBoardStatusRegister.csv

        Step 2
        Description: Send an RMAP write command to program the Master Control register of the Master board (LVCMOS bus interface, enable transmission).
        Pass Criteria: -
        Reached EOF. File: C:\SPI4SPACE\SPI4SPACE_Test_Inputs\CommonFiles\ShortLongBusEnableTxConfiguration.csv

        Step 3
        Description: Command the SPI Master to send an RDSR command to the SPI Memory and poll the Master status register until the transaction is completed.
        Pass Criteria: -
        Reached EOF. File: C:\SPI4SPACE\SPI4SPACE_Test_Inputs\TC_SPI_01\RMAP_Files\Step3_WriteFIFO_RDSR.csv
        Result: True Register Value Read 80020000

        Step 4
        Description: Read the SPI Master Rx FIFO to retrieve the Status Register value which is the second byte.
        Pass Criteria: Validate that the value of the Status Register after power-up must be 0.
        Reached EOF. File: C:\SPI4SPACE\SPI4SPACE_Test_Inputs\TC_SPI_01\RMAP_Files\Step4_ReadFIFO_MemStatus.csv

        Step 5
        Description: Command the SPI Master to send a WRSR command to the SPI Memory with WEL = 1 and poll the Master status register until the transaction is completed.
        Pass Criteria: -
        Reached EOF. File: C:\SPI4SPACE\SPI4SPACE_Test_Inputs\TC_SPI_01\RMAP_Files\Step5_WriteFIFO_WRSR.csv
        Result: True Register Value Read 80020000
```

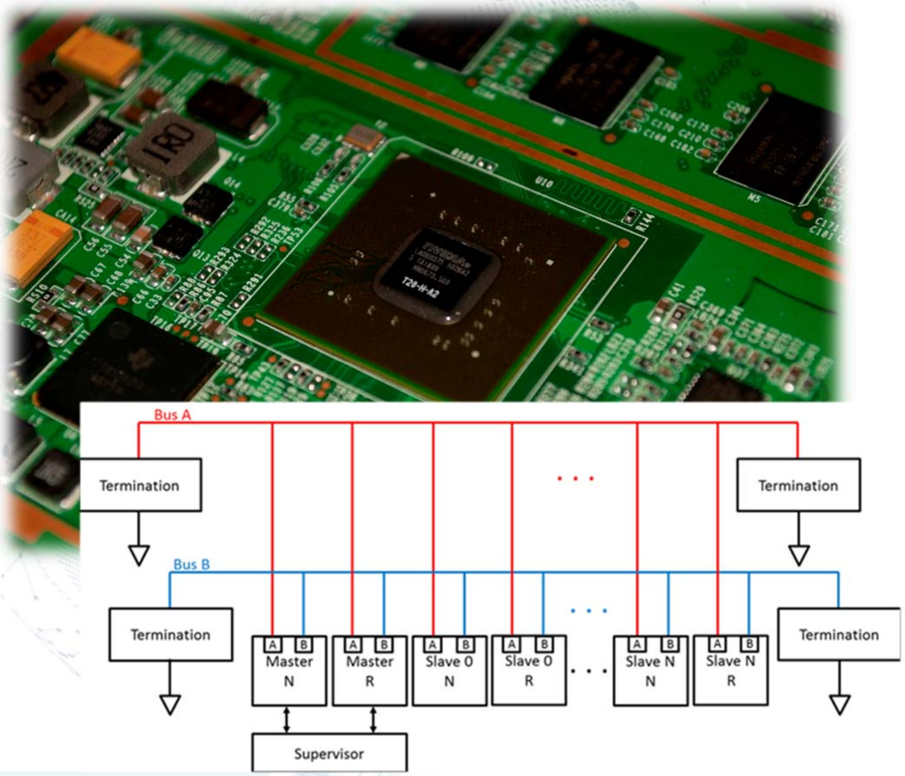
Results/comments:

- SPI in configuration 1 operates up to 10 MHz (~12 ns delay are only due to the LVCMOS ICs)
- SPI in configuration 3 operates up to 30 MHZ but it requires clock domain crossing. More clock cycles would ease synchronization
- Dead time needed between SS assertion and SCLK edges to ensure variations of the delays of the LVCMOS ICs & PCB tracks.

Questions and Answers



Back Up slides

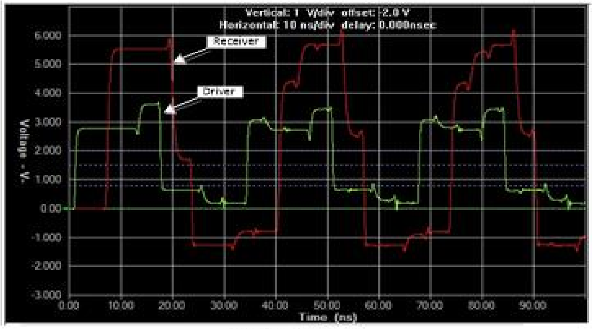


LVCMOS – No Termination

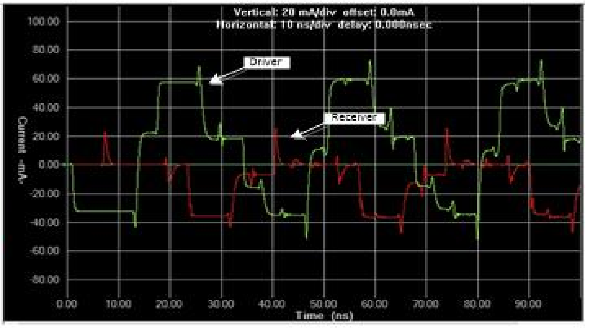
Unacceptable signal quality in unterminated bus

False transitions

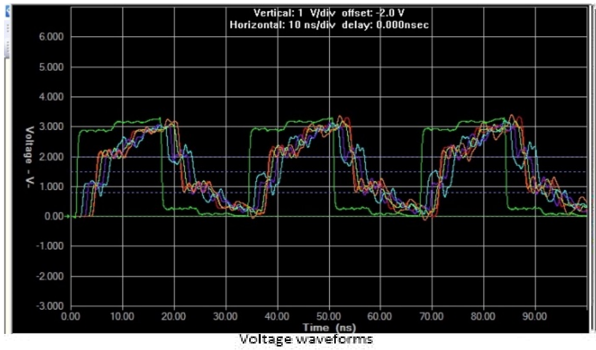
→ Voltage and current above IC maximum specifications



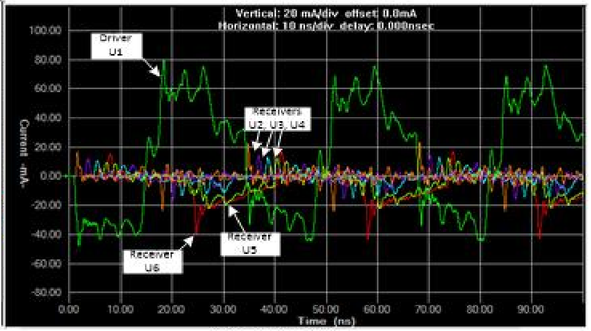
Voltage waveform



Current waveform



Voltage waveforms



Current waveforms

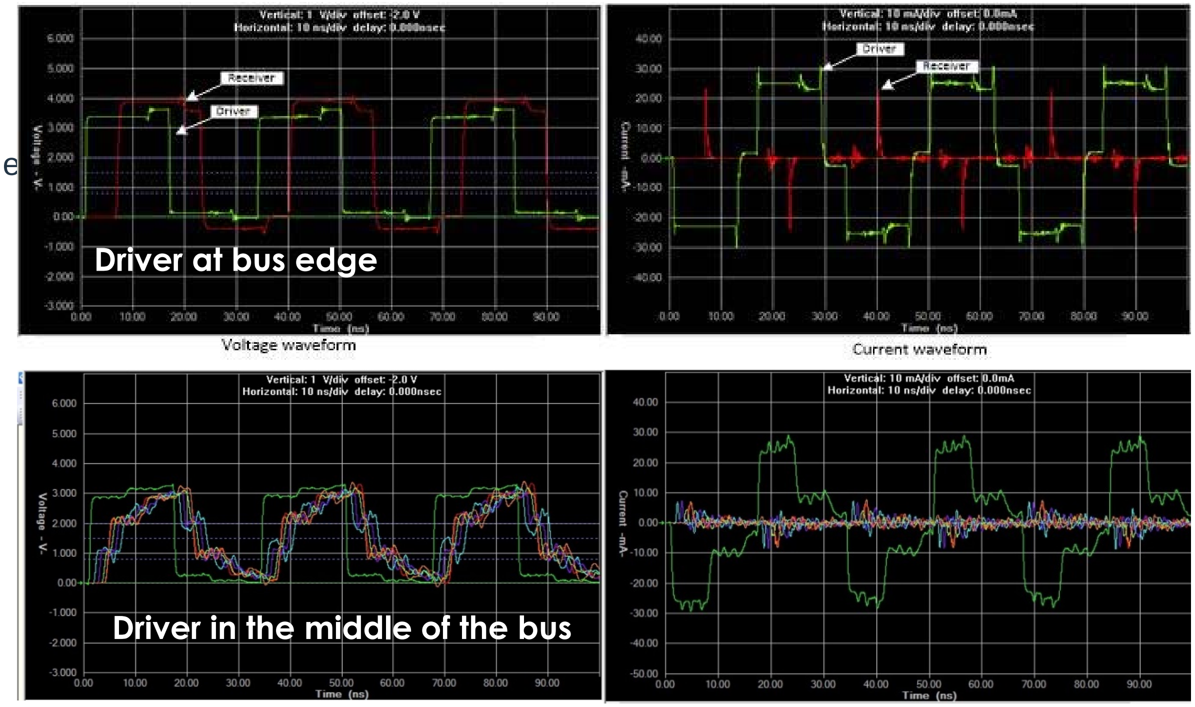
LVCMOS – Series Termination

Current is limited

Pulse shape better when the drive is at the edge of the bus (is it the Master ?)

Slave boards also drive the bus (MISO, SSCLK)

→ **Unsuitable**



Driver at bus edge

Voltage waveform

Current waveform

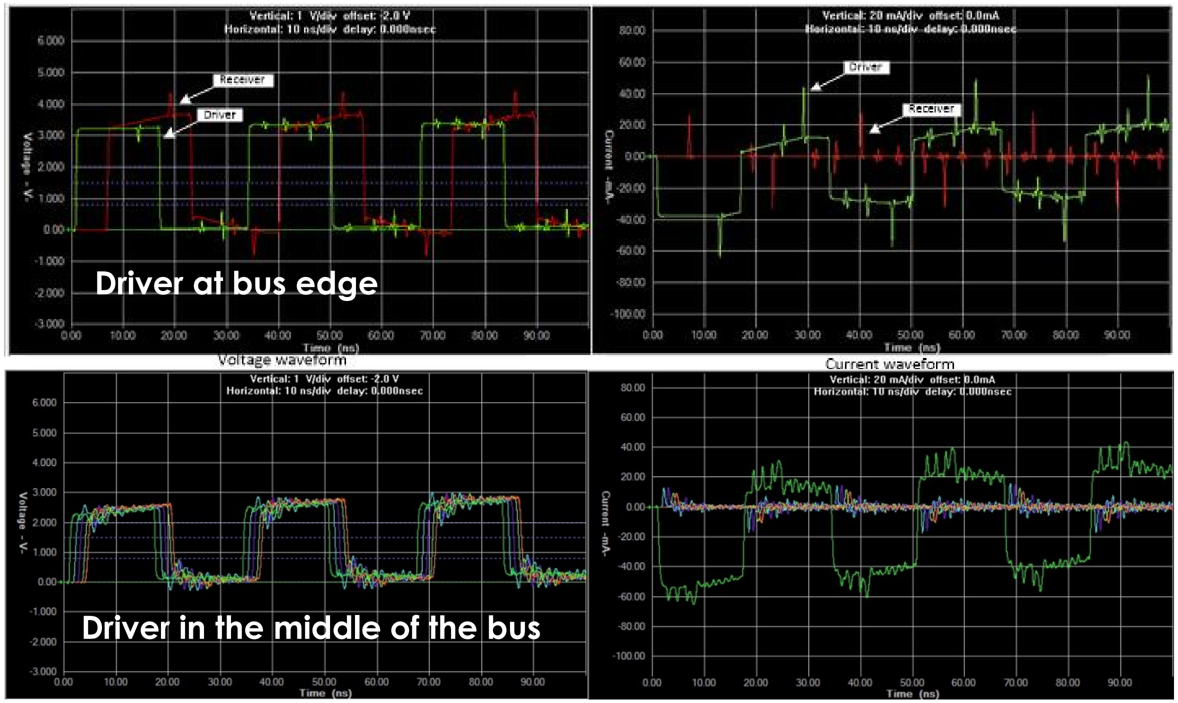
Driver in the middle of the bus

LVCMOS – AC Termination

Pulse shape is improved

No different voltage levels due to reflections

Damping resistor can limit further high current draw but creates resistor divider



Voltage waveform

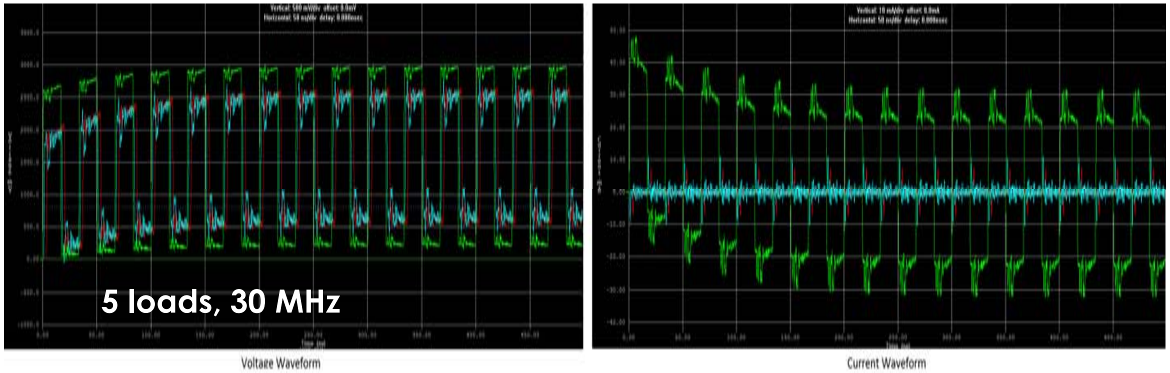
Current waveform

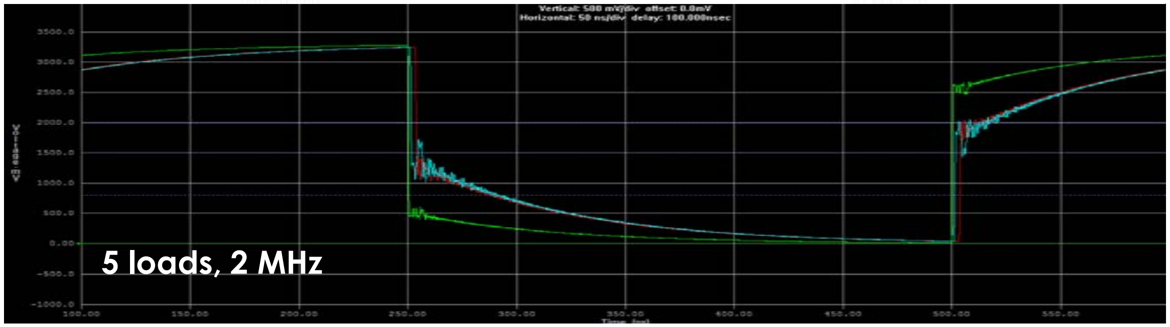
LVCMOS – AC Termination

DC offset due to capacitor charge - discharge

High driver current draw during the first pulses

→ Capacitor trimming required





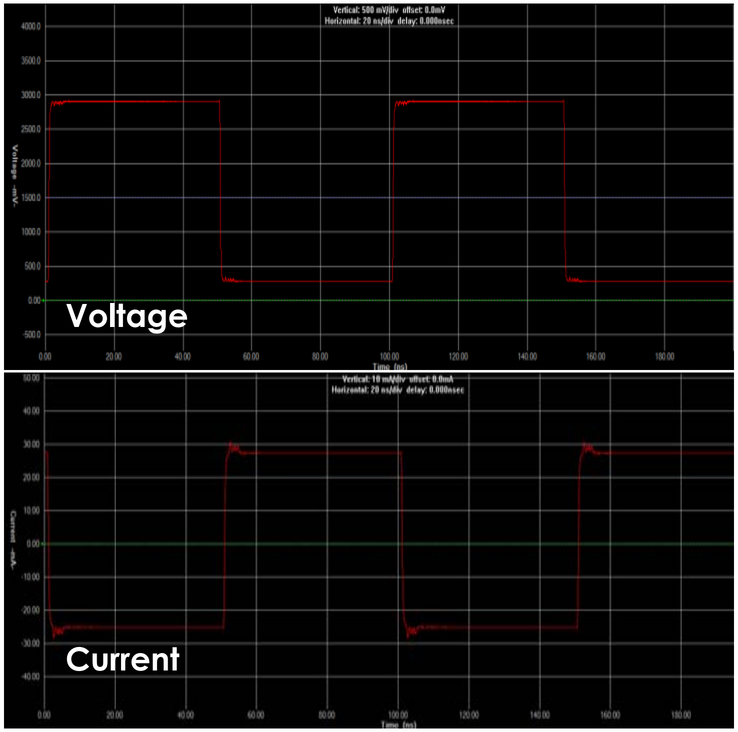
LVCMOS – Thevenin Termination

Originally not a candidate due to DC biasing

Used as reference for comparison of Thevenin-with-capacitors, termination resistors trimming

Provides a perfect pulse shape

Not full swing – inherent Thevenin limitation



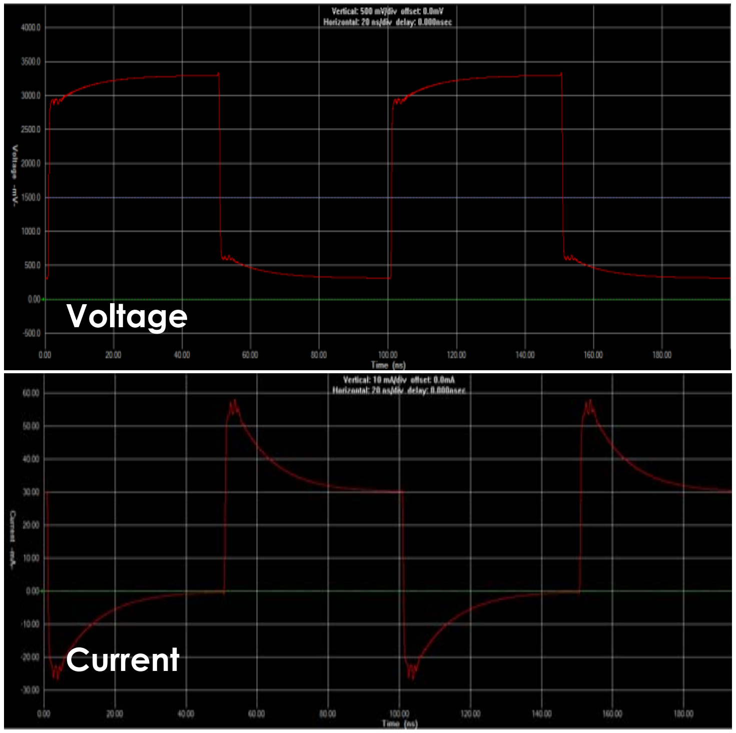
LVCMOS – Thevenin with capacitor on the “pull-down” leg

Capacitor stops DC consumption on idle

Switches up to Vcc but not GND

Capacitors smooths the rise/fall edges

Current momentarily exceeds datasheet max current*



* Communication with Texas Instruments confirmed that max current of 50 mA in the datasheet refers to DC consumption. The current can momentarily reach 250 mA if adequate decoupling is provided.

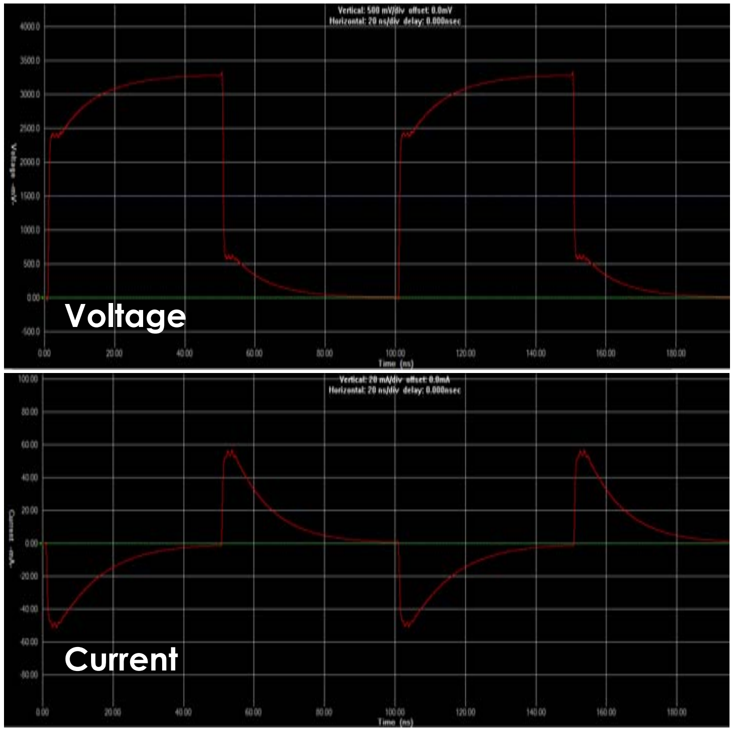
LVCMOS – Thevenin termination with capacitors

Capacitor stops DC consumption on idle

Switches up to Vcc and GND

Capacitors smoother even further

Current consumption below max datasheet level


Vertical: 500 mV/div offset: 0.0mV
Horizontal: 20 ns/div delay: 0.000nsec
Voltage -mV-
Voltage
Time (ns)
Vertical: 20 mA/div offset: 0.0mA
Horizontal: 20 ns/div delay: 0.000nsec
Current -mA-
Current
Time (ns)