OHB System AG
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SPACE SYSTEMS

Developing a SMP2 compliant Hardware-In-the-Loop simulation framework

We. Create. Space.

Introduction

- Previously
  - SMP2 Software Validation Facility for MTG
  - OHB's SMP2 simulation environment, Rufos
- Moving forward with SMP2 use
  - common base simulator for all new projects
- For a current project (SARah), a **Hardware-In-the-Loop (HIL)** Assembly, Integration & Verification simulator needed
- Development of **SMP2 simulation framework for HIL** simulator
- Allows **reuse of SMP2 models** between software and HIL simulator facilities

Brief refresher

Rufos

- OHB's own SMP2 simulation environment
- Initial development targeted **Linux OS**
- Python script interpreter
- Light-weight MMI

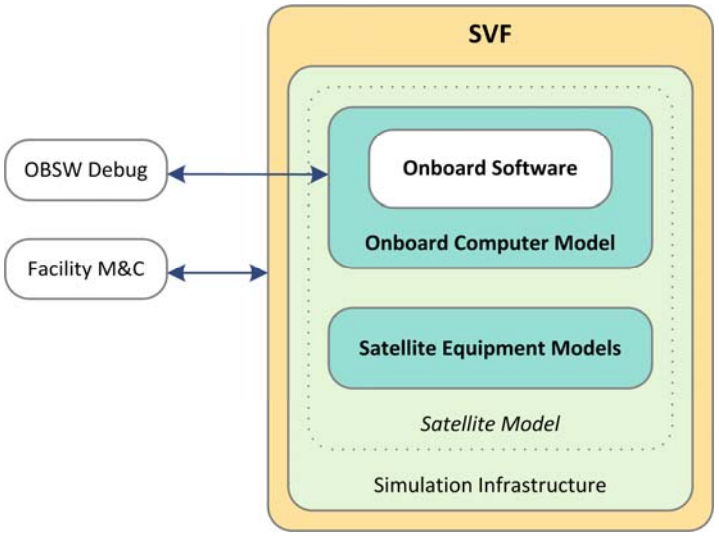
Simulator facilities

- **SVF**, Software Validation Facility: pure **software**
- **AIVS**, Assembly, Integration and Verification Simulator: **Hardware-In-the-Loop (HIL)**
- **TOMS**, Training, Operations and Maintenance Simulator: pure **software**

Simulator facilities: SVF/TOMS vs AIVS

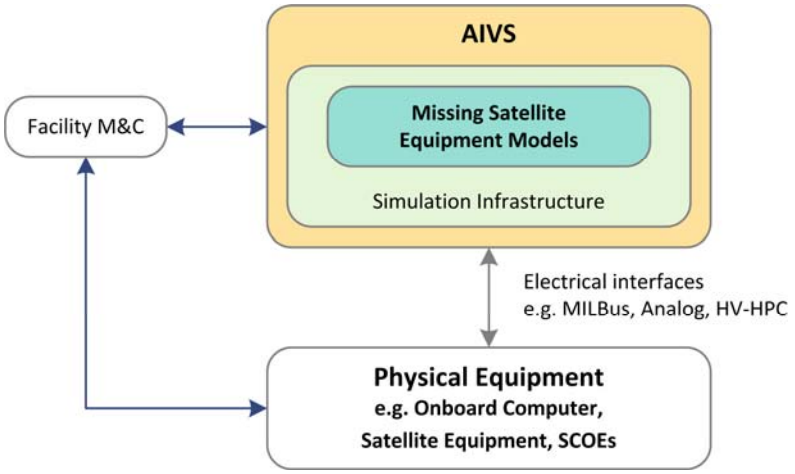
SVF/TOMS

- Simulates the whole satellite
- Simulation in software only



AIVS

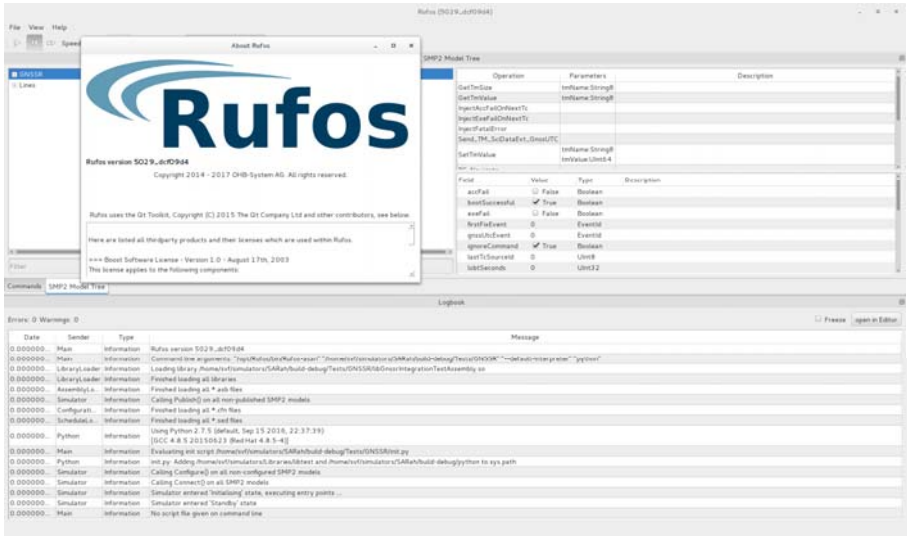
- Simulates only some equipment
- Hardware-In-the-Loop



Simulator facilities for OHB Project (SARah)

SVF

- Equipment models first use
- Uses Rufos



AIVS

- Hardware platform: dSPACE SCALEXIO

Photo: dSPACE

AIVS hardware platform: dSPACE SCALEXIO

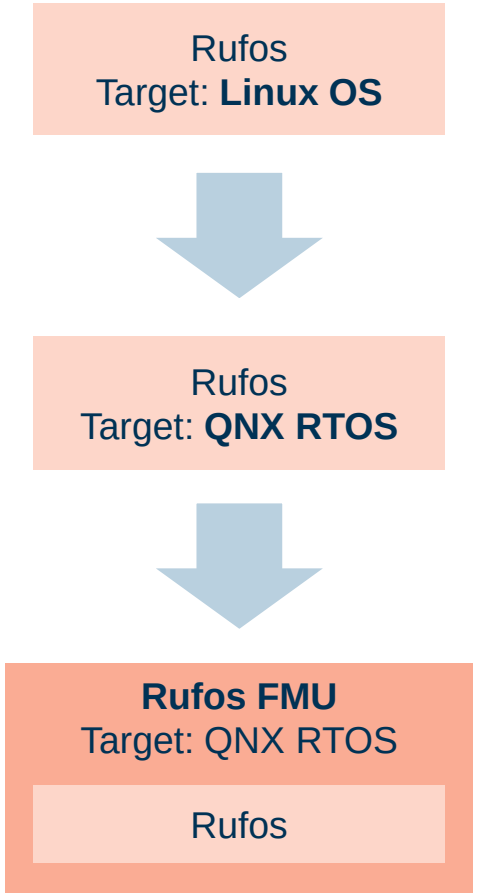
Components

- Processing unit with **QNX RTOS**
- I/O boards
- Other electronics

Interfaces

- Hardware interfaces built for SARah AIVS, include:
  - MILBus
  - RS422 UART
  - Analog signal I/O
  - Bi-level discrete I/O
  - HV-HPC
- No MMI
- Network
  - dSPACE software on external PC for development, monitoring and control

SMP2 simulation environment on SCALEXIO



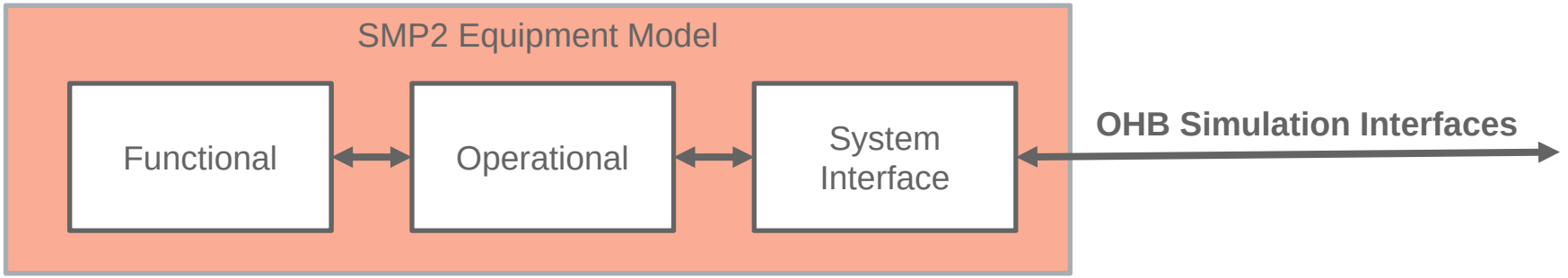
- Cross-compiled
- Ensured hard real-time performance
  - System calls with bounded execution time
  - Memory pools for dynamic allocation
- Removed MMI

- Wrapped with FMI standard
  - Supported by SCALEXIO software stack

Rufos (SMP2 simulation environment) running on SCALEXIO

SMP2 models of satellite equipment

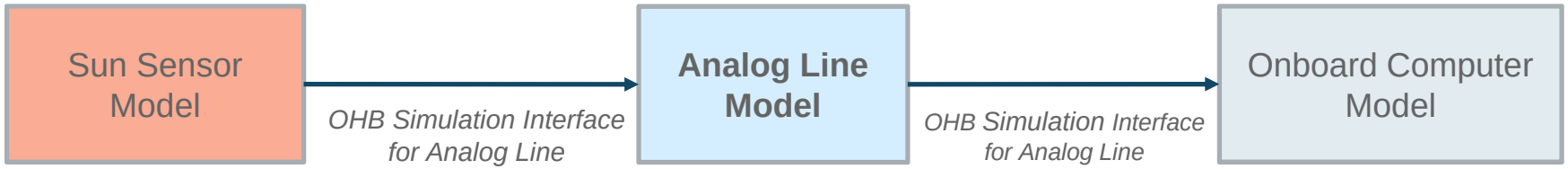
- Models have Functional, Operational and System Interface parts
- System Interface simulates electrical interfaces (e.g. MILBus, Analog I/O)
- System Interface uses **OHB Simulation Interfaces**
  - Collection of internal OHB standard C++ interfaces (e.g. IAnalogLine, IPulseLine)
- OHB Simulation Interfaces are comparable to SystemIF ports of Spacecraft Simulation Reference Architecture (SSRA)



Simulating electrical interfaces: SVF, TOMS

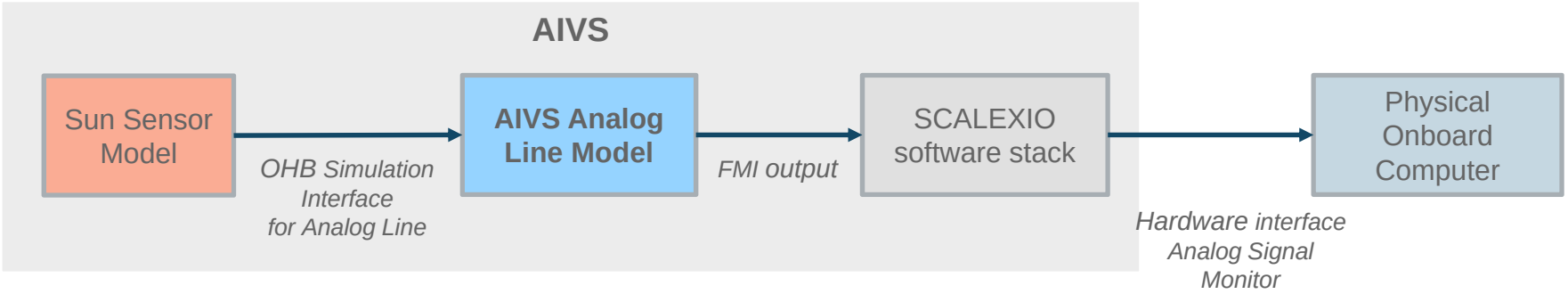
- Harness connections are simulated by **Line Models**
- Line Models have two ends: each can connect to another model, via an OHB Simulation Interface
- Line Model for each OHB Simulation Interface (e.g. Analog Line model, Pulse Line model) in the OHB Platform Library

- Example: Sun Sensor model, with an analog output connected to the Onboard Computer model

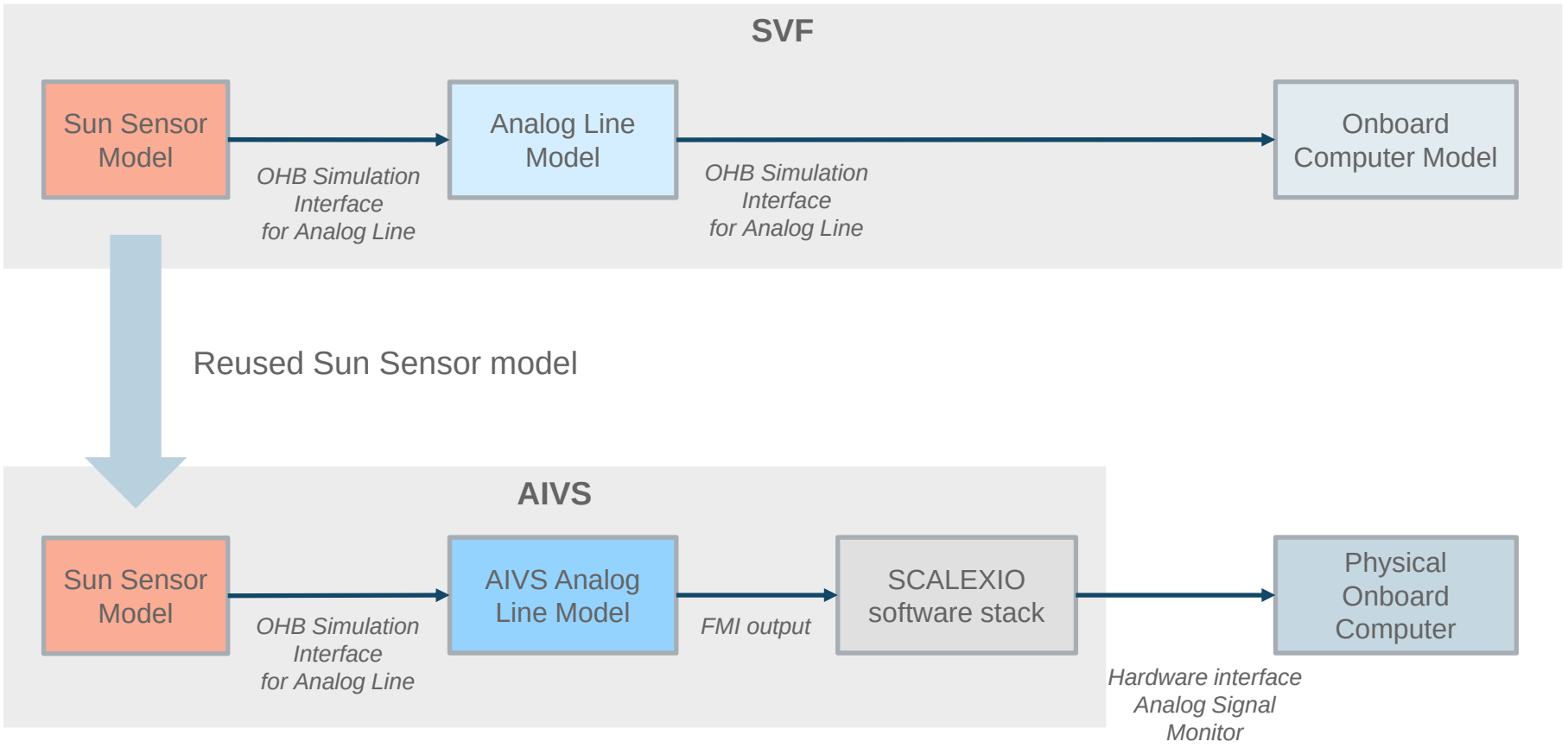


Simulating electrical interfaces: AIVS

- Developed new **AIVS line models** to **connect equipment models to AIVS hardware I/O**
- One end connects to an equipment model via OHB Simulation Interface
- The other end connects to AIVS hardware I/O signal
  - via FMI variables exposed by SCALEXIO software stack
  - for MILBus and RS422 UART, via driver APIs
- Example: Sun Sensor model, with an analog output, sets the output voltage on AIVS hardware connected to physical Onboard Computer

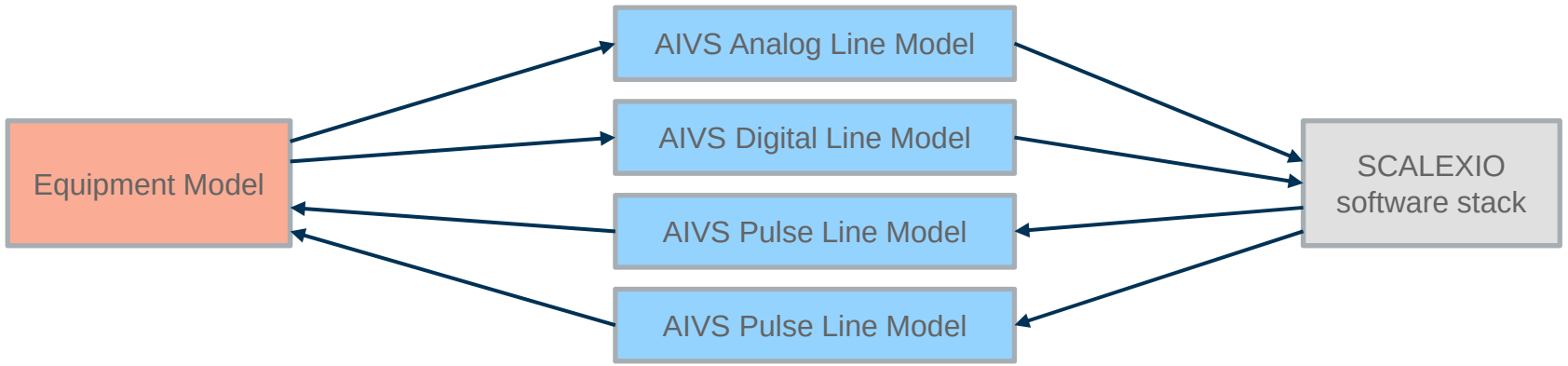


Simulating electrical interfaces: SVF/TOMS vs AIVS



Reusing SMP2 equipment models in AIVS

- Equipment models are developed once
- First used for the SVF, then the AIVS
- To integrate a new equipment model into the AIVS:
  - Add instance of equipment model
  - Add instance of corresponding line model for each electrical interface
  - Configure connections
  - Only takes a couple of hours



Results

- Rufos SMP2 simulation environment for both Linux and SCALEXIO platforms
- Rufos on SCALEXIO runs in steps at 1000 Hz
- AIVS Line Models for
  - MILBus (RT)
  - HV-HPC Input
  - Analog signal I/O
  - Bi-level discrete I/O
  - Power (consumption)
- SARah AIVS includes various AOCS models reused from SARah SVF
- Initial end-to-end integration testing has been successful
  - MILBus communications successful, multiple RTs
- SARah AIVS can be monitored & controlled via network similarly to SCOEs
  - Python scripting

Ongoing work

- Implement RS422 UART AIVS line model
- Integrate more equipment models into SARah AIVS when ready
- Implement AIVS user functions, e.g. NTP time synchronisation
- Load testing
- Validate Rufos on QNX OS

Conclusions

- Rufos on AIVS hardware platform (SCALEXIO)
- AIVS line models, linking OHB Simulation Interface to AIVS hardware
- → **SMP2 Hardware-In-the-Loop simulation framework**

- Equipment models developed for SVF can be reused for AIVS HIL without modification
- Reduces engineering, development and validation effort

- **SMP2 allows reuse of models between different simulator facilities**

Thank you

- AIVS line models implemented according to needed response time:
  - HV-HPC: detect pulse widths of >= 50 ms
  - Analog, digital inputs: update rate of 200 ms
  - M1553: multiple, consecutive transfers (within the same minor frame) are successful

- SARah AIVS SCALEXIO:
  - FMI Inputs: 41 (36 currently connected)
  - FMI Outputs: 62 (56 currently connected)
  - 2 M1553 Buses, 12 M1553 RTs (1 Bus, 10 RTs currently connected)
  - 2 RS422 UARTs

- Currently, when no activity and steps of 1 ms
  - 93.4% of steps execute in less than 10 us
  - 2.6% between 10 us and 40 us
  - 0% between 40 us and 100 us
  - 4% between 100 us and 110 us
  - 0% more than 110 us