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DARWIN AVIONICS DEMONSTRATOR

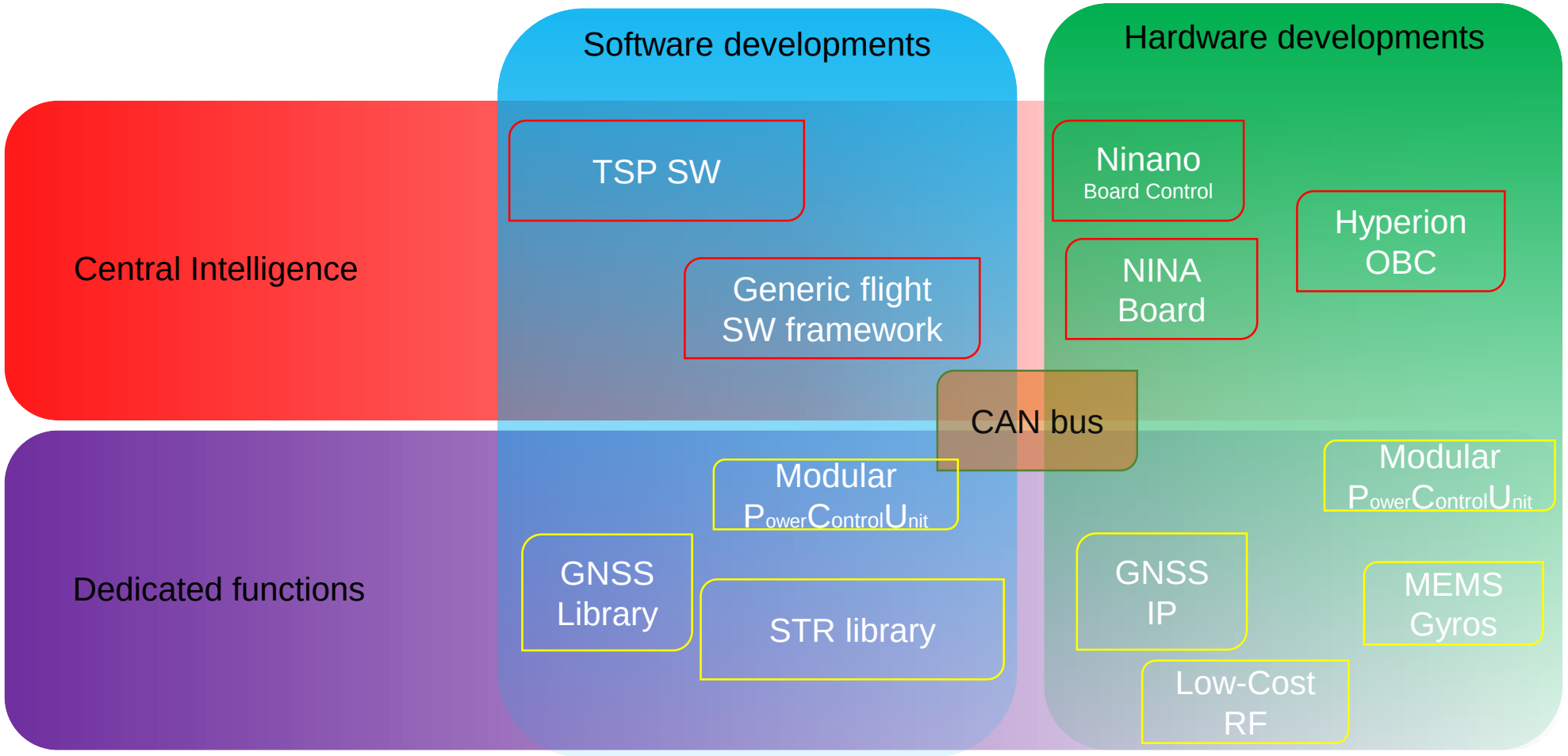
11th ESA ADCSS Workshop
Noordwijk, 19/10/2017

On The Origin Of Species

The project stemmed from 3 observations:

- A lot of R&D projects carried out separately in many fields of avionics but never brought together
- New SOCs now available are much more capable than traditional space hardware
- Cost (+ Mass & Power & Volume) are increasingly important in space industry

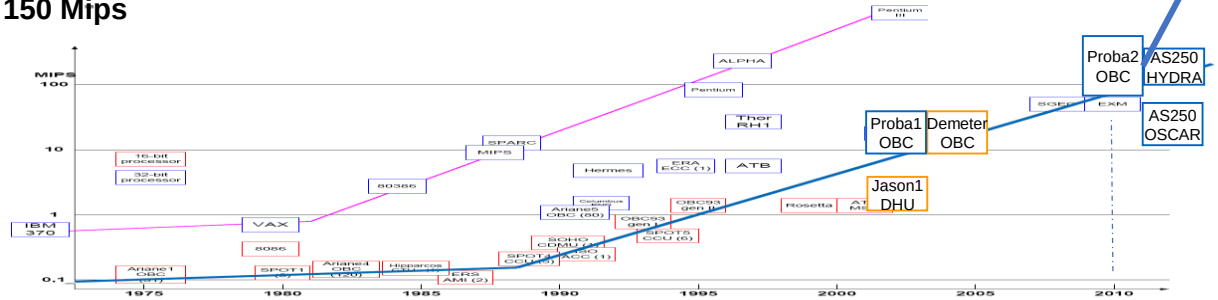
R&D Building blocks



Evolution Of Space Processors

1000 Mips CPU Hyperion — Zynq

150 Mips



1989 **2010** **2019**

GR712 ~150MIPS

AT697 ~100MIPS

SCOC3 ~60MIPS

ERC32 ~10MIPS
LENA ~4MIPS
T805 ~2MIPS

MA31750 ~2MIPS

The Aim Of DARWIN

- **Designing a new avionics architecture based on technologies coming from R&D projects**

  ⇒ Integration of dedicated functions in the OBC

    - Reduction of peripheral hardware complexity
    - Reduction of consumption
    - Reduction of validation and test workload

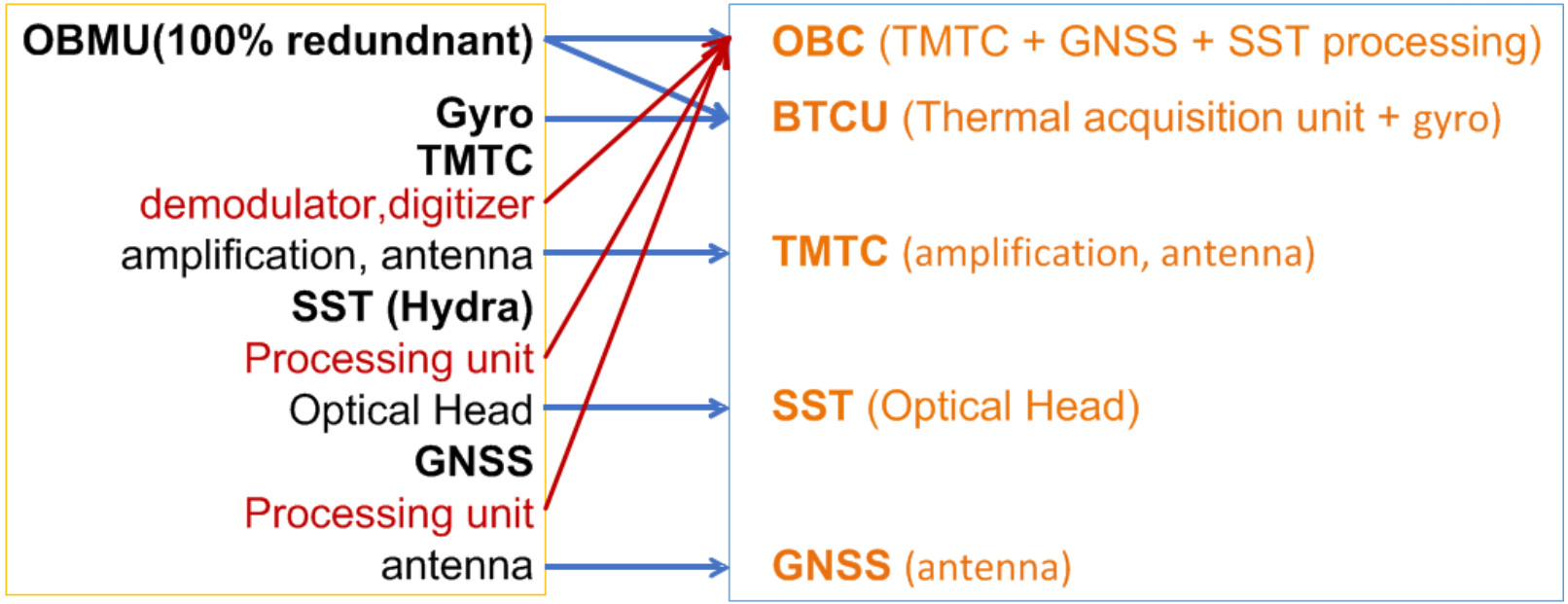
  ⇒ Federate and harmonize R&Ds

  ⇒ Prepare for new SoCs (Dahlia)

  ⇒ Capitalize on Nanosat initiatives

- **Building a demonstrator and assessing it in a representative environment**

Avionics Architecture



High reliability Version

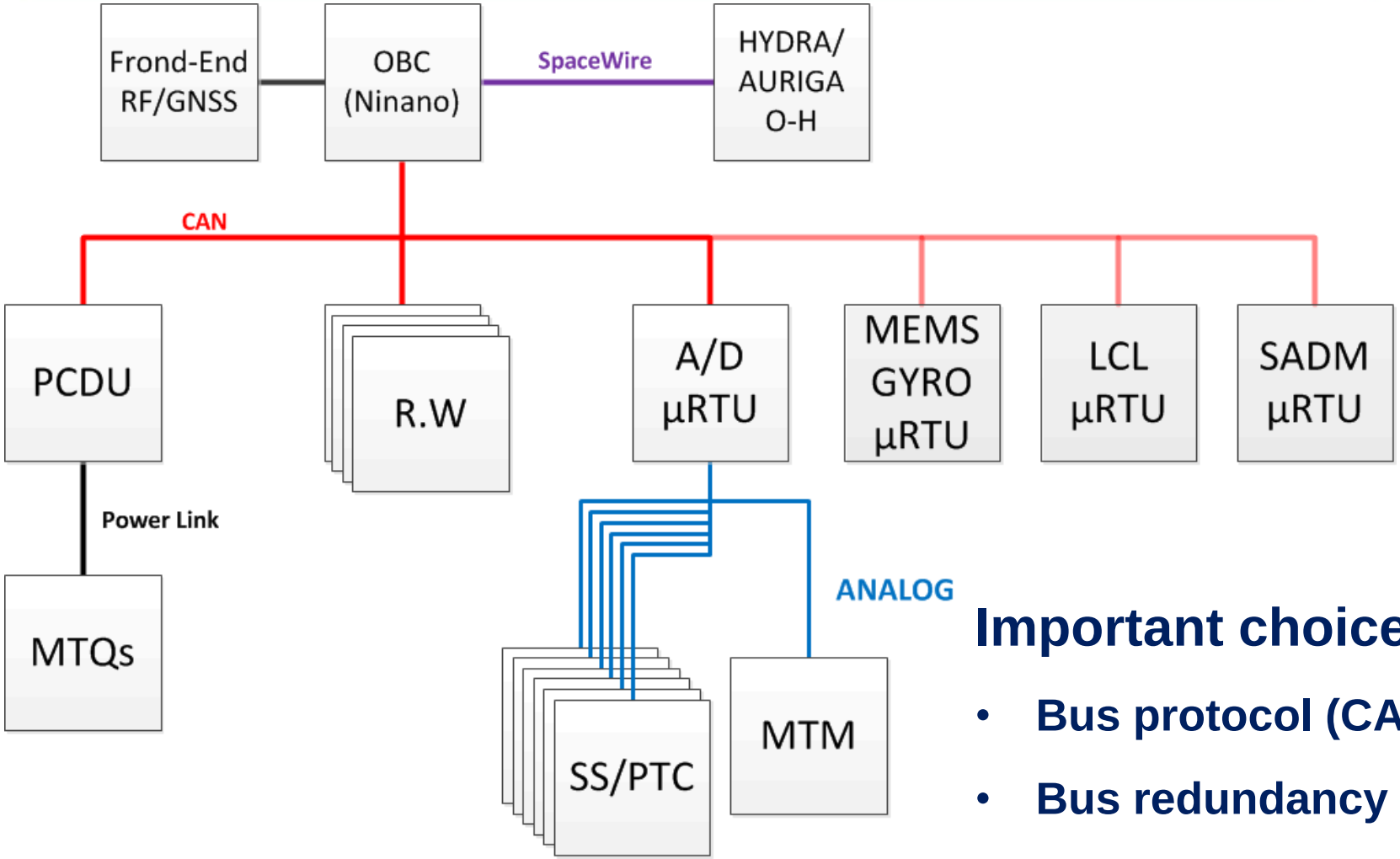
⇒ ~35kg
⇒ ~70W

⇒ ~25kg
⇒ ~40W

Medium/low reliability version

⇒ ~15kg
⇒ ~30W

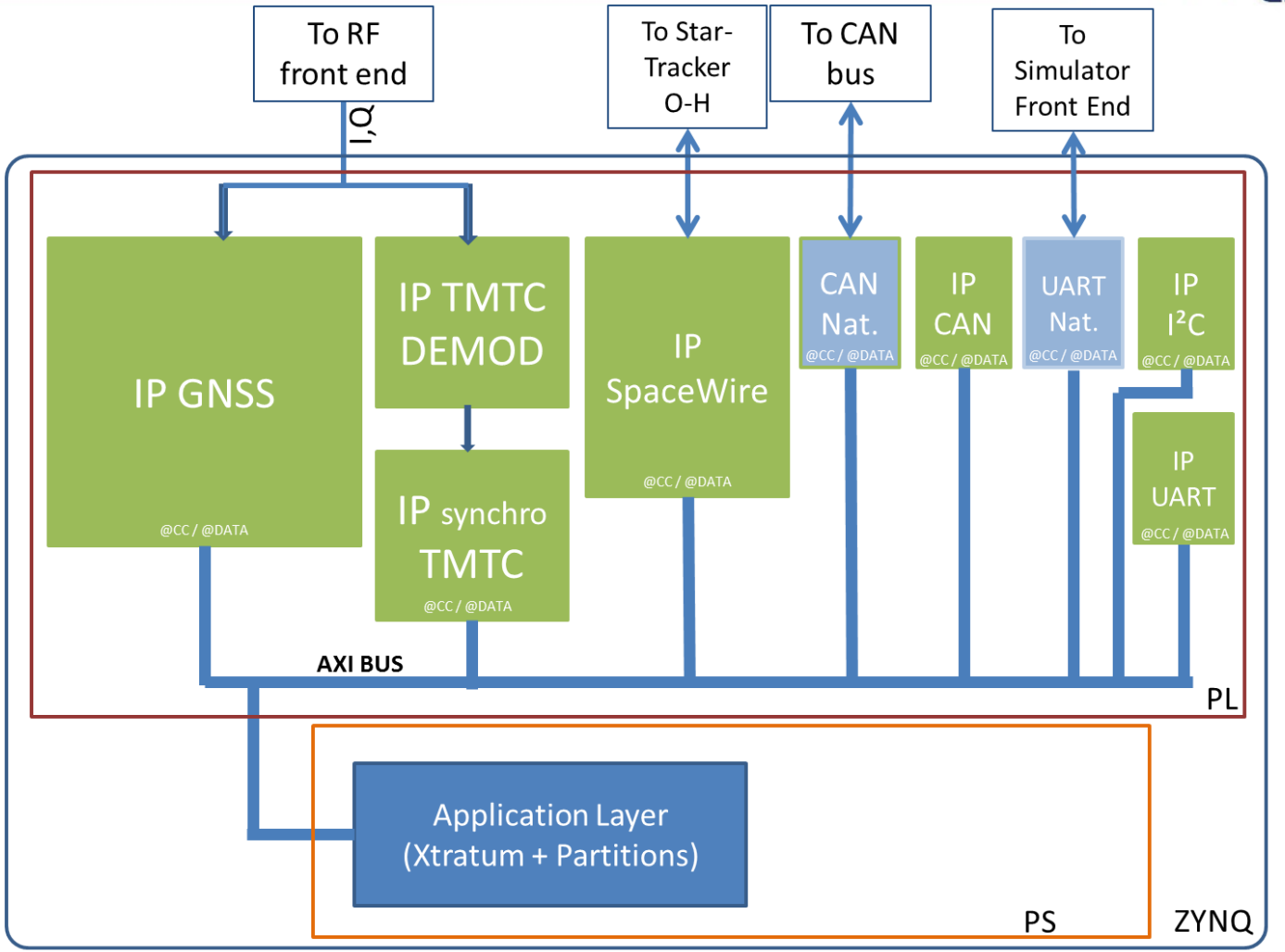
Avionics Architecture



Important choices

- **Bus protocol (CAN vs. CANOpen)**
- **Bus redundancy scheme**

SoC Architecture: VHDL

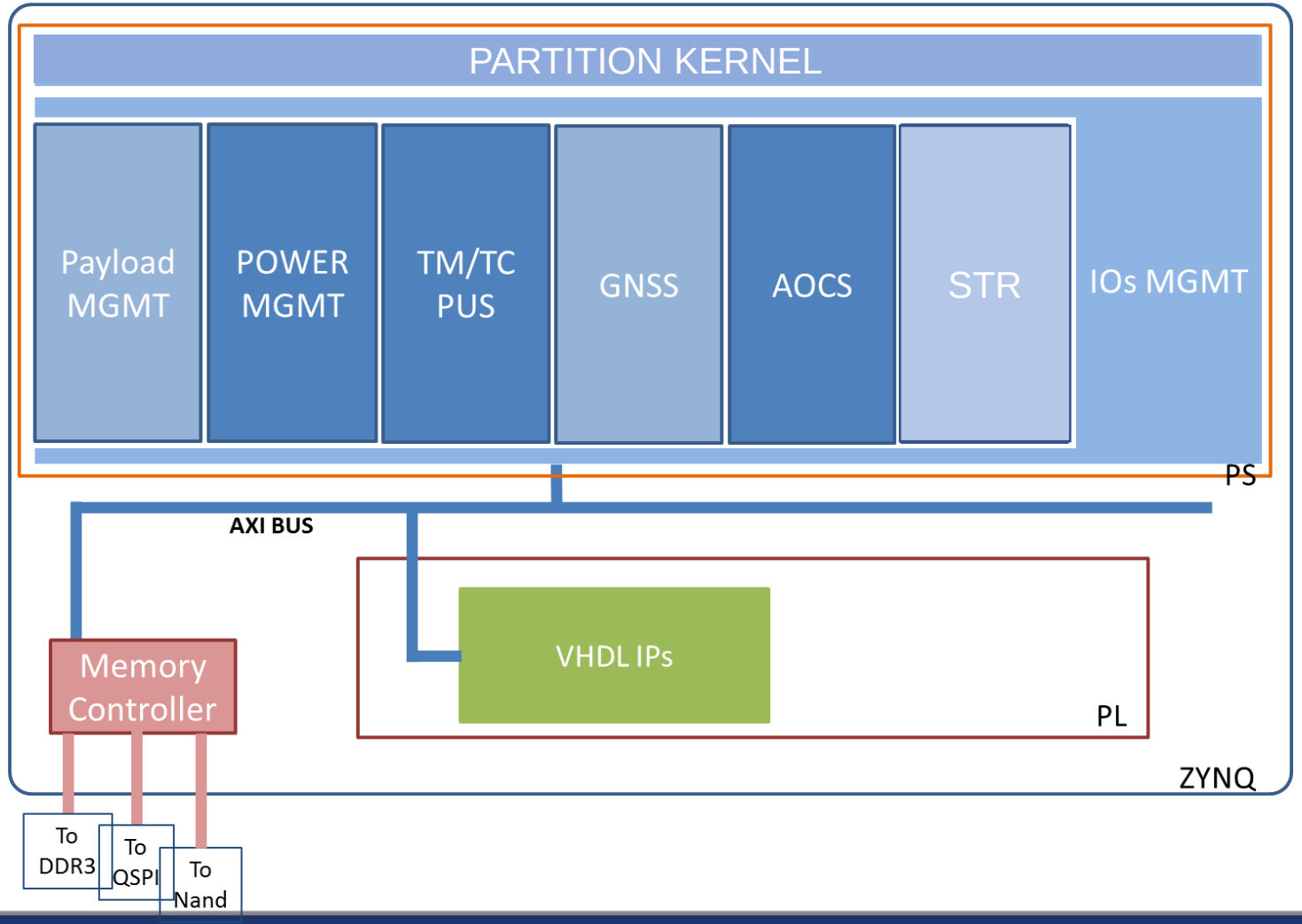


SoC Architecture: VHDL

Open points:

- **Which IP for each function**
- **Which architecture**
- **Which type of SW/HW interface (DMA or FIFO)**
- **Which redundancy scheme**
- **How to manage intellectual property when multiple suppliers are involved**

SoC Architecture: Software



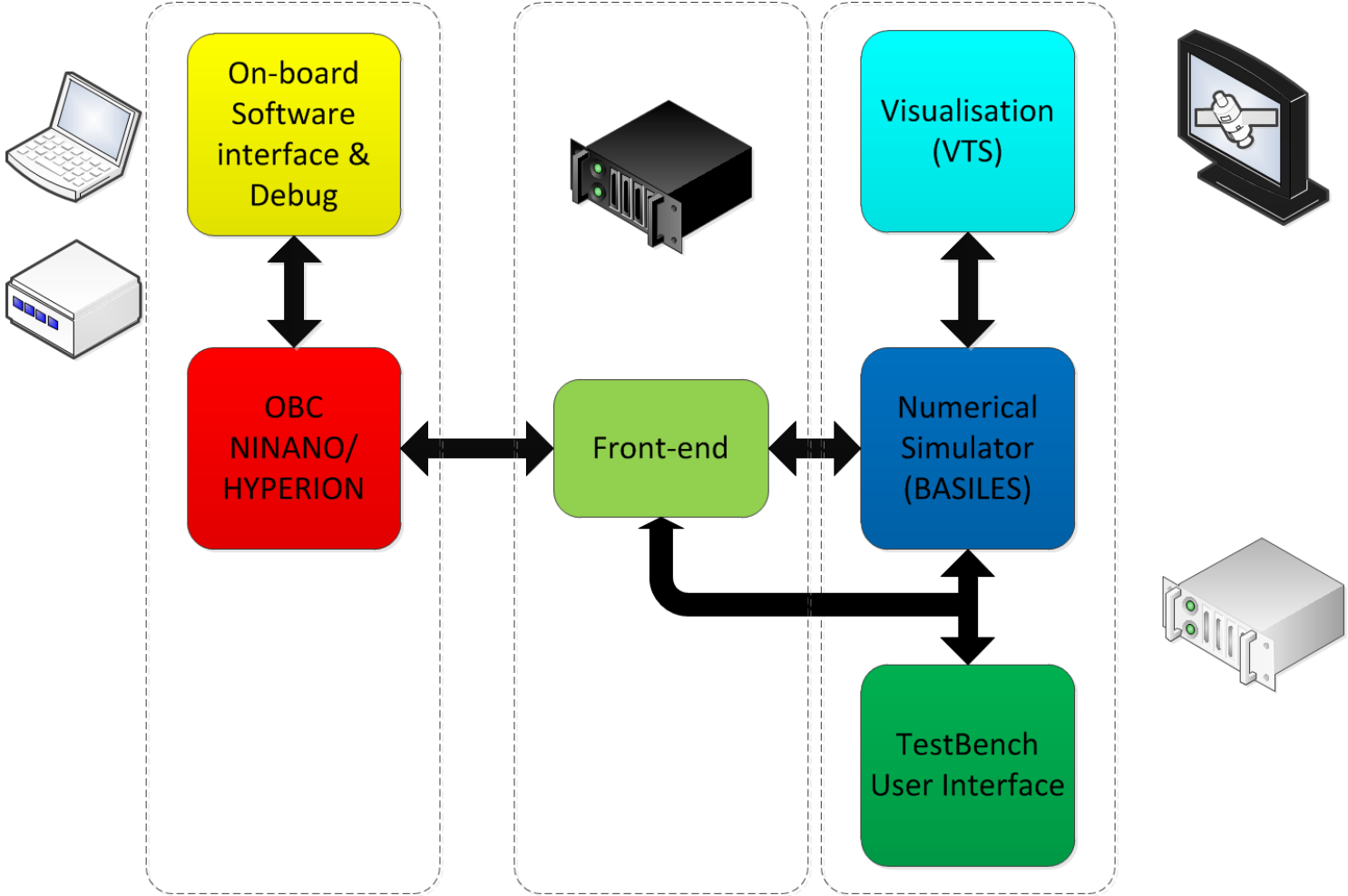
SoC Architecture: Software

Open Points:

- **How to manage IOs**
  - Centralized in a single partition
  - Distributed among all partitions
- **How to access the hardware (DMA or FIFO)**

ITT in progress: K-O of development end of 2017

Testbench Architecture



Desired Outcome

The Demonstrator must allow to determine:

- **The Processor (PS) load factor with Star-tracker and GNSS**
- **The FPGA (PL) load factor, maximum frequency range**
- **The Zynq power consumption and heat dissipation**
- **The best way to control the selected interfaces (CAN, SpW,…)**

Limitations

Concerning IPs:

- GNSS is not fully representative in simulation
- TMTC link: No RF Stage

Limitations

Concerning Software:

- No FDIR (Except for AOCS)
- No Data Loading
- No real Payload management
- No real Power and thermal management
- On-Board management incomplete
- TMTC: No connection with Synchro IP

Major Milestones

- **2016** : Demonstrator definition as a research project in the Avionics department with a 3,5 yrs planning
- **2017**: Important budget increase through CO3D project and planning compression to 2 yrs
- **2017-2018** : Development and integration on Ninano SBC
  Design of Hyperion OBC
- **2018** : **Validation** et **demonstration** on Hyperion

Thank you for your attention

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