

Darwin

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In recent years, the emergence of powerful and yet compact commercial processors and Systems on chips has given the space industry an opportunity to access computing power capabilities an order of magnitude above its traditional hardware at a fraction of the cost.

DARWIN is an avionics demonstrator developed at CNES with the aim of harnessing these new devices to create a highly integrated, versatile, compact, and low cost on-board and data handling system (C&DH). The demonstrator will bring together the great number of R&D projects have been carried out in hardware, software and VHDL development at CNES in the past few years.

The hardware system will rely on a single board computer built around a Xilinx Zynq 7030 called Ninano, initially developed at CNES for Nanosatellites. The considerable computing power of that chip and its embedded FPGA will allow for the implementation of a number of specific tasks that have traditionally been carried out in separate devices, such as GNSS, TM/TC, and Star-Tracker algorithms.

The software on the other hand will be implemented using time and space partitioning, and hence a strict segregation between the various tasks. This segregation is expected to ease the integration of the various parts of the software, and provide a more robust implementation.

In order to assess the performances of this demonstrator, a hardware-in-the-loop simulator will be built. This test bench will couple the avionics system to a representative simulator of the DEMETER satellite (CNES Myriade family) using a CANbus. An actual star-tracker optical head will also be connected to the on-board computer, and optically stimulated by the simulator. Using this simulator, it will be possible to evaluate de capacity of the system to properly control the attitude of a satellite including star-tracker processing. The other implemented functions (GNSS, TM/TC) will not be used by the simulator, but will be assessed separately.

Although the most tangible outcome of this project will be the demonstrator itself, it will also provide a unique opportunity to develop the methods and skills necessary to successfully integrate software and VHDL IPs from different providers in a single chip.