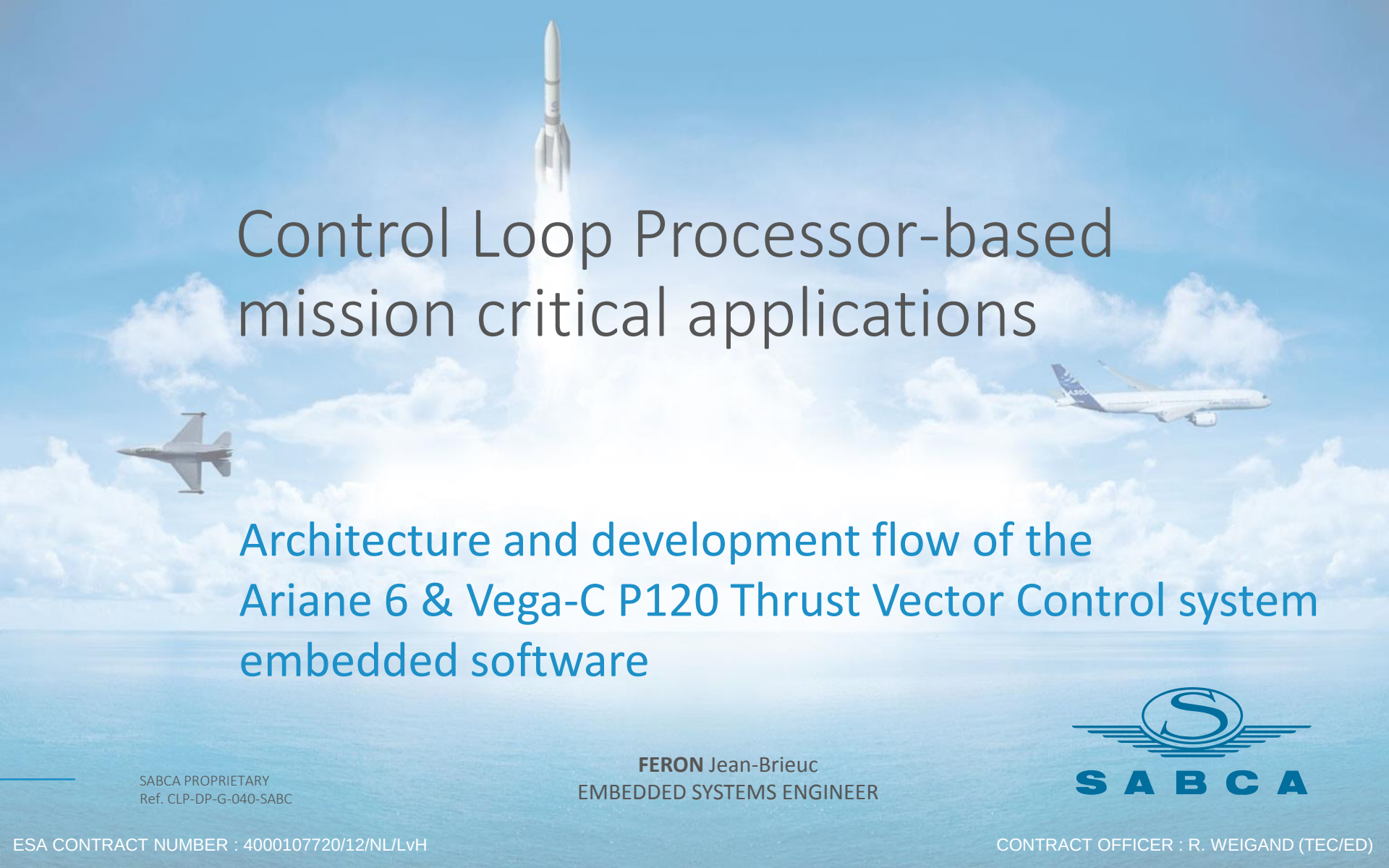


Control Loop Processor-based mission critical applications

Architecture and development flow of the Ariane 6 & Vega-C P120 Thrust Vector Control system embedded software

FERON Jean-Brieuc
EMBEDDED SYSTEMS ENGINEER

SABCA

ESA CONTRACT NUMBER : 4000107720/12/NL/LvH

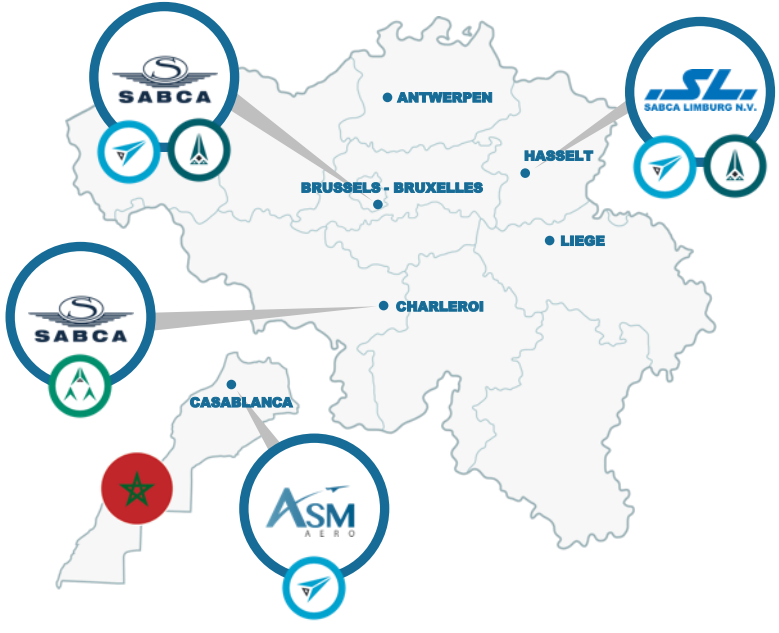
CONTRACT OFFICER : R. WEIGAND (TEC/ED)

Who are we?

SABCA

> Shareholders

> Plants



What do we do?
at SABCA

> Markets


Defence

Aviation

Space

Ariane 6 & Vega-C P120
Thrust Vector Control (TVC) system

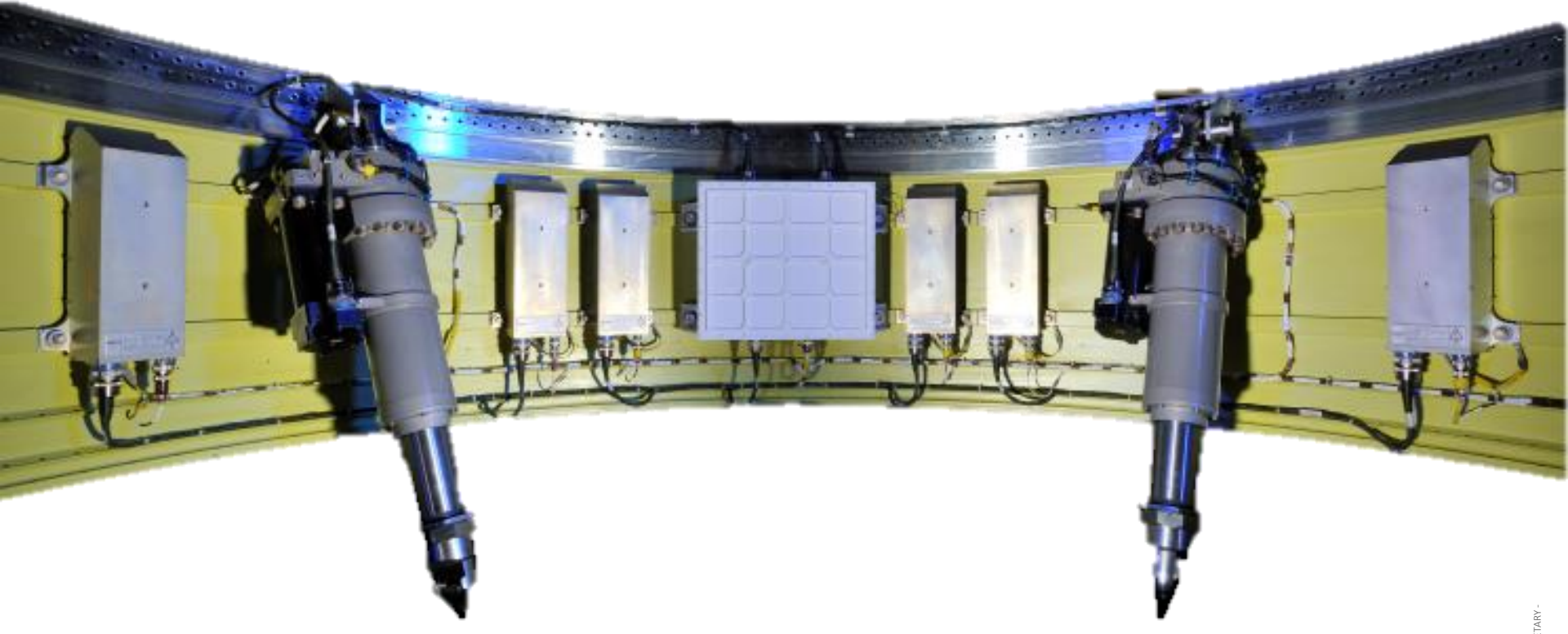
System architecture | Context & constraints | Control architecture

SABCA

Architecture

of the Ariane 6 & Vega-C P120 TVC system

> Vega P80 TVC system :



Context & constraints

of the Ariane 6 & Vega-C P120 TVC system

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> Launcher
  - First launch : 2019 (Vega-C), 2020 (Ariane 6)
  - Planning status : post PDR

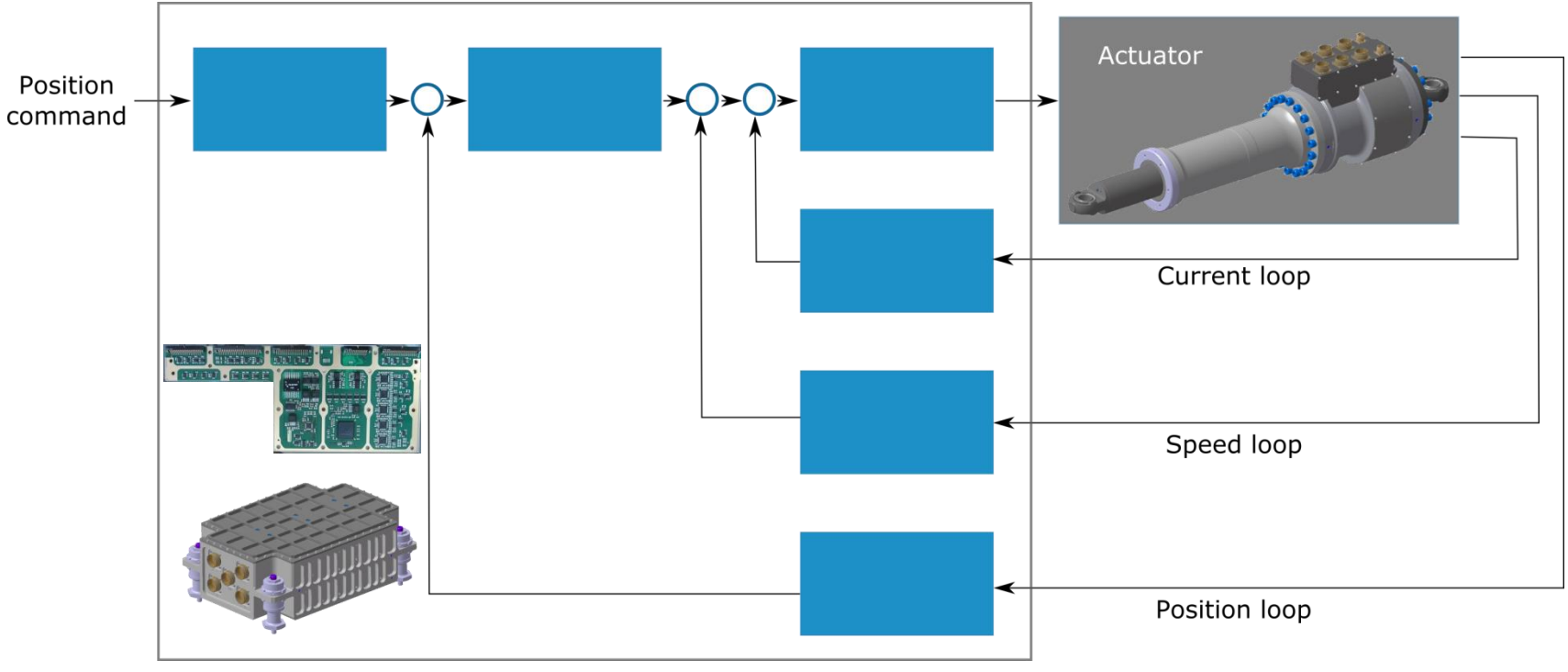
> Thrust Vector Control system
  - Requirements
    - Stroke
    - Accuracy
    - Speed
    - Reliability
    - Differential force feedback
  - Constraints
    - High vibration
    - High temperature
    - Vacuum
    - Shocks

Wikipedia CC by 3.0

Control architecture

of a single Ariane 6 & Vega-C P120 actuation system

- Commands are received from the launcher on-board computer
- 3 nested control loops : current , speed, position



Embedded software requirements & constraints

of the Ariane 6 & Vega-C TVC system

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> Requirements

- Control the actuator position
- Communicate with On-Board Computer
- Perform measurements (functional & non-functional)
- Support launcher interfaces (TM/TC/measurements,…)
- Meet ECSS constraints (Class B)
- Support configuration commands
- Support different operational modes
- Withstand a tight planning at a competitive cost

Impact on the processing platform selection?

Embedded software requirements & constraints

of the Ariane 6 & Vega-C TVC system

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> Requirements

- Control the actuator position
- Communicate with On-Board Computer
- Perform measurements (functional & non-functional)
- Support launcher interfaces (TM/TC/measurements,…)

→ Performance requirements

- Meet ECSS constraints (Class B)

→ SW criticality requirement

- Support configuration commands
- Support different operational modes
- Withstand a tight planning at a competitive cost

→ Agility requirements

Impact on the processing platform selection

Control Loop Processor in a nutshell

Reliable Agile

Processing platform

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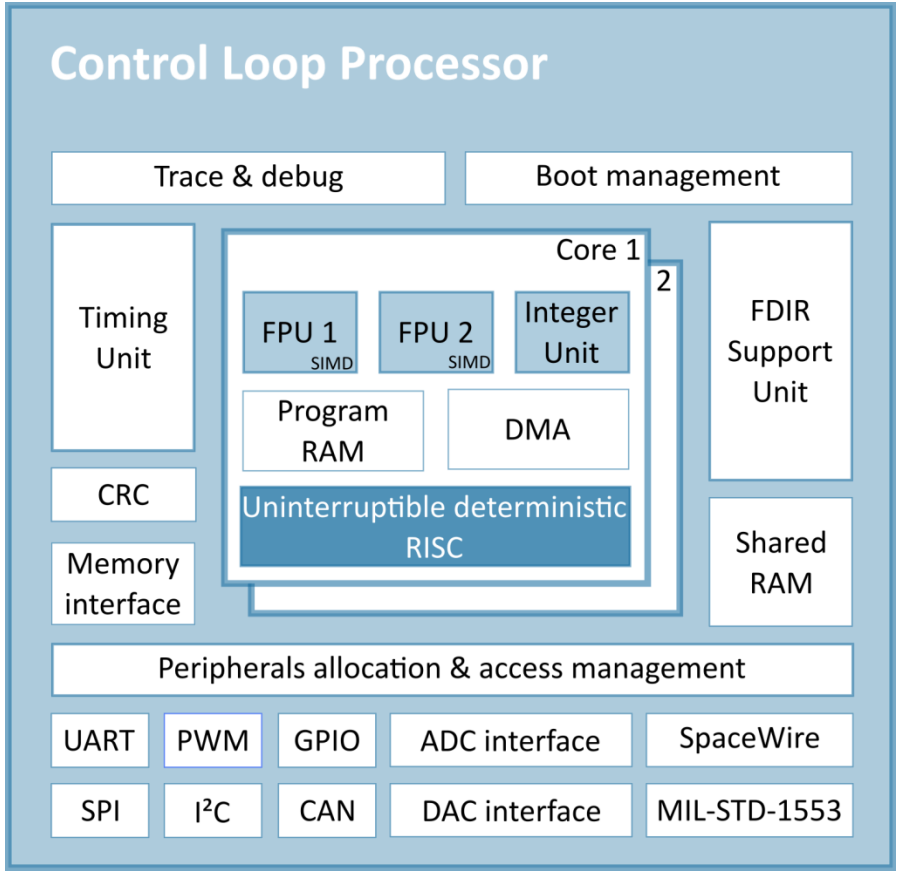
A softcore processor and a development platform

with 3 specificities

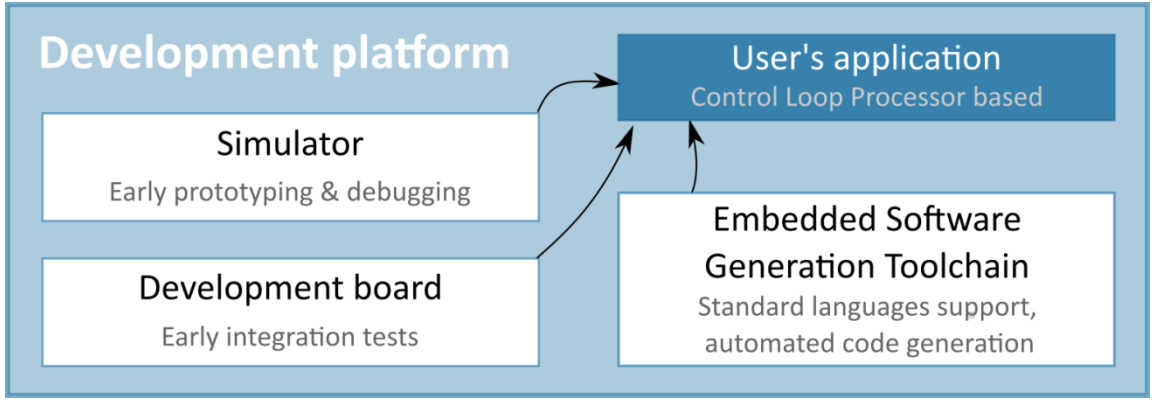
Reliable	Agile	Performance
Deterministic Cache-free & non interruptible architecture	Quick turnaround time Straightforward code generation	Precision arithmetic IEEE-754 floating-point operations
Certified European space standards compliance	Flexible softcore architecture Configurable number of cores, arithmetic units or memory size	High throughput Dual-core SIMD architecture, Direct Memory Access
Fault-tolerant Error detection & correction Radiation hardening	Short design validation time Deterministic system behaviour Small state space to validate	High connectivity High-speed communication interfaces
Integrated Communication interfaces, Low level control	Project planning flexibility Early demo & late changes support	Real-time HW/SW synchronization Operating System free

Architecture
of the Control Loop Processor



A complete development platform

supporting the user all along its development process



- Simulator

  Cycle- and bit-accurate C++ compliant model, provides early representative processing performance.

- FPGA development board

  Integrating all the communication interfaces for early integration tests

- Embedded Software Generation toolchain

  Eclipse based configuration wizards, automated code generation from Simulink

Ariane 6 & Vega-C P120 TVC embedded software

Software architecture | Performance | Development flow

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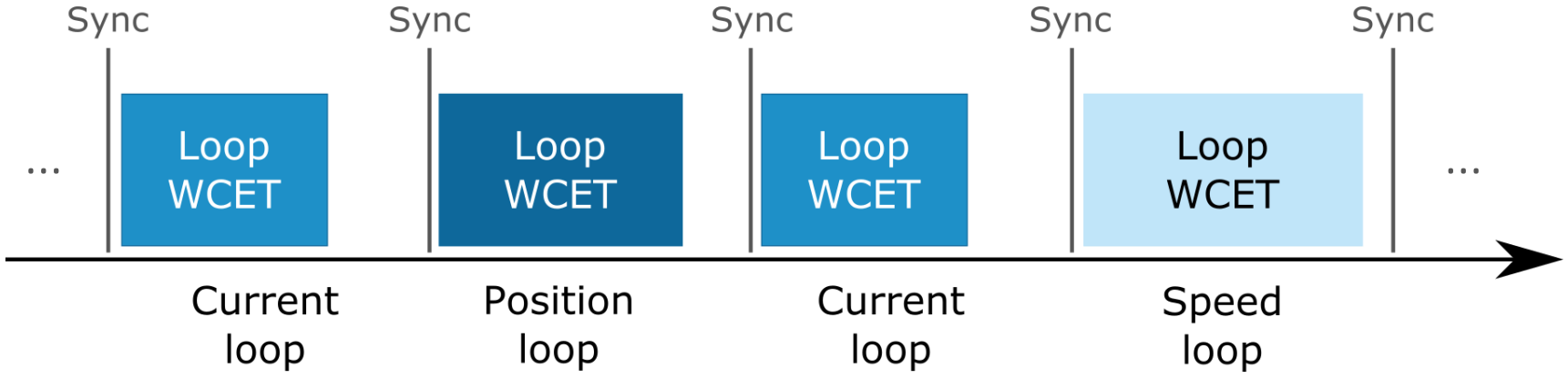
Embedded software architecture
of the Ariane 6 & Vega-C P120 TVC system

- Two cores with the same software each control one actuator
- A dedicated CLP hardware timer synchronizes the whole system
- Analog acquisitions performed outside PWM switching
- I/O servicing through software polling



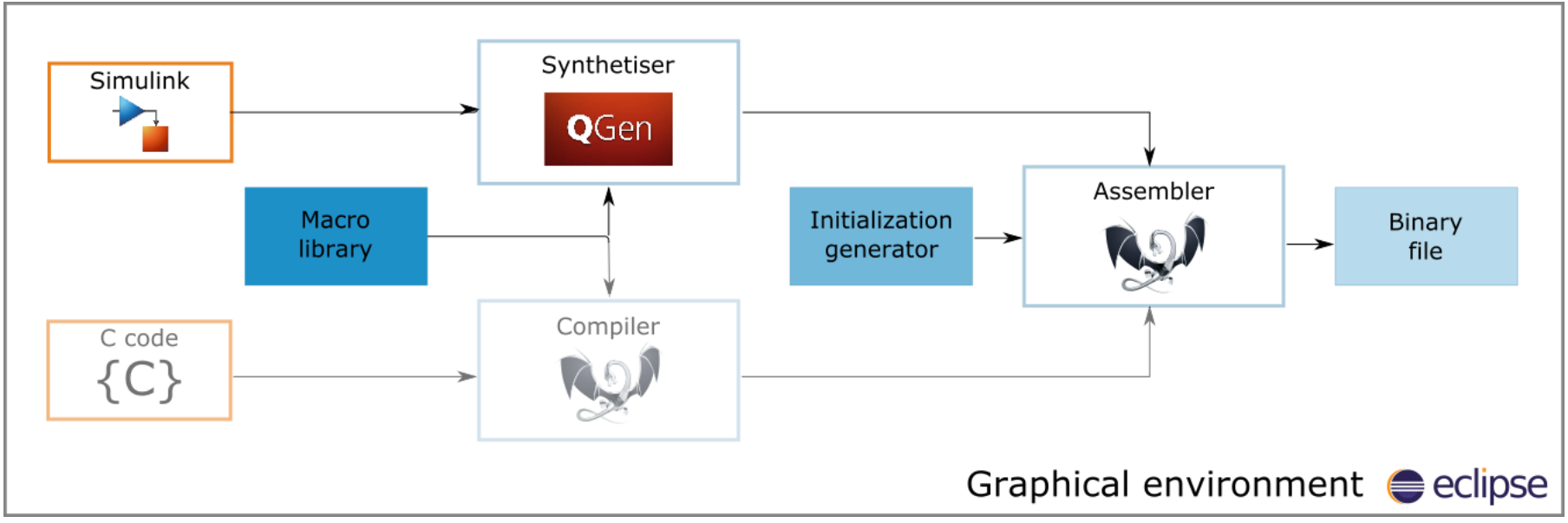
Performance
of the controller based on the CLP platform

- Taking advantage of the CLP architecture
  Dual-Core, SIMD, fault tolerance
- Complexity
  Floating point control with complex operations (motor control direct & reverse transforms, 1st & 2nd orders filters) and power sharing.
- Resources usage

Program memory	< 40%
RAM	< 20% (worst case)
Registers	minimal
Peak CPU load	< 75%
Average CPU load	< 70%

Development flow
of the CLP embedded software

- The macro library is highly optimized and pre-validated
- The binary file is validated against different reference models
- Point-to-point source & output software cross-checking



Progress illustration

Vega-C Z40 TVC system

Ref. CLP-DP-G-040-SABC

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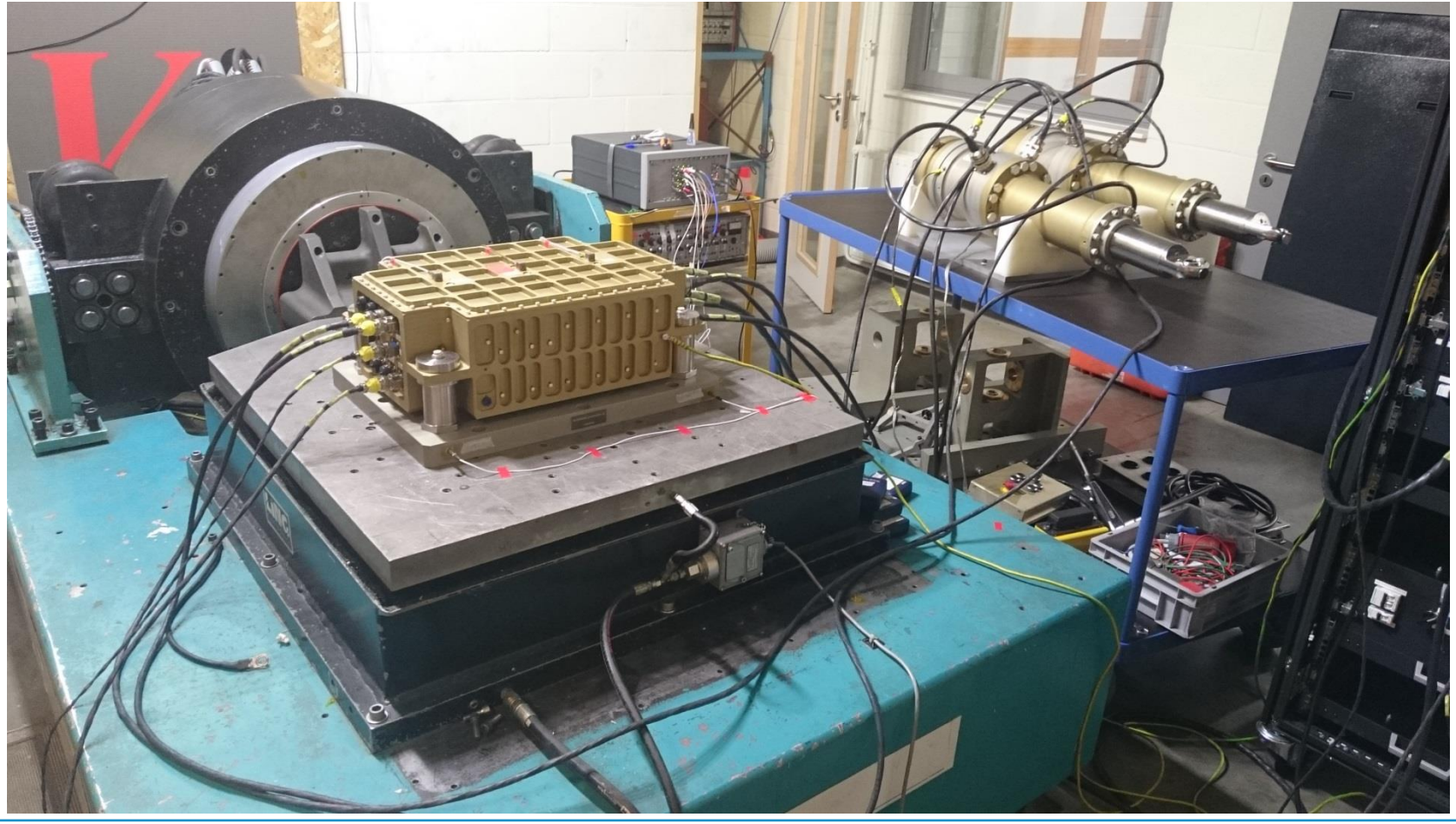
Environment tests

of Vega-C Z40 TVC system



Conclusion

what should you take away?

> There is a strong link between
  - Thrust Vector Control system requirements
  - Processing platform architecture
  - Embedded software performance & development effort

> The existence of a reliable & agile processing platform is a reality

> Our customers take advantage of this platform for their mission critical applications. Why don't you?

Evaluation pack available on request!

Thank you!

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