Introduction to Dyplo and its latest status regarding support for rad-hard FPGAs and RTEMS

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This presentation will introduce Dyplo and the steps currently being taken to add support for RTEMS and the radiation hardened Xilinx Virtex5QV FPGA. The goal of Dyplo is to significantly simplify dynamic reuse and programming of SRAM based FPGA logic.

Dyplo consists of an IP-Core, a software API and drivers and comes with development support tooling. The software API provides an interface to software application developers. This API makes it easy to program, use and change functionality in the FPGA from software running on a CPU. Changing the functionality can be done at run time, without disturbing other functionality in the FPGA. The development support tooling enables software developers to easily deploy functionality, written in C/C++, on the FPGA without the help of VHDL engineers. VHDL engineers can also benefit from using Dyplo. They can easily connect their VHDL-programmed-logic and IP cores to the Dyplo framework, which will then take care of the interfacing with software. Dyplo does this all by using the partial reconfiguration feature that is present in modern SRAM-based-FPGAS.

Dyplo has initially been developed for use on the Xilinx Zynq SoC based devices with drivers for Linux and with development support tooling that runs on Linux and Windows. Later support has been added for Xilinx Kintex-7 and Ultrascale+ devices and drivers have been developed for Windows.

Currently Topic is in the context of a GSTP project, making the Dyplo-IP compatible with the radiation hardened Xilinx Virtex 5QV FPGA technology and adding drivers for the RTEMS operating system. This will be validated by running a Dyplo demo which consists of a control application on RTEMS on a LEON softcore processor on a Virtex 5, image processing algorithms that are dynamically deployed on the Virtex 5 and a SpaceWire connection that receives and sends the image data.