MOVE THE WORLD FORWARD MITSUBISHI HEAVY INDUSTRIES GROUP

Development of Next-generation Space-Grade Processors, SOI-SOC series

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19.Oct.2017

MITSUBISHI HEAVY INDUSTRIES

Introduction

- Mitsubishi Heavy Industries have been working on space-grade system-on-chip processors, SOI-SOC series, in partnership with JAXA.

- The first product is SOI-SOC2 which is flight-proven in ASTRO-H and ERG satellites, etc.

- And now, increasing demands for high-speed/high-reliability communication in spacecraft applications, we have been developing SOI-SOC3. SOI-SOC3 is a product that aimed to improve the SpaceWire function based on SOI-SOC2.

- We have currently been developing SOI-SOCX simultaneously with SOI-SOC3. SOI-SOCX targets innovative space missions and Dual-Use markets. SOI-SOCX will have renewed semiconductor process and CPU to realize higher processing speed and world’s top-class power efficiency.

Roadmap of SOI-SOC series

Mitsubishi Heavy Industries have been working on space-grade system-on-chip processors, SOI-SOC series, in partnership with JAXA.

Product		2016	2017	2018	2019	2020	2021	2022
SOI-SOC 2	・Standard-Model ✓SingleCore ✓Standard SpW-I/F	Flight model Available ASTRO-H launched	ERG launched					
SOI-SOC 3	・Enhanced-Model ✓SingleCore ✓High-end SpW - Hardware offload of RMAP, SpW-R,D	Under Development FPGA Sample Chip	EM Sample Chip	Flight model Available				
SOI-SOC X	・Next-Gen.-Model ✓DualCore ✓Various I/F (SpW,1553,Ether etc.) ✓On-ChipRAM ✓Low-Power	Under Development		FPGA Sample Chip	EM Sample Chip	Flight model Available		

Overview of SOI-SOC2

MHI approach for Radiation-Hardening

1. Manufacturing Process level

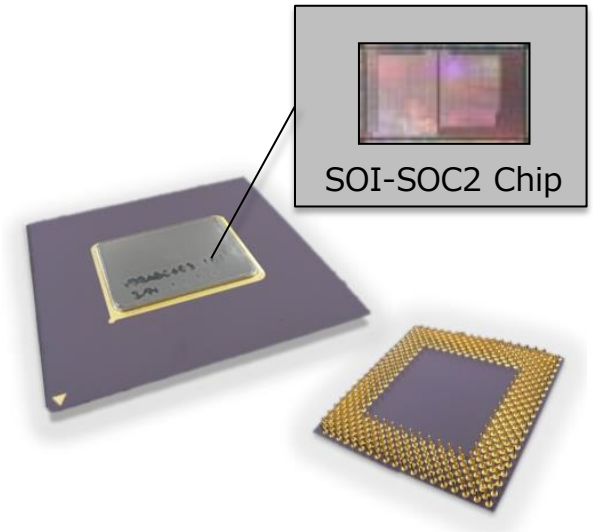
Adoption of Silicon on Insulator (SOI) technology

2. Circuit Architecture level(RHBD)

Development of circuit design for radiation effects mitigation

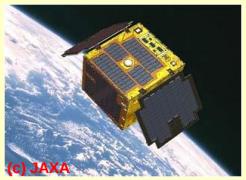
Application in space

SOI-SOC2 has been applied to many satellites and successfully worked on orbit.



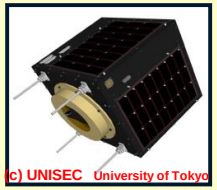
Radiation-hardened processor SOI-SOC2

SDS-1 satellite



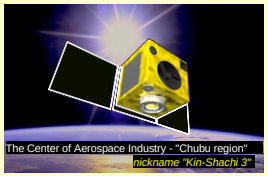
SDS-4 satellite

UNITEC-1 satellite

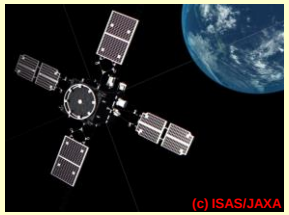


ASTRO-H satellite

ChubuSat-3 satellite



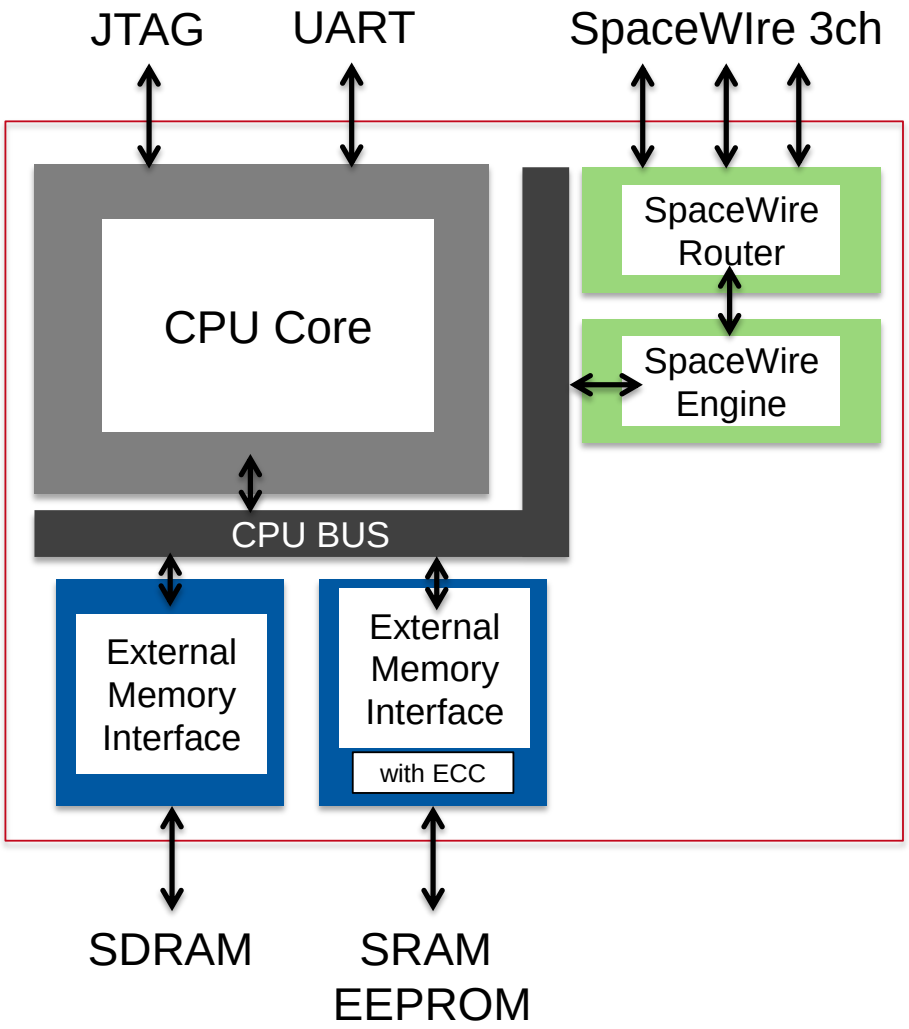
ERG satellite



SOI-SOC2 is a Flight proven Microprocessor

Specification of SOI-SOC2

Block Diagram



Specification

Item		Specification
Semiconductor Process		200nm SOI
CPU Core		32bit RISC Processor Max.100MIPS
Memory interface		SDRAM I/F and SRAM/EEPROM I/F
SpaceWire		-
	Link Frequency	Max. 100MHz
	External Port	3ch
	Hardware offload	-
Package		Ceramic PGA 447pin

Overview of SOI-SOC3

Motivation

1. Upgrade of SpaceWire

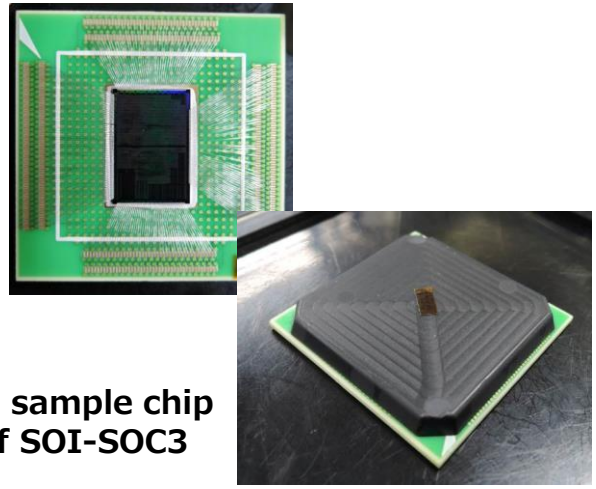
Large-scale SpaceWire network is widely used in satellites, especially science missions.

CPU load in such network tends to become higher due to its SpW protocol, largely its RMAP protocol and synchronization protocol using Time-Code.

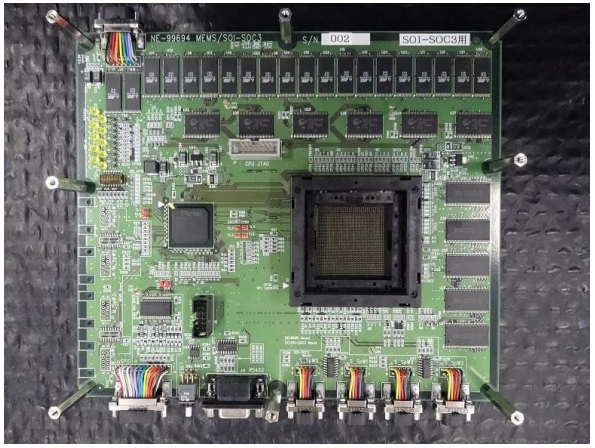
Thus, needs of improvement of SpW-Engine built in SOI-SOC are increasing.

2. Standard development environment

In order to shorten development period of spacecrafts and reduce development cost, needs for evaluation board and software development environment which includes OS, BSP and Middleware are increasing.



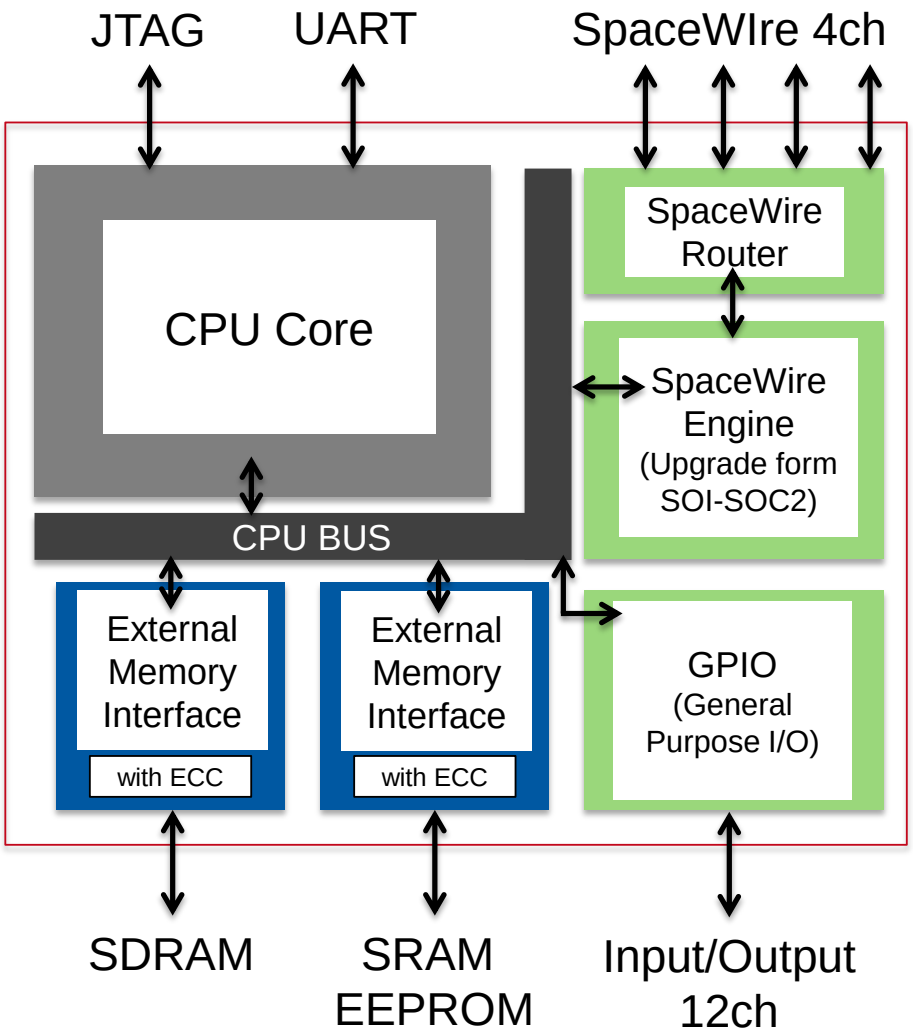
EM sample chip of SOI-SOC3



Evaluation Board of SOI-SOC3

Specification of SOI-SOC3

Block Diagram



Specification

Item		Specification
Semiconductor Process		200nm SOI
CPU Core		32bit RISC Processor Max.100MIPS
Memory interface		SDRAM I/F and SRAM/EEPROM I/F
SpaceWire		
	Link Frequency	Max. 120MHz
	External Port	4ch
	Hardware offload	RMAP Protocol SpaceWire-D Protocol SpaceWire-R Protocol
Package		Ceramic PGA 447pin/ Plastic BGA

SpaceWire Engine of SOI-SOC3

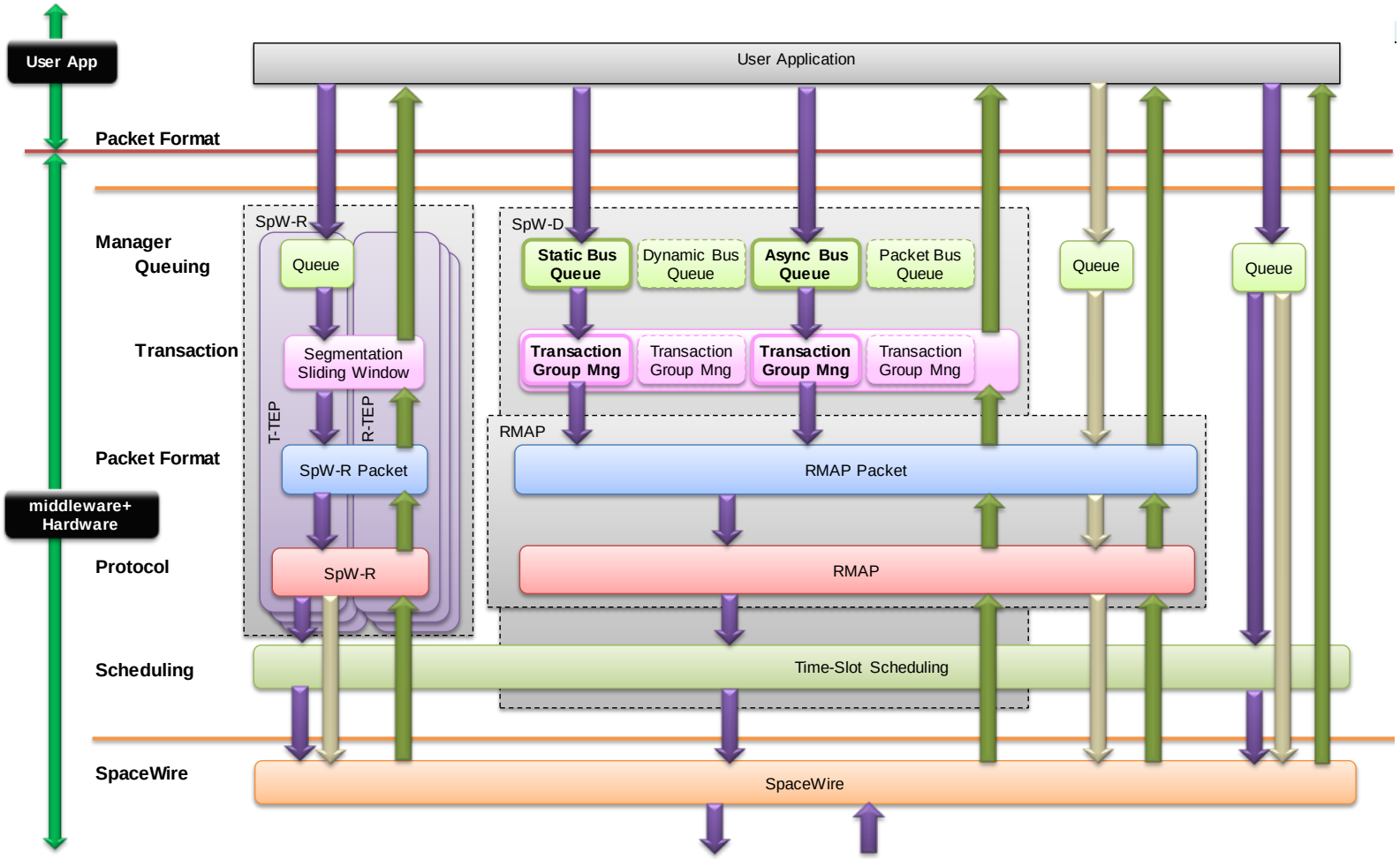
- SOI-SOC3 has a high-reliability SpaceWire engine, supporting upcoming SpaceWire standards.
  - ✓Deterministic Data Delivery, SpaceWire-D (Draft D Issue 0.15)
  - ✓Reliable Data Transfer, SpaceWire-R (SCDHA 151-0.4 Issue 0.4)

- The SpaceWire engine is mainly performed on hardware.
  - ✓High accuracy scheduling and high performance with improve CPU load.

Protocol	Function	Hardware support
RMAP	RMAP Write	✓Header format check (Key, Logical Address, CRC etc.) ✓Data transfer to external memory with DMA ✓Generate write reply
	RMAP Read	✓Header format check ✓Data transfer from external memory with DMA ✓Generate read reply
SpaceWire-D	Timing Control	✓Control of send timing of RMAP command
	Time-Code Watchdog	✓Detect Early/Late watchdog
SpaceWire-R	Segmentation	✓Break SDU(Service Data Unit) into SpW-R data packets at sending end ✓Reconstruct SDU from data packets at receiving end
	Data Ack Reply	✓Check SpW-R data packet ✓Reply data ack packet

Software Interface of SOI-SOC3

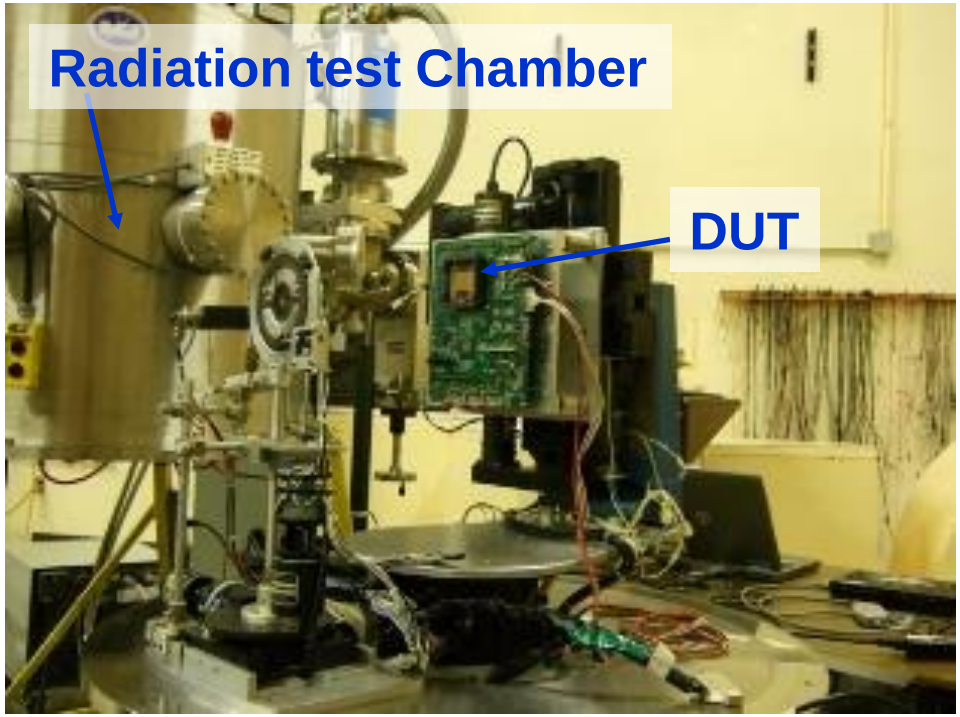
- Users can handle SpaceWire easily.
  - ✓Real-time Operating System (TOPPERS HRP2) and BSP/Middleware are available.
  - ✓Middleware supports RMAP, SpaceWire-D, SpaceWire-R protocols.



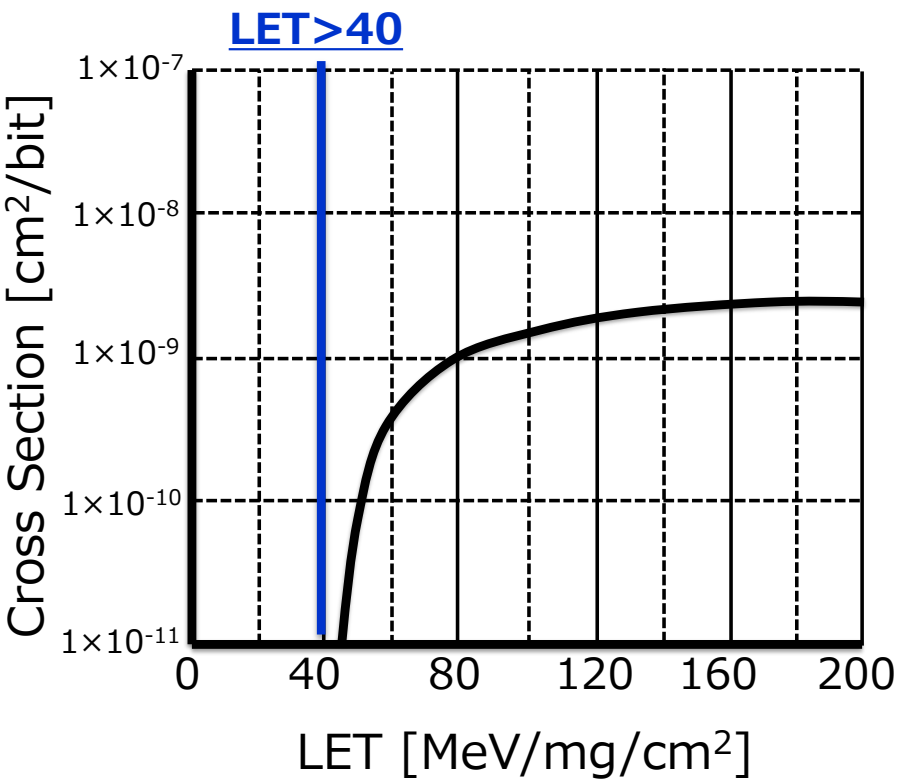
Radiation Hardness of SOI-SOC2/3

- 200nm SOI process shows excellent performance for radiation.
  - ✓ SEL free
  - ✓ SEU 25~40 MeV/（mg/cm^2）

- Radiation Test



- Cross Section of SRAM



Overview of SOI-SOCX

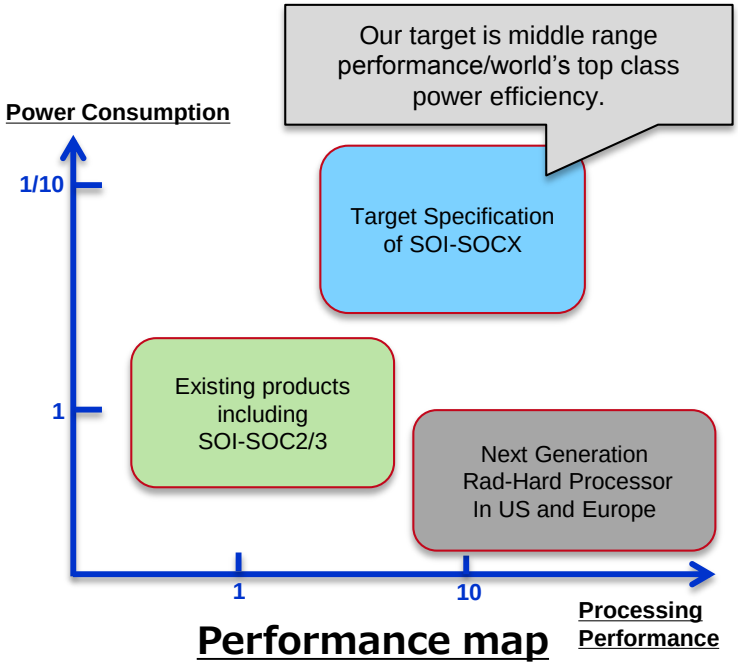
Motivation

1. Steady development

We selected a new semiconductor process to improve the product's performance, but we will steadily develop by using SOI-SOC2/3 design assets, especially RHBD techniques.

2. Needs for the future

SOI-SOCX targets innovative space missions and Dual-Use markets. We discussed with future users frequently and set development goals.



Performance map

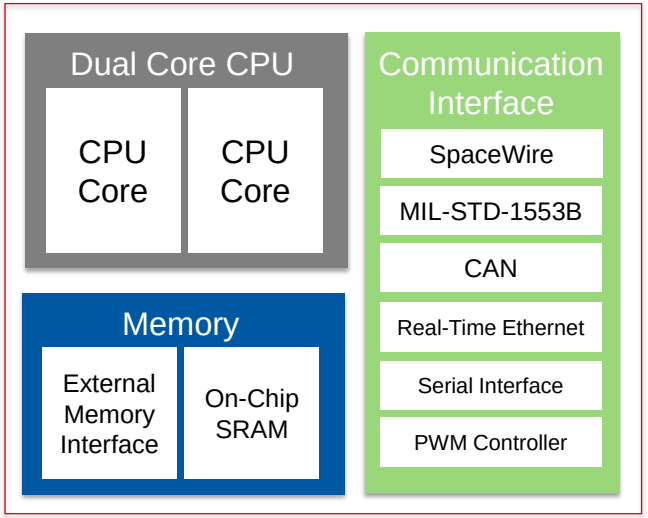
1) Processing Performance
- ・Performance improvement more than 10 times of SOI-SOC2/3

2) Low-Power and Built-in RAM
- ・Reduce power consumption by 1/10 compared to SOI-SOC2/3
- ・Large size built-in RAM （Mbyte～）

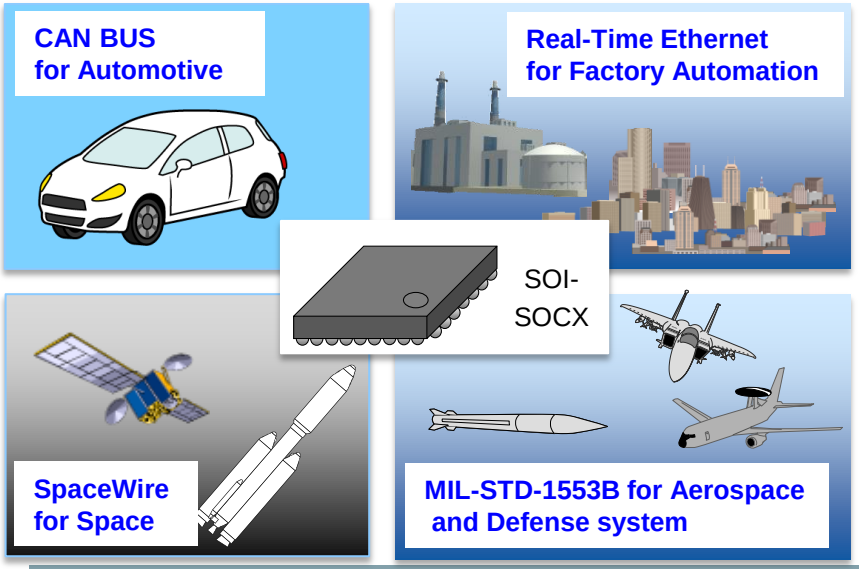
3) Communication Interface
- ・Various communication interfaces for the flexibility and scalability
  - ✓MIL-STD-1553B, Ethernet, SpaceWire, CAN Bus etc.
  - ✓SpaceWire-Engine has hardware offload of RMAP protocol as with SOI-SOC3. To cope with future changes of SpaceWire standards, SpW-R and SpW-D are implemented as software.

Overview of SOI-SOCX

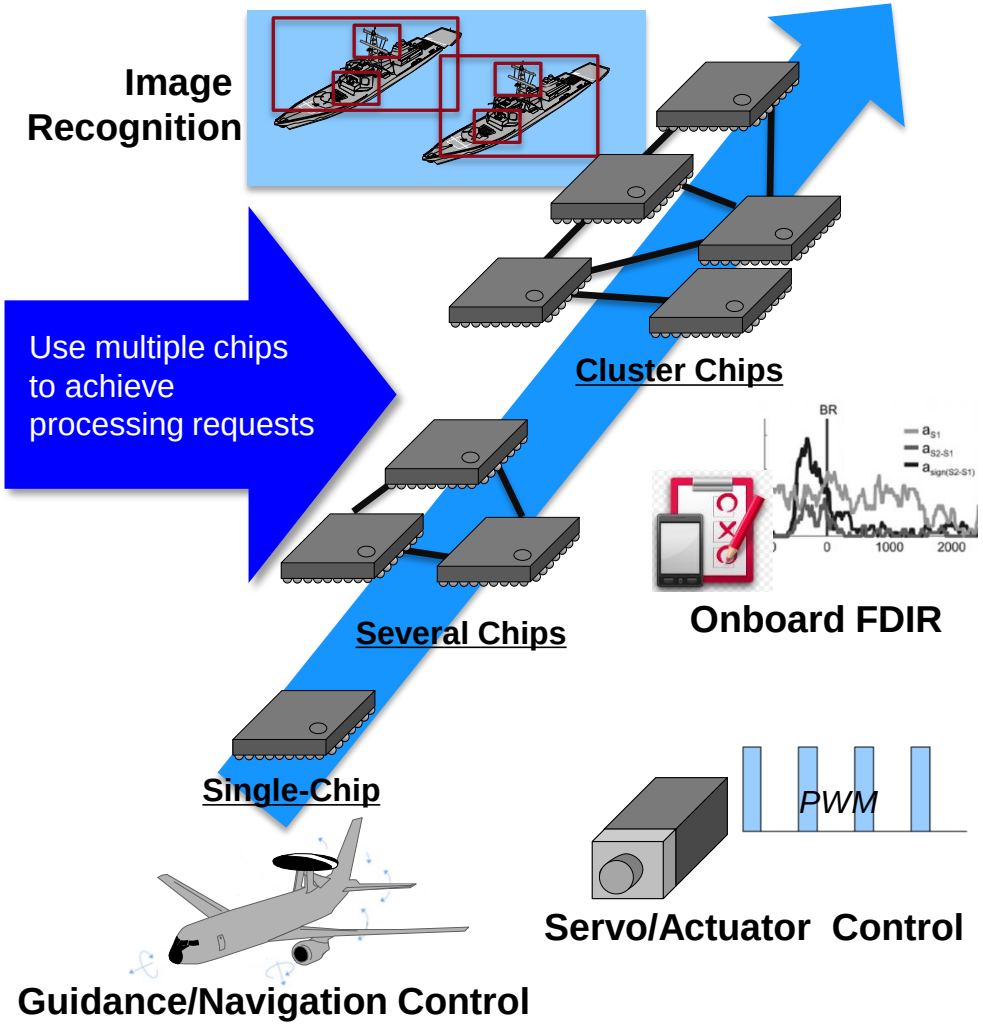
Block Diagram



Communication Interface



SOI-SOCX can realize a scalable computing systems in many field.



Conclusions

■ We introduced the overview and current status of our products.

✓SOI-SOC2 is the flight proven microprocessor.

✓SOI-SOC3 is the improved model of SOI-SOC2 which has the high-reliability and the high performance SpaceWire engine. It will release in the coming year.

✓SOI-SOCX is the next-generation model which will improve processing performance, power efficiency, etc. It will release in 2020.

Thank you for your attention.
Please feel free to contact us.

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