RC64™—Rad hard high performance DSP manycore

by Mr. Ran Ginosar & Tsvika Israeli (Ramon Chips)

RC64™ is a rad-hard manycore DSP combining 64 VLIW/SIMD DSP/CPU cores, lock-free 4 MB EDAC-protected shared memory, a hardware scheduler and a task-based programming model. The hardware scheduler enables fast scheduling and allocation of fine grain tasks to all cores. First silicon prototypes are available since August 2017. RC64 achieves 50 16-bit GMACS and 25 single precision GFLOPS, 120 Gbps SpaceFibre connectivity, 38 Gbps LVDS exchange with ADC/DAC, and over 6 Gbps data rate to EDAC-protected external DDR3 memory. All I/O is directed at the shared memory, and the DSP/CPU cores communicate exclusively with the shared memory—they neither talk to each other nor to any I/O.

RC64 is designed to withstand at least 300 kRad TID, to be resilient to latchup, to be protected of SEU and to auto-recover recover from SEFI. The processor includes enhanced means for FDIR. RC64 employs novel hardware and software methods for the mitigation of thermal cycling effects.

Ramon Chips will apply a proprietary payload-oriented reduced complexity qualification flow to RC64. As RC64 is not intended for platforms, and since it is designed to perform signal processing rather than life-and mission-critical control, customers have opted to forego full ESCC9000 or MIL-PRF-38535 Class S screening and qualification.

RC64 will primarily be delivered as part of a complete NOGAH™ system, a software-defined digital payload customized by Ramon Chips to the customer's application, typically comprising tens of RC64 chips, enhanced COTS devices such as memories, voltage regulators, ADC/DAC and clock sources, and, most critically, system software and reference application software, optimized for the application and for RC64, and modifiable by the customer. Alternatively, it is possible to directly procure RC64 chips.

SW development tools for RC64 include DSP compilers (C90 and assem), task-graph compiler, shared memory verifier, simulators, many-core debugger, profiler and tracer. An application development flow from Matlab® to RC64 code provides a cost-effective path to implementation. Run-time software avoids an operating system; instead, a thin executive kernel takes care of boot, I/O management, interface to hardware scheduling and support for FDIR. A library of computing kernels, applications, networking, I/O and FDIR functions is also provided.

Several applications are presently being developed for RC64. A wideband DVB-S2x modem enables 1—2 Gbps communication on one RC64, extendable by employing multiple chips. 1D and 2D FFT of various sizes, formats and precisions are investigated. Real-time object detection in hyperspectral images has been demonstrated. Image and signal compression methods are developed. Radio and RADAR processing algorithms include spectrum analysis, interference mitigation and digital beam forming. Communication tools include channelization, switching, routing, and deep packet inspection. Other applications include resilient storage, fault tolerant computing and machine learning. A key area supporting other application is cyber defense and protection.