GR740 and GR716 (and GR712RC) Development Status and Applications

Space Processors: High Performances Symmetric/Asymmetric Multicore

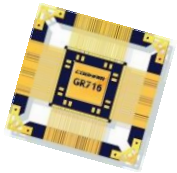
ADCSS 2017

ESTEC, Noordwijk, The Netherlands

2017-10-19

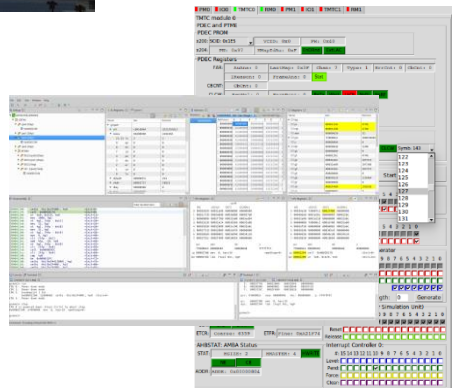
Introduction / Agenda

- Current, and in-development, space microprocessors
  - GR712RC – Existing space-grade microprocessor
  - GR740 – Next generation microprocessor
  - GR716 – LEON microcontroller development



- Applications

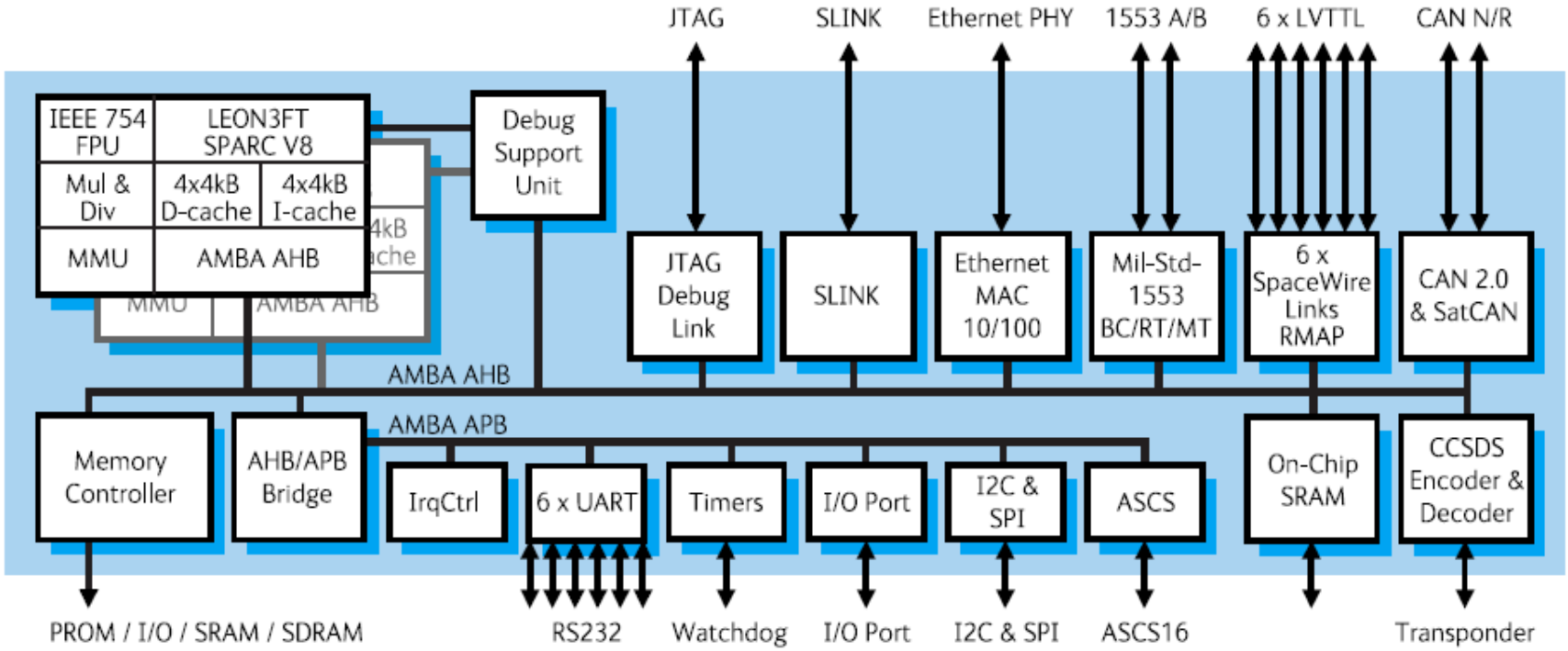
- Software ecosystem
  - Toolchains update



- Outlook: Future developments of processor IP, standard products, and the supporting software ecosystem

GR712RC Dual-Core LEON3FT Processor

50 project wins and 50 projects in evaluation as of Jan 2017

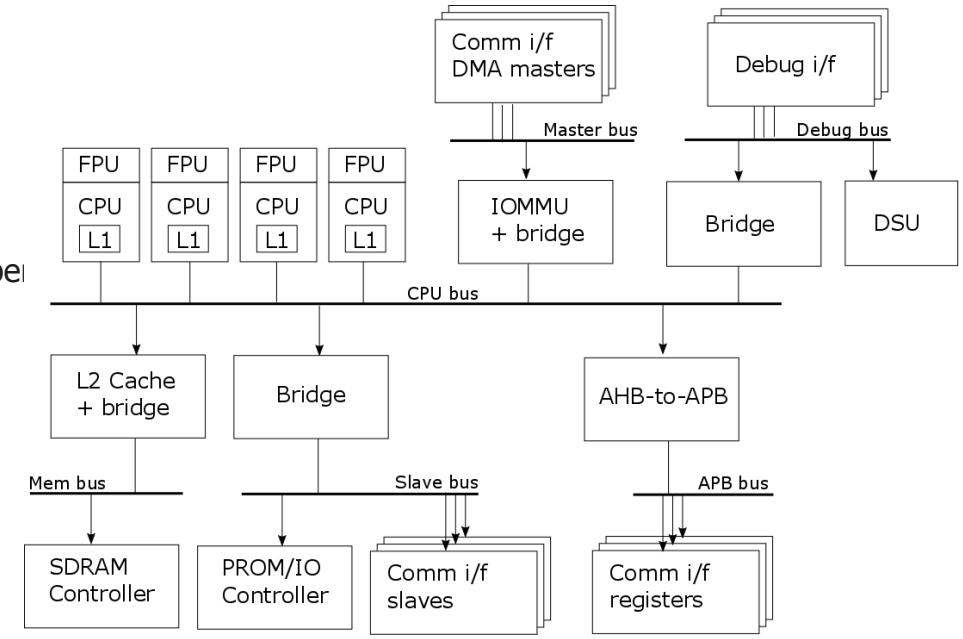


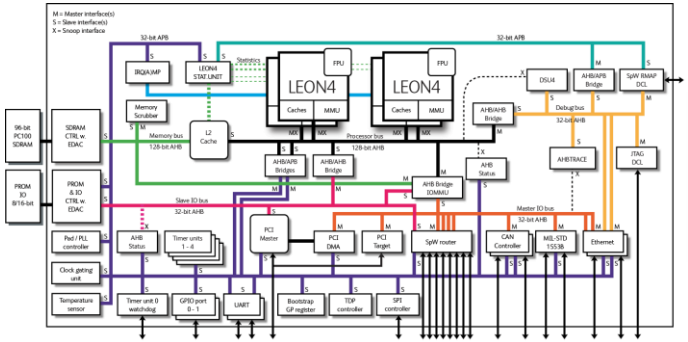
- TowerJazz 180 nm CMOS technology: Ramon RadSafe cell library
  - TID 300 Krad(Si); SEL: LET > 118 MeV/cm2/mg; 1.8V core, 3.3V I/O voltage
- Power consumption (typical): 15 mW / MHz (dual core, MMU, FPU)
- Dual Core LEON3FT Fault-tolerant processor (SMP)
  - 32 KiB cache with 4 parity bits per word
- CQFP240, 0.5 mm pitch, 32x32 mm, hermetically sealed
- Assembly by HCM/SERMA in France

Next step - Quad-Core LEON4FT

Architecture - designed for multi-processing

- System-on-chip
  - 4 x LEON4 fault tolerant CPU:s with MMU, FPU
  - 16+16 KiB Level-1 I+D cache, separate per CPU
  - 2048 KiB Level-2 cache, shared between CPUs
  - PLLs for clock generation
  - SDRAM memory controller with EDAC and scrubbe
  - PROM memory controller with EDAC
  - Communication interfaces
- Targeting general-purpose payload processing.
- Separated debug subsystem
  - Tracebuffers for on-chip bus and processors
  - Allows continuous read-out of trace data
  - Special instructions for instrumentation
  - Filtering on device before entering buffers
- Extended to support A(S)MP operation
  - Duplication of functionality (IRQ ctrl, timers, …)
  - Peripheral memory ranges spaced further apart
- Peripheral units capable of DMA connect to L2 cache and external memory through IOMMU
- Remote boot – through SpW RMAP, PCI
- Improved processor control interfaces for processor core stop/(re)start without device reset (Si rev 1)

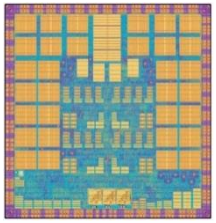


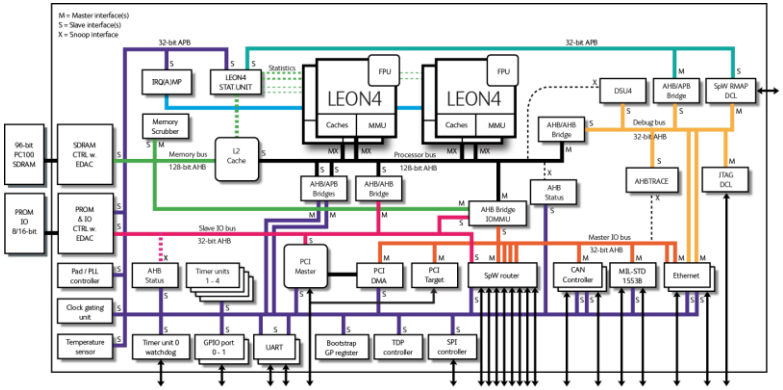


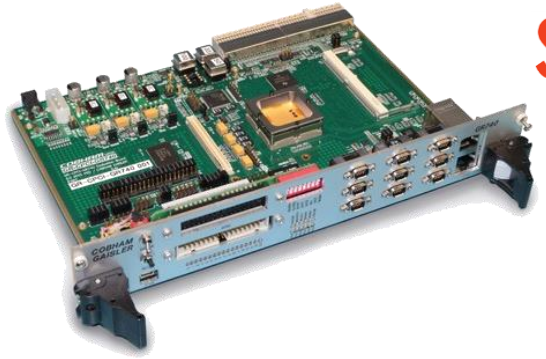
GR740 - Quad-Core LEON4FT Processor

European Next Generation Microprocessor development

- ESA's Next Generation Microprocessor (NGMP)
- Quad-core LEON4FT rad-tolerant SoC device
  - 4x LEON4FT with dedicated FPU and MMU
  - 128 KiB L1 caches connected to 128-bit bus
  - 2 MiB L2 cache, 256-bit cache line, 4-ways
  - 64-bit SDRAM memory I/F (+32 checkbits)
  - 8-port SpaceWire router with +4 internal ports
  - 32-bit 33 MHz PCI interface
  - 2x 10/100/1000 Mbit Ethernet
  - Debug links: Ethernet, JTAG, SpaceWire
  - MIL-STD-1553B, CAN 2.0B, 2 x UART
  - SPI master/slave, GPIO, Timers & Watchdog
- ST 65nm bulk CMOS process
- LGA625 / CCGA625 package
- Rated 250 MHz. Power consumption (including I/O) at 40°C:
  - 4x CPU: 1.85 W (1700 DMIPS)
- Current work to develop flight model.
- Differences for FM silicon to be listed in v1.7 of the user's manual
  - Backward incompatible change: Boot interface via interrupt controller







SPARC

- See: http://gaisler.com/gr740 for technical note on validation and latest set of documentation.

GR740 updated schedule

As of 18 October 2017

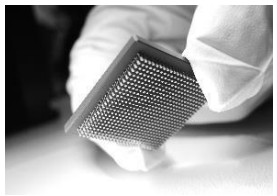
GR740	Status	Milestone	Comments
Phase 2 CCN-1 - redesign	*done*	*2017 July*	*netlist delivered*
Phase 2 CCN-1 - layout		2017 Sep	ongoing
Phase 3a – contract signature		2017 Oct	In negotiation
Phase 3a – new silicon tapeout		2017 Nov	
Phase 3a – new silicon validation		2018 Feb	
Phase 3a – new prototype part delivery		2018 Feb	
Phase 3b – contract signature		2018 Jan	pending approval
Phase 3b – space level assembly		Q1 2018	
Phase 3b – space level screening		Q3 2018	
Phase 3b – space level qualification		Q4 2018	
Phase 3b – space level flight part delivery		2018 Dec	QML-V/Q equivalent
Phase 3b – space level qualification approval		2019 Dec	QML-V/Q

esa
European Space Agency
Agence spatiale européenne

RYMDSTYRELSEN
Swedish National Space Board

COBHAM
Cobham Gaisler AB

life.augmented



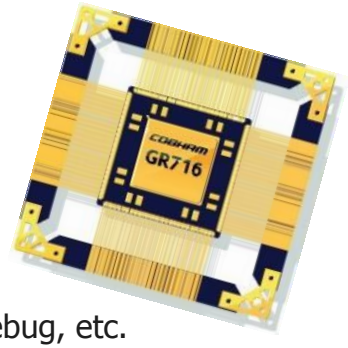
GR716 – LEON3FT Microcontroller

European microcontroller development

COBHAM

Evaluation kits in Q2 2018

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, 50 MHz
  - 16-bit instruction set support to improve code density
  - Floating Point Unit. Memory protection units
  - Non-intrusive advanced on-chip debug support unit
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- SpaceWire interface with time distribution support, 100 Mbps
  - LVDS Driver and Transmitter
- MIL-STD-1553B interface
- CAN 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- ADC 11bits @ 200Ksps, 4 differential or 8 single ended
- DAC 12bits @ 3Msps, 4 channels
- Multi-channel DMA controller
- External ADC/DAC controller
- Mixed General purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm
- **FM partially funded. Current outputs are prototypes and eval board.**



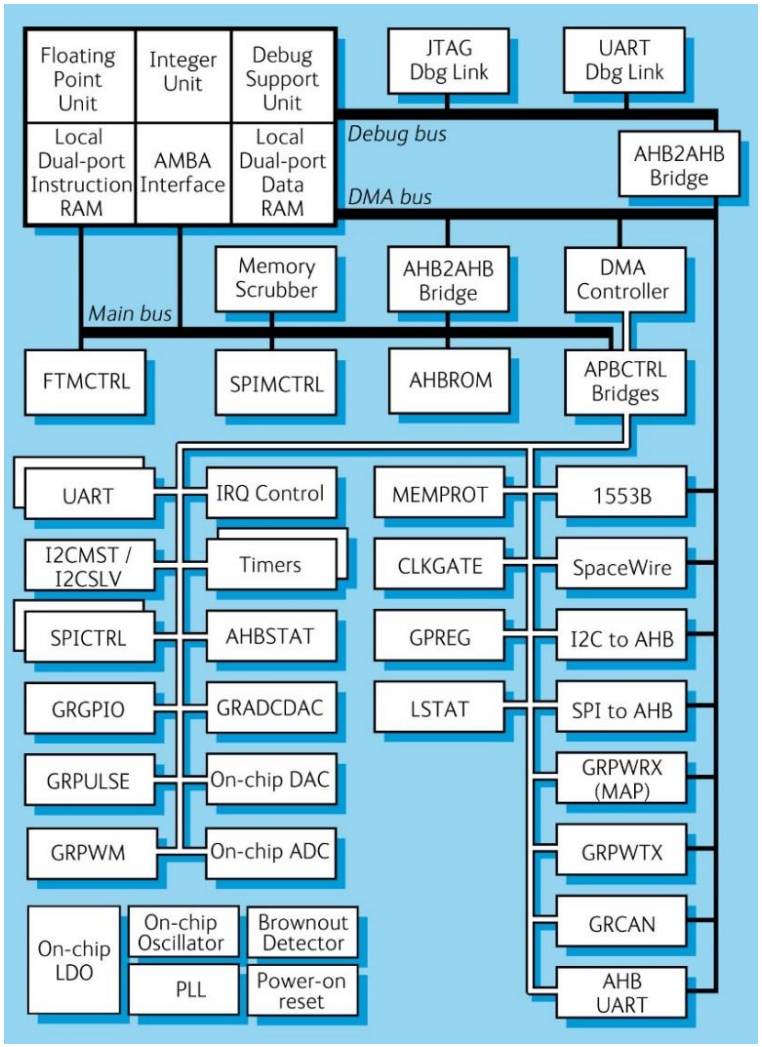
COBHAM
Cobham Gaisler AB

imec

UMC

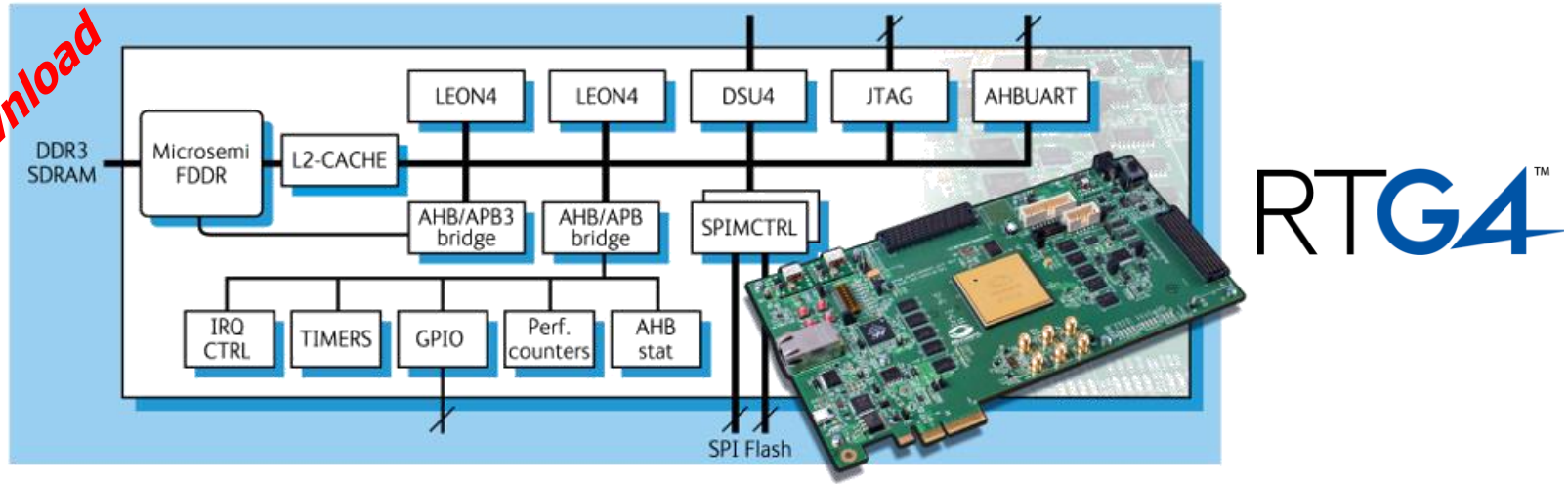
micross components

SPARC



LEON3/LEON4: RTG4 evaluation bitfiles

Pre-built evaluation FPGA configurations



- LEON3 / LEON4 configuration bitfiles available from: http://gaisler.com/LEON-RTG4
- Users program bitfiles directly onto their Microsemi RTG4 Development Kits
- RTG4_ES and RTG4 PROTO at 50 MHz.
- GRMON2 evaluation version support
- No cost, no registration
- Example bitstreams unsuitable for flight

- LEON3 designs:
  - LEON3 – SPARC V8 32-bit Processor
  - Dual-core and quad-core
  - ES and PROTO devices
  - GRFPU – High performance or low area
  - L2CACHE – Level-2 cache controller
  - Timers, interrupt controller, UARTs, JTAG debug
- LEON4 design:
  - LEON4 – SPARC V8 32-bit Processor, quad-core
  - L4STAT – LEON4 statistics unit
  - L2CACHE – Level-2 cache controller
  - GRFPU – High-performance IEEE-754 Floating-Point Unit
  - Timers, interrupt controller, UARTs, JTAG debug

GR712RC First Flights

GR712RC Dual-Core LEON3FT processor

MASCOT asteroid lander, launched 3rd of December 2014 on Hayabusa-2 (JAXA)

http://2013.spacewire-conference.org/downloads/SpW2013ProceedingsFinal.pdf

AEROFLEX GAISLER

PENDER ELECTRONIC DESIGN

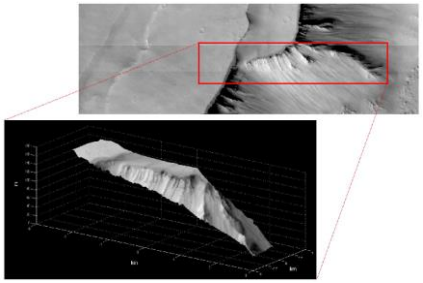
HIREL DESIGN

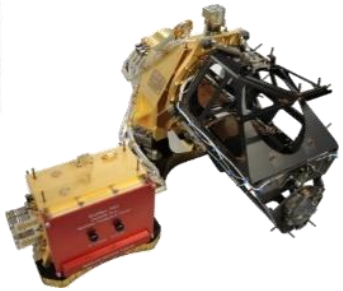
TELESPAZIO VEGA DEUTSCHLAND
A Finmeccanica / Thales Company

DLR

---

b UNIVERSITÄT BERN





CaSSIS (Colour and Stereo Surface Imaging System) launched 14th of March 2016 on ExoMars 2016

www.cassis.unibe.ch

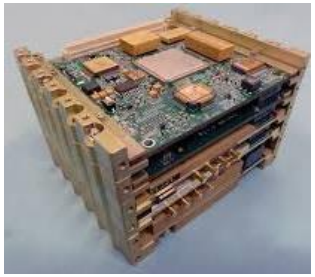
CYGNSS (Cyclone Global Navigation Satellite System), eight satellites launched 3rd of December 2016

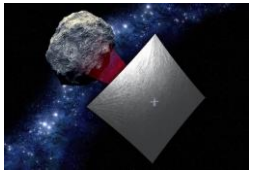
https://www.nasa.gov/cygnss

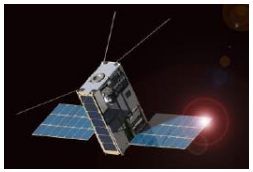
LEON3FT processor in CubeSats

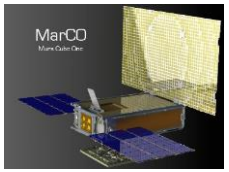
CubeSats using LEON3FT technology

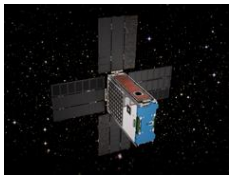
- NEA Scout
  - Marshall Space Flight Center/JPL/LaRC/JSC/GSFC/NASA
  - Near Earth Asterioed Scout
  - **JPL - SPHINX - GR712RC**
  - JPL - IRIS radio – LEON3FT IP
- Lunar Flashlight
  - JPL / NASA
  - Map Polar Surface Ice, search for ice in lunar craters
  - **BCT XACT – LEON3FT IP**
  - JPL - SPHINX - **GR712RC**
  - JPL - IRIS radio – LEON3FT IP
- BioSentinel
  - NASA Ames Research Center
  - BCT XACT – LEON3FT IP
  - **MODAS - Space Dynamics Lab – UT699**
  - JPL IRIS radio – LEON3FT IP - TBD
- MarCO
  - JPL / NASA
  - Mars telecom Relay Demo
  - InSight insertion real-time Mars relay
  - BCT XACT / XB1 Bus - LEON3FT IP
- CuSP
  - SwRI / NASA / GSFC / JPL
  - CubeSat mission to study Solar Particles
  - **JPL - IRIS radio – LEON3FT IP**
  - SwRI - SATYR - **GR712RC**
  - Southwest Deep-Space Explorer (SDX-6)
- JUMPER
  - JPL NASA / SwRI, LASP
  - JUpiter MagnetosPheric boundary ExploreR
  - **SwRI - SATYR GR712RC**
  - JPL - IRIS radio – LEON3FT IP

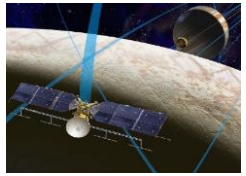










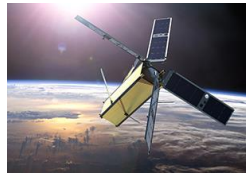
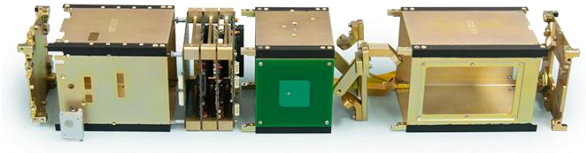
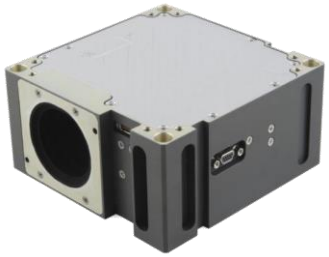


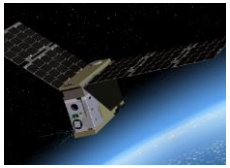
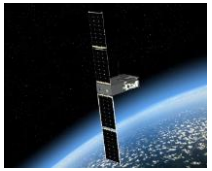
LEON3FT processor in CubeSats

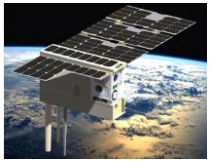
CubeSats using LEON3FT technology

- Inspire
  - JPL / NASA
  - Interplanetary Nano-Spacecraft Pathfinder in Relevant Environment
  - JPL IRIS radio – LEON3FT IP
- LunaH-Map
  - JPL / NASA / ASU
  - Lunar Polar Hydrogen Mapper
  - BCT XACT – LEON3FT IP
  - JPL IRIS radio – LEON3FT IP
- Lunar IceCube
  - Morehead State University, NASA GSFC
  - BCT XACT – LEON3FT IP
  - JPL IRIS radio – LEON3FT IP
- ORS Tech 1, ORS Tech 2
  - JHU/APL
  - LEON3FT IP
- Space Dynamics Labs – Pearl platform
  - **Picosatellite Exo-Atmospheric Research Laboratory**
  - Multicore LEON3FT SBC 25 to 266 MHz
  - SDL - Modular Avionics System (MODAS) SBC
- Blue Canyon Technologies – FlexBus / **XB spacecraft bus**
  - **XACT - LEON3FT IP**
  - S5 - AFRL
  - ACSENT - AFRL
  - RAVAN - JHU/APL
  - PlanetiQ 1-12 - PlanetiQ
  - CubeRRT - Ohio State, NASA
  - CSIM FD - University of Colorado
  - TEMPEST-D - Colorado State, JPL
  - HaloSat - University of Iowa / NASA
  - MinXX - University of Colorado, NASA



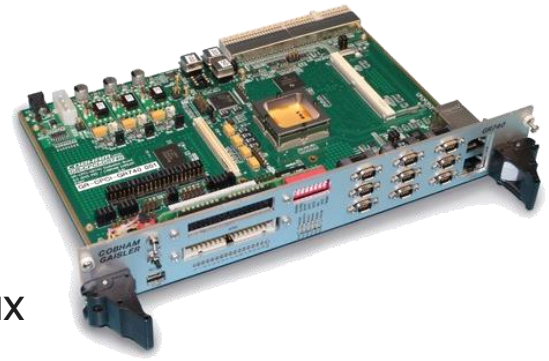





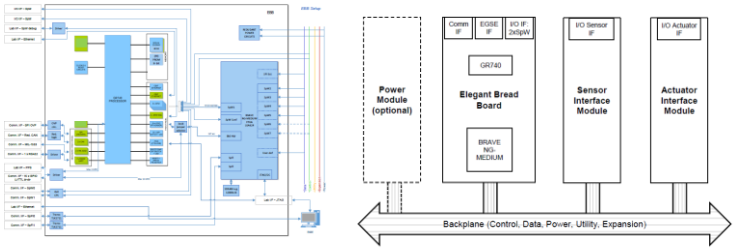





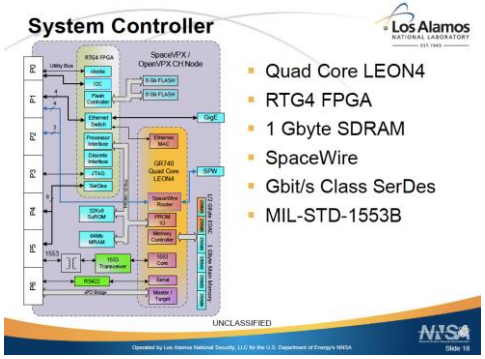
GR740 Adoption

- Primarily used with GR-CPCI-GR740 board
- Users now immediately start using all cores (different case than GR712RC)
- Different starting points for multi-core:
  - Start with bare-C images – or – Leap to using SMP Linux
  - RTEMS with AMP configurations – Part of this group expected to transition to RTEMS-SMP
  - VxWorks (already SMP capable since 6.7)
- Flight and development board at customers





ESA Compact Reconfigurable Avionics – Data Handling Core



"Adopting SpaceVPX at Los Alamos", Rob Merl and Paul Graham, MAPLD2017

Software ecosystem

Toolchains, OSs, runtimes, tools

- Available free open-source compilers and kernels:
  - BCC: GNU GCC compiler with LEON BSP, for standalone applications
  - BCC2: LLVM & GNU GCC compiler, for standalone applications
  - RTEMS: "Real-Time Executive for Multiprocessor Systems"
  - Linux 2.6 – 4.9
- LEON port and BSP for commercial operating systems:
  - VxWorks 6.x/7.x
  - ThreadX-5.0
- Ada support: Toolchain from AdaCore (F)
- RTEMS 4.8 EdiSoft and in-house variants at various companies
- Other OSs/environments already ported to LEON include: PikeOS, XtratuM, …

- Tools: GRMON debugger, Eclipse IDE available, TSIM2 and GRSIM Simulators

Software ecosystem

Operating systems, verification

- Goal: You can pick any available software environment for any LEON device
- Limitations exist:

Software	UT699(e), UT700, GR712RC	GR740	GR716	SSDP	LEON3/4 generic
BCC / BCC2	✓	✓	✓	✓	✓
RTEMS	✓	✓	✗	✓	✓
Linux	✓	✓	✗	✓	✓ (MMU)
VxWorks	✓	✓	✗	✓	✓
ThreadX	✓	✓	✓	✓	✓

- Drivers: Provided by Gaisler as-is. Qualified drivers at customers
- Software V&V: Heavy use of TSIM2 simulator for code coverage analysis
  - GR740 and beyond have specific instructions for instrumentation – used together with trace buffer filtering to get execution traces in real time.

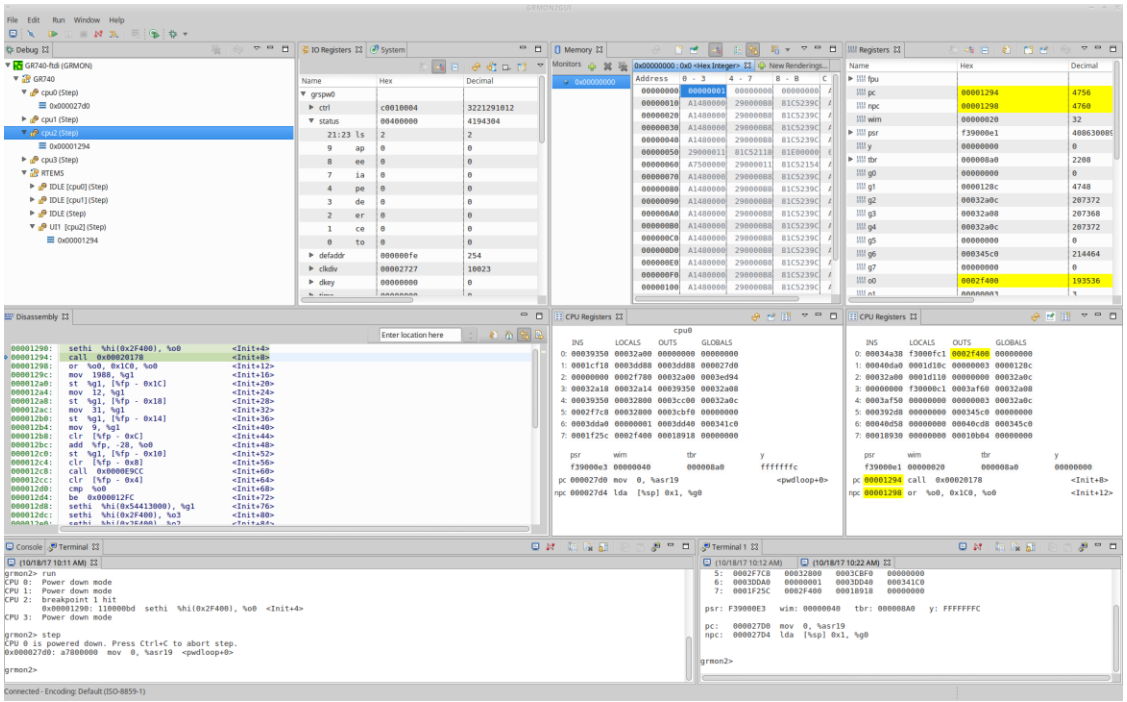
Toolchains update

BCC2, GCC updates, VxWorks 7, RTEMS 5, Linux 4.9

- BCC2, new bare-metal toolchain released in may 2017:
  - LLVM-4.0 support (first LLVM toolchain from CG)
    - New backend for LEON-REX 16-bit ISA (GR716)
    - Relies on Binutils for linking
    - Uses assembler and compiler from LLVM
  - GCC-4.9
  - C11 & C++11 support
  - Newlib 2.5.0
  - multi-core ASMP support in BCC run-time (GR740, GR712RC)
  - BCC run-time reworked to improve interrupt latency and lower footprint (GR716)
- Long-term GCC-7.2 toolchain support for LEON, will be used for:
  - RTEMS-5.1
  - VxWorks 7
- VxWorks 7 release in October 2017.
- RCC-1.3 (RTEMS-5) second pre-release in October 2017. Including new GR740 BSP with SMP support funded by ESA.
- Linux 4.9 LTS release in October 2017.

Software outlook

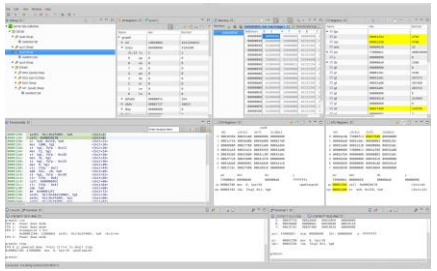
- TSIM3
  - multi-core simulator, improved configuration, replaces GRSIM and TSIM2.
- LLVM LEON backend support
  - Planned continued collaboration with ESA. Planned for RCC-1.3 (RTEMS-5)
  - Targeted optimizations for GR712RC and GR740
- BCC2 updates
  - GCC 7.2
- GRMON-GUI available in 2018.



Software outlook

GRMON-GUI

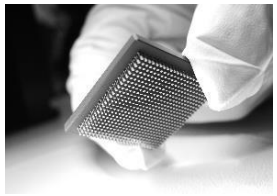
- Graphical hardware debugger for LEON available in 2018 Q1.
- Built on state of the art Eclipse TCF technology used/maintained by leading embedded vendors WindRiver and Xilinx
- Responsive user interface:
  - fetching only target data displayed in GUI
  - Eclipse closely interfaced to target HW (no GDB in background)
  - new caching architecture
  - GRMON optimized for processors used in space (AT697, GR712RC, GR740, ..)

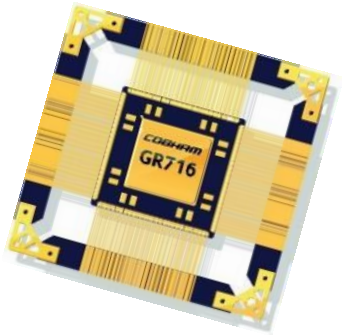


- Provides same functionality as GRMON CLI plus Graphical UI
- Integrated with CLI, execution control via CLI or GUI or mix (single-step, breakpoint, …)
- Targets custom GRLIB ASICs, existing LEON chips and non-CPU systems
- Multi-core support. User extensible by means of eclipse plug-ins and Tcl scripts
- GUI features in short:
  - Execution threads and CPUs view (RTEMS/VxWorks/BCC)
  - Dissassembly view, System view (info sys), I/O register view (info reg)
  - Optimized LEON register view
  - VT100 Tcl terminal view with tab-completion, history, etc.
  - Application terminal (UART tunnelling) view

Demo in ADCSS 2017 booth!

Hardware outlook





- GR740 FM availbility
- GR716 prototype development kit
- Hardware design / IP library:
  - Architectural improvements/extenions/upgrades
  - SPARC32 line continues with the LEON5
  - New IP: High-speed serial link, memory controller, accelerators
  - HPP/GPP track vs. uC track
  - IP certifications
- ”GR745”: GR740 design plus the following enhancements:
  - Architectural improvements for higher compute performance
  - Extended support for time and space partitioning
  - More efficient virtualization support, hypervisor mode in HW
  - Move to DDR2/3/4 memory for performance and capacity
  - High-speed serial interfaces (SpFI / SRIO)
  - Flipchip packaging for improved pin count and signal integrity
- HW+SW: Trace solutions

THANK YOU FOR LISTENING!