11th ESA Workshop on Avionics, Data, Control and Software Systems (ADCSS-17)

New Generation Transportation Avionics Test Bed

gmv INNOVATING SOLUTIONS

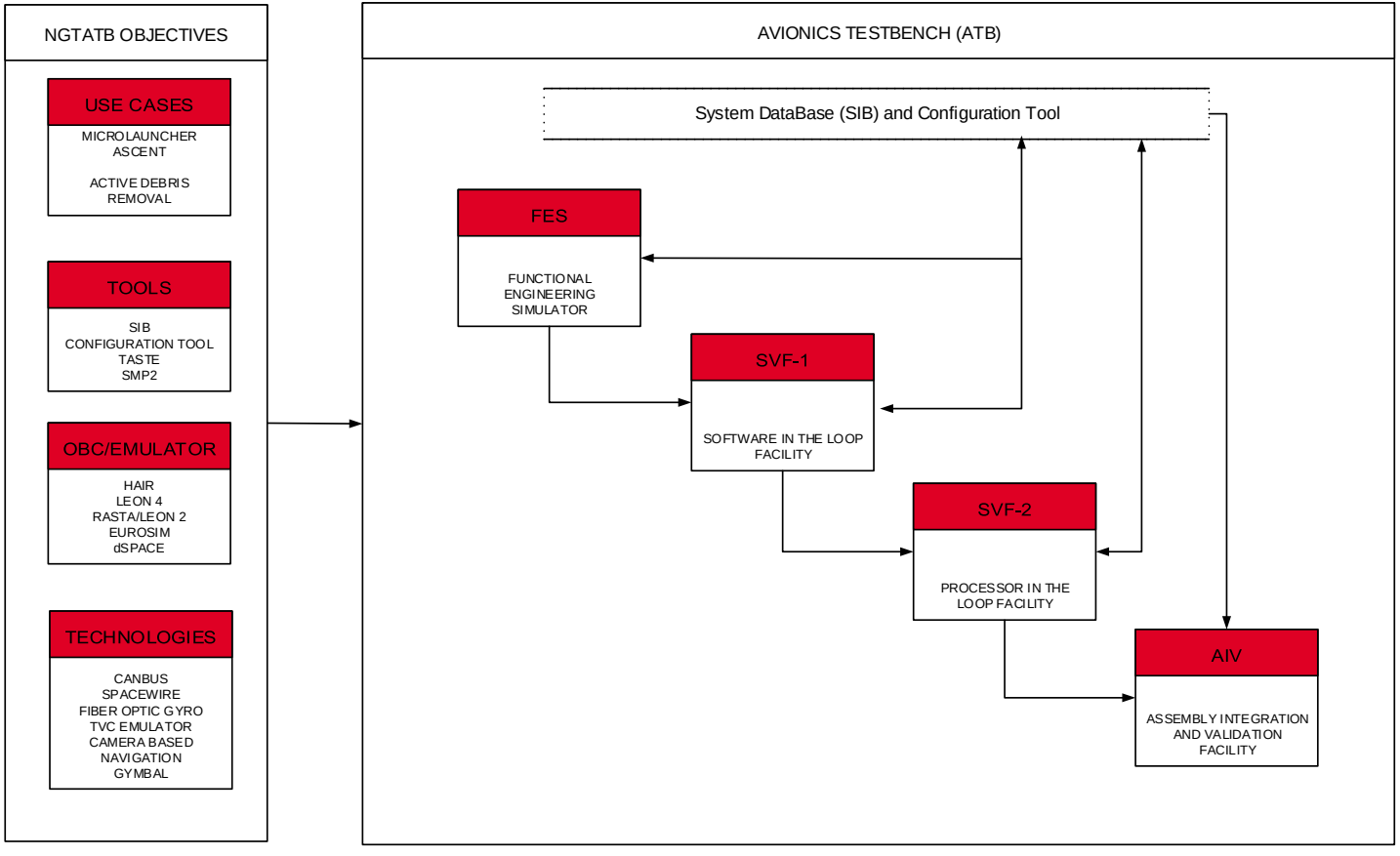
Project Background and Objectives

- The concept of Avionics Test Bench (ATB) is here intended as the integration of:
  - System oriented SW
  - Hardware simulators
  - OBC emulators
  - Real HW allowing to verify and validate the specification of a space avionics system.

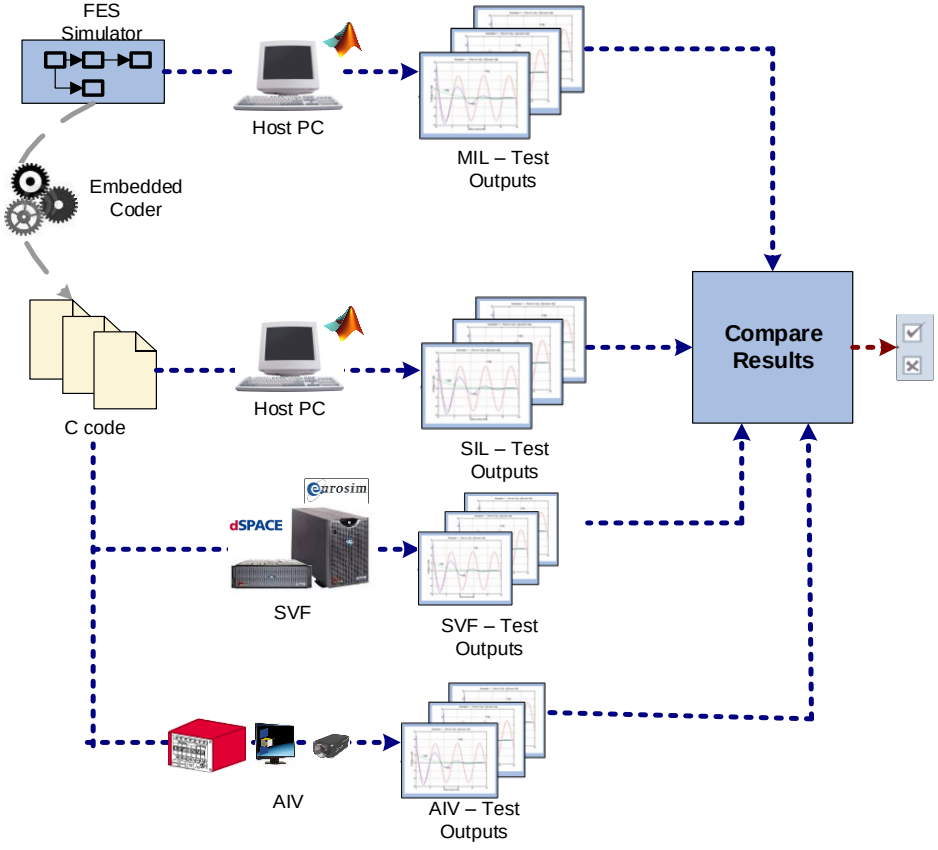
- ATB architecture implemented in this project permits performing several activities, being the most relevant (use cases):

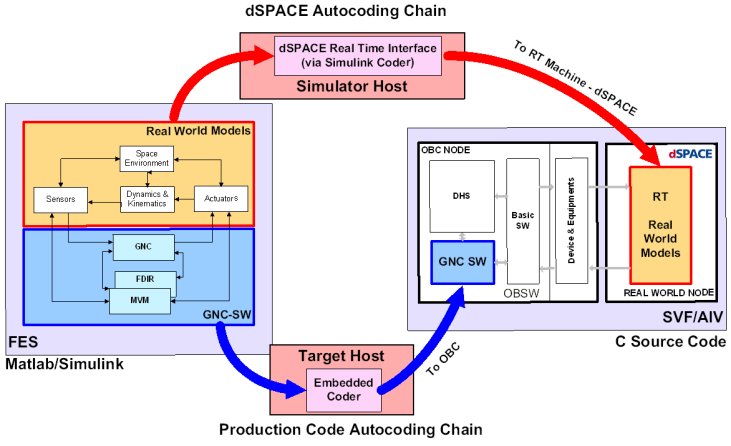
  - Pre- and Post-flight analysis for ESA space missions.
  - Standards and technology demonstration.
  - Technology assessment in support of projects.
  - Staff competence related activities

Project Background and Objectives



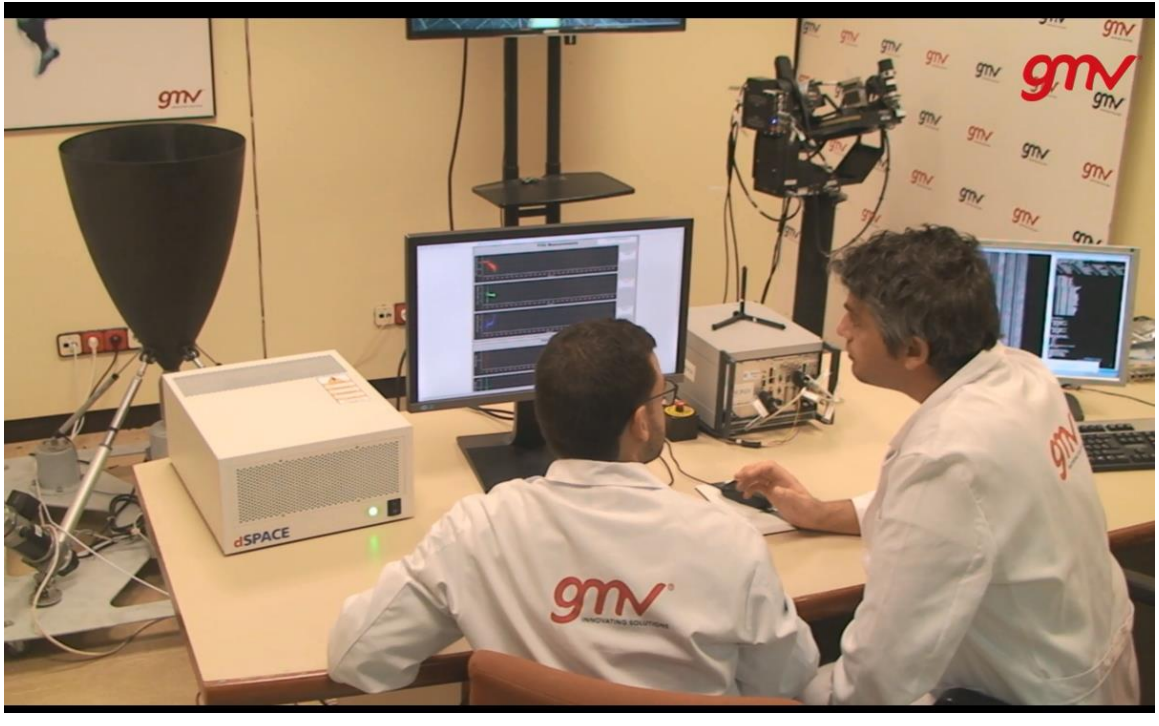
ATB V&V Approach





Project Background and Objectives

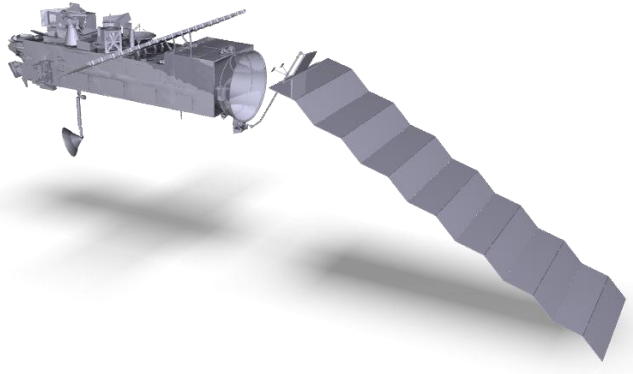
- The main goal of NGT-ATB has been to improve the existing ATB infrastructure in terms of
  - Use Cases and Mission Scenarios
  - OBC/Emulators
    - HAIR Multicore Emulator
    - Leon 4/ Multicore
  - Technologies
    - TVC Emulator
    - Gymbal/FOG
    - SpaceWire/CanBus
  - Tools
    - System DataBase
    - Configuration tool
    - Taste
    - Visualization Tool



Two Scenarios Considered

- Micro Launcher Ascent Scenario

- Active Debris Removal

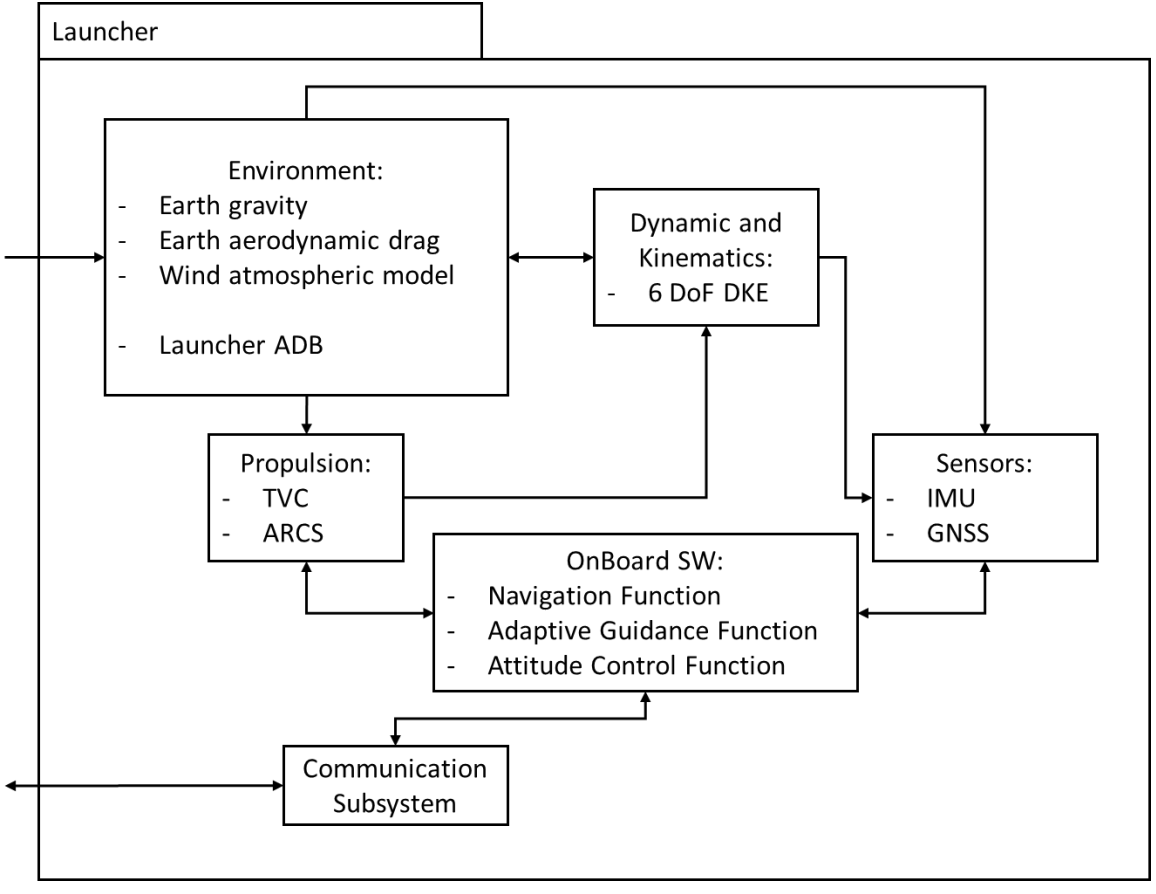


FES Instantiation

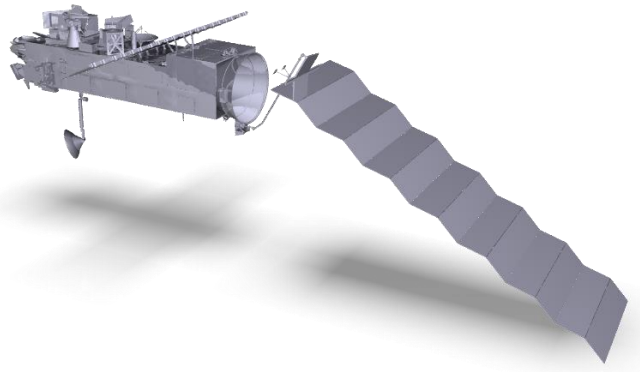
FES CONFIGURATION

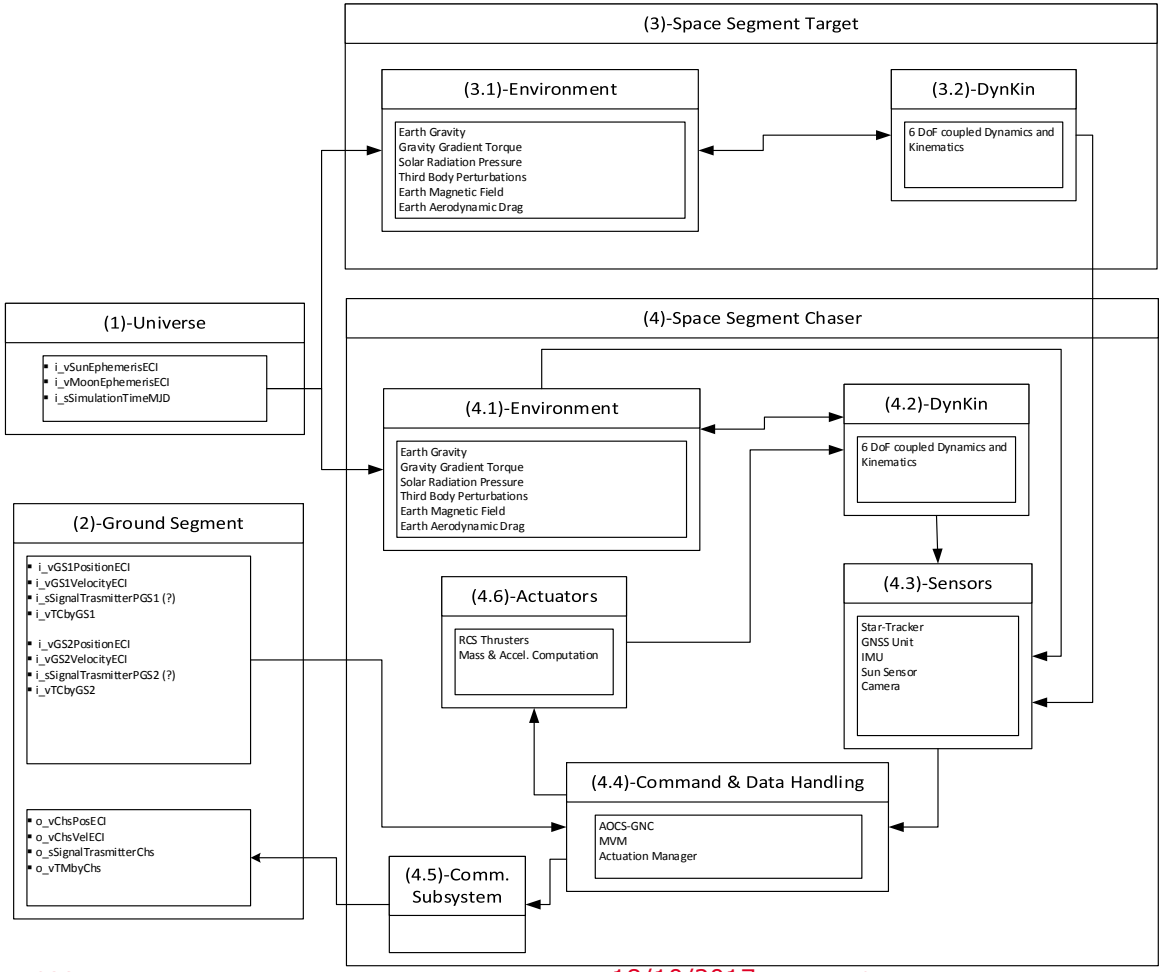
- The FES configuration (or GNC-MIL) of the NGT-ATB supports the following main system functional design and validation activities:
  - Support the system requirement consolidation
  - Validate the key algorithms needed in the system (e.g. GNC, AOCS)
  - Trade-off different design alternatives
  - Verify system preliminary and detailed design
  - Validate the system performance through a set of analyses

LAU-FES Configuration



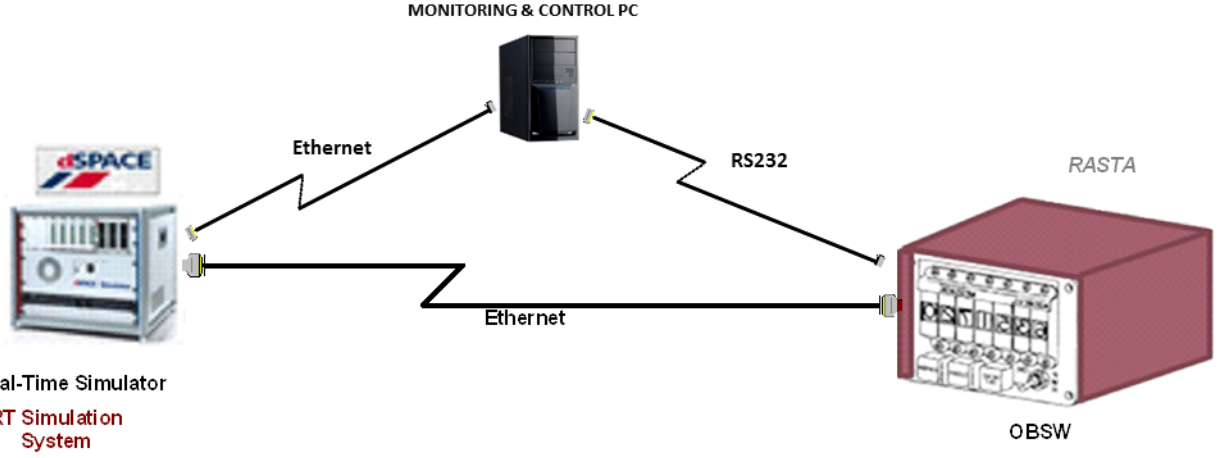
ADR-FES Configuration





SVF Instantiation

SVF-LAU Configuration



- SVF-LAU based on three main elements connected via Ethernet:
  - **dSPACE** machine running Real World simulated models
  - **RASTA** with **LEON2** board running GNC SW
  - **PC** to monitor and control simulation for both dSPACE and LEON2

SVF-LAU Architecture Overview

- PIL set-up for LAU-SVF is based on:
  - Real-World RT Simulator: **dSPACE DS1007** board
  - RASTA: **GR-RASTA-101** with **LEON2** board
  - Monitoring and Control PC: **Windows PC**
  - **Ethernet UDP/IP**
  - **Serial RS232**

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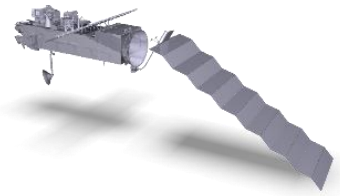
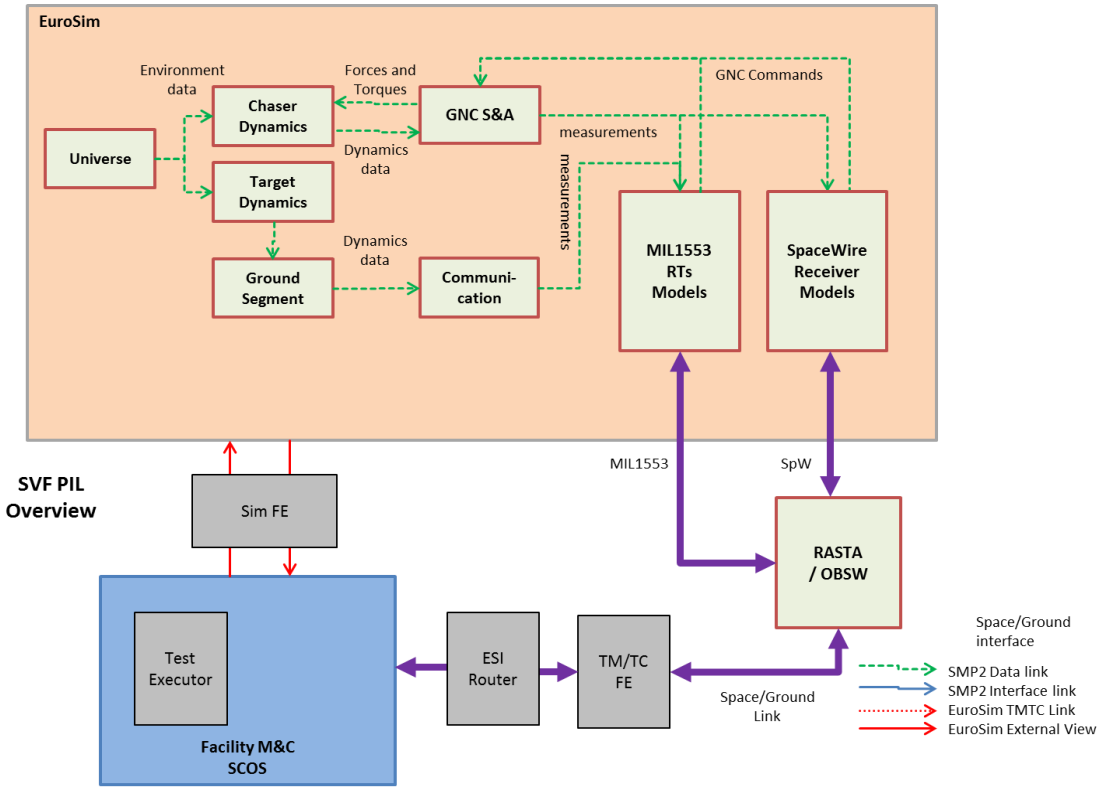


SVF-ADR

Simulation Composition

- EUROSIM RW
  - Autogenerated SMP2 Models
  - Spacewire SMP2 Model
- LEON-4 OBSW
  - Autogenerated GNC Code
  - Basic layer OBSW (TM, Data Disp)



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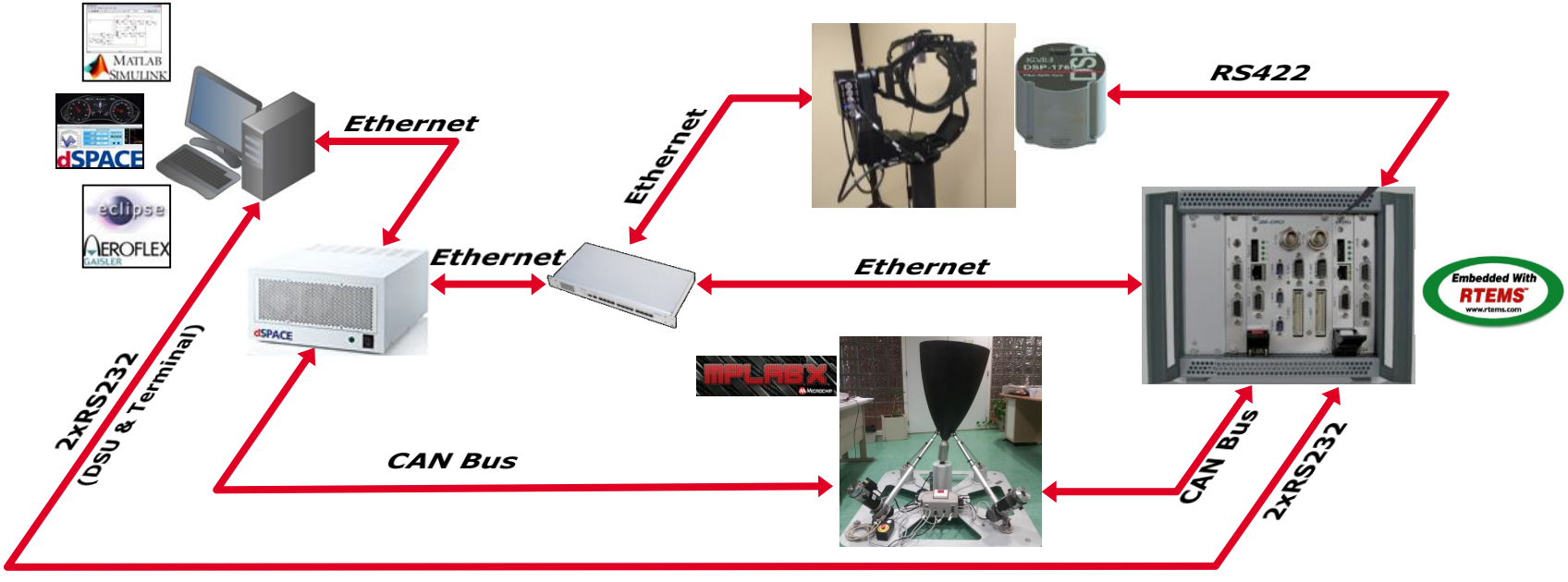
AIV Instantiation

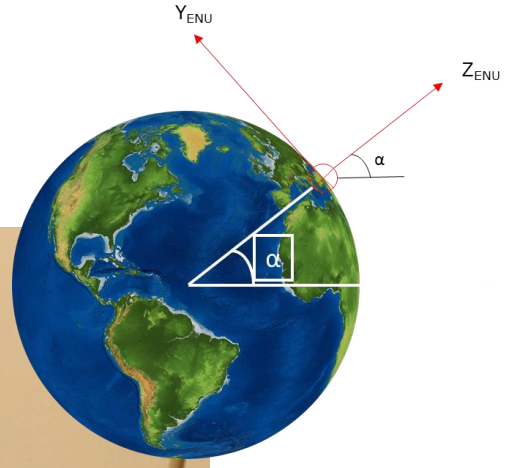
AIV-LAU HW & SW Architecture

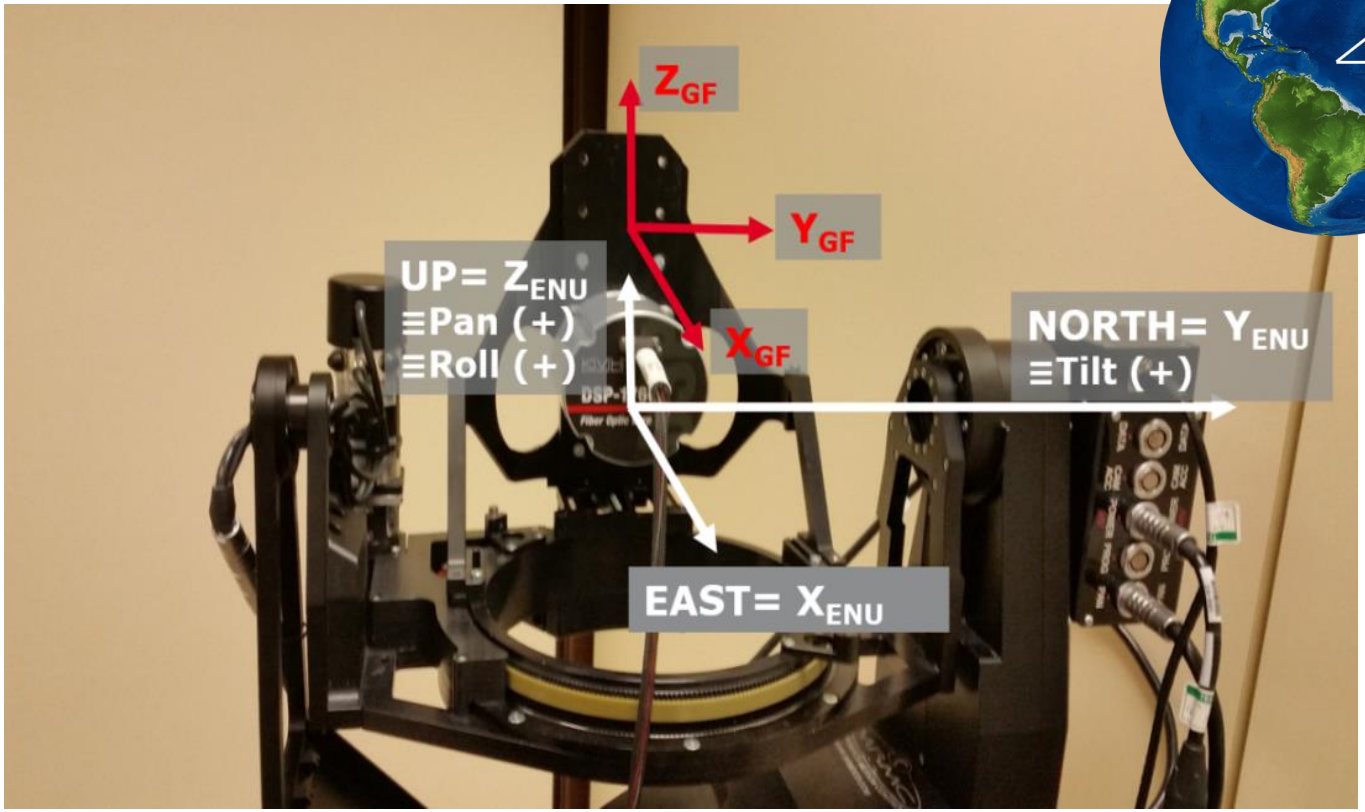
LAU-AIV Hardware architecture is including RS232, RS422, Ethernet & CAN Bus interfaces.

LAU-AIV Software architecture is including Matlab/Simulink, dSpace ControlDesk, Eclipse, RTEMS & MPLAB-X.



Gimbal

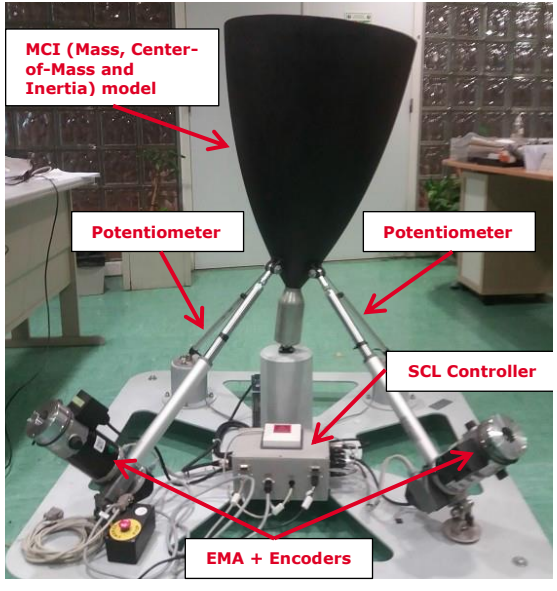

Y_ENU
Z_ENU
α
α


Z_GF
Y_GF
X_GF
UP= Z_ENU
≡Pan (+)
≡Roll (+)
NORTH= Y_ENU
≡Tilt (+)
EAST= X_ENU

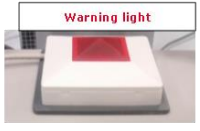
Thrust Vector Control

Thrust Vector Control Architecture

The TVC is composed by the MCI (Mass, Centre-of-Mass and Inertia) model, potentiometers, EMA + Encoders and SCL (Small Control Loop) controller. The SCL unit provides RS232 and CAN interfaces.



Power System equipped with remote power switch and warning light.



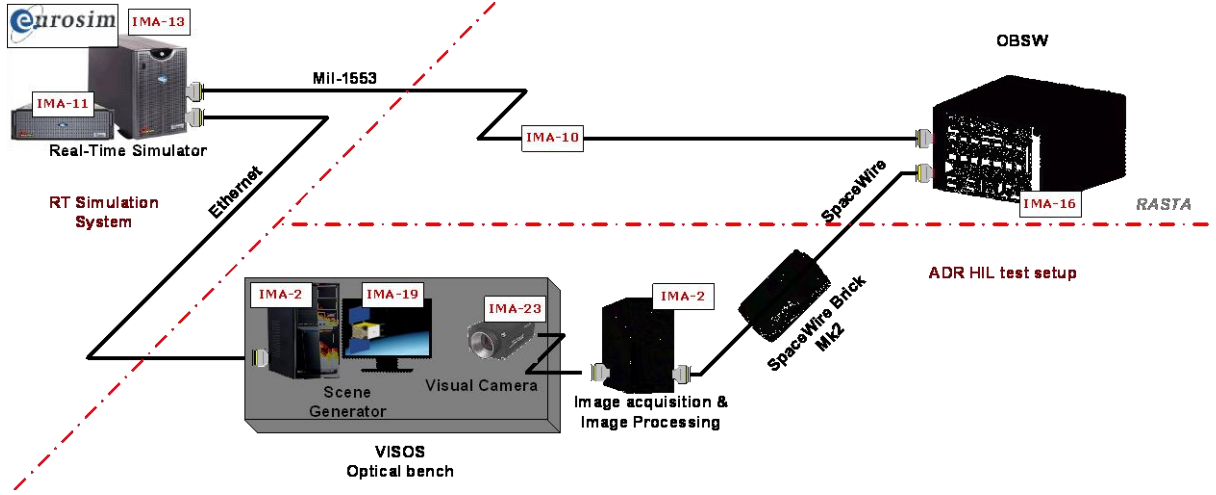
Powerful EMAs: Max load 800N
Encoder resolution 0.0012 mm

SCL is composed by two modules (actuators and observers). The SCL controller is based on PIC microcontrollers.

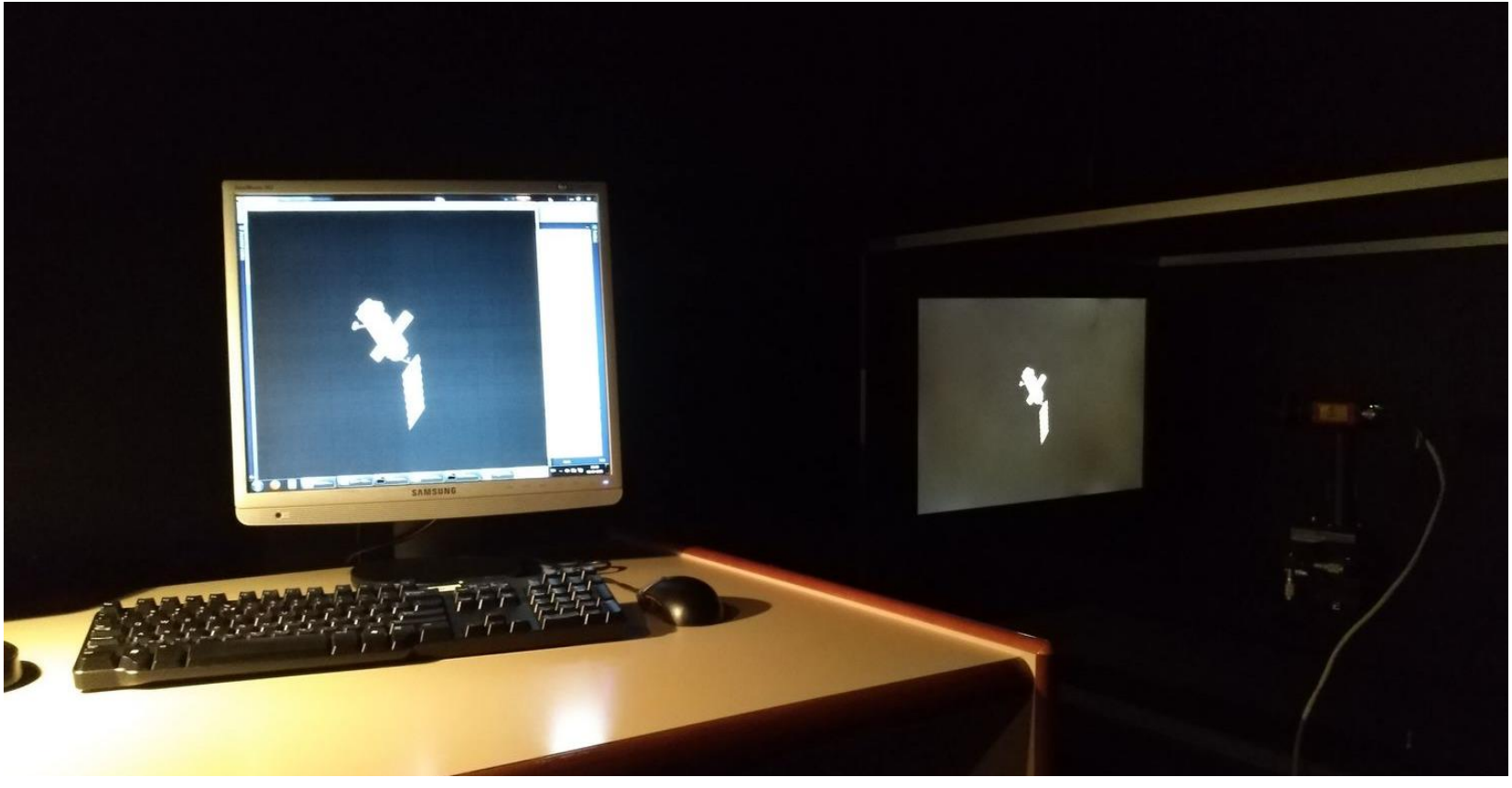
Instantiate AIV–ADR

Configuration based on the implementation of the ADR SVF-PIL

- The Real World models are assembled by the configurator tool starting from the SMP2 generated from the FES.
- This assembly is loaded in EUROSIM and executed in real time providing via Ethernet connection the trajectory data of chaser and target to the VISOS bench that generates the target images that are captured by the camera.
- The raw data from the camera is captured from the PC that performs the image processing algorithms to get the features that are passed to the NGMP board via SpW connection.
- The NGMP board executes the OBSW that generates the commands that are passed to the simulated actuators running in EUROSIM.



AIV-ADR: GMV Optic Lab Settling



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