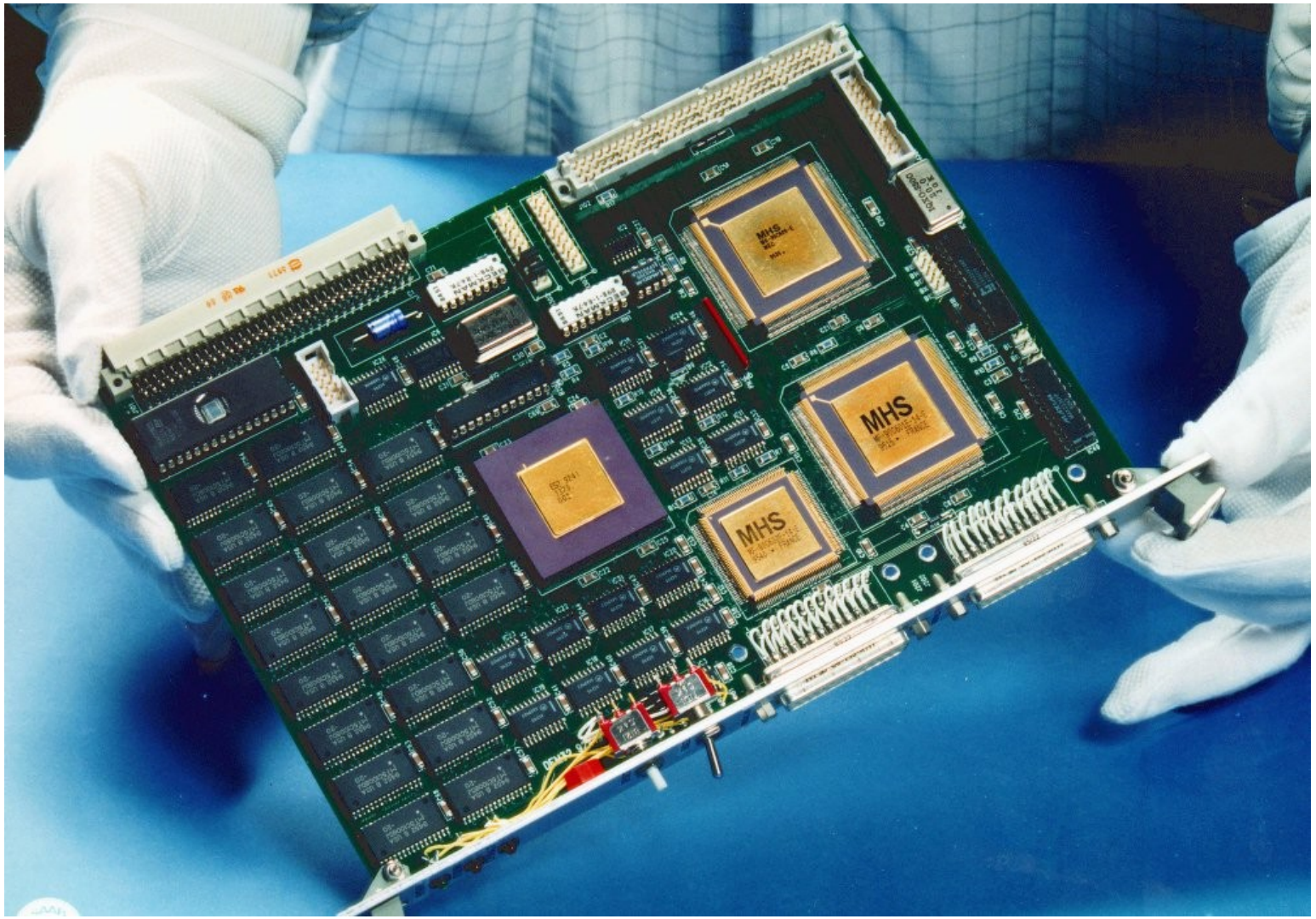
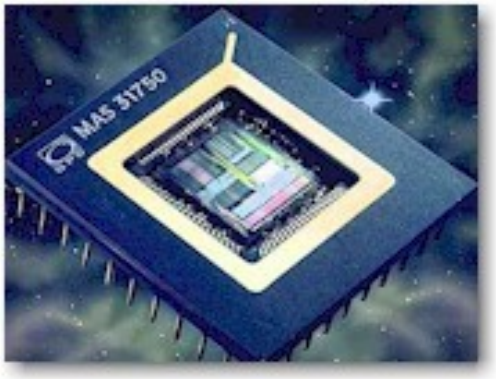
25 Years of SPARC

- a personal retrospective by Jiri Gaisler



First European rad-hard processors

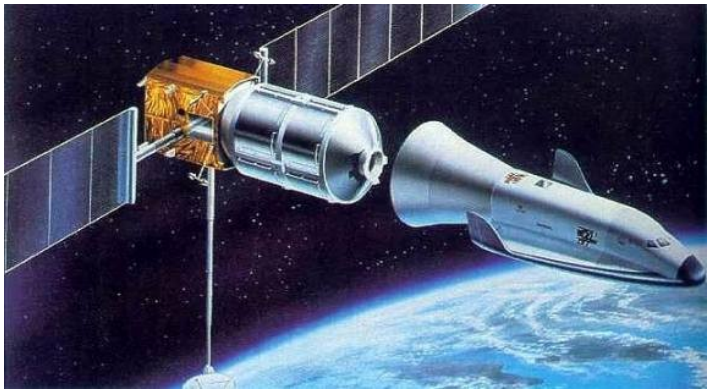
- Based on MIL-STD-1750
  - MAS281 (MDC281 clone): 0.5 MIPS, 3-chip, 1989
  - MA31750, new design, monolithic, 2 MIPS, 1991
- Deemed sufficient for large majority of missions



New challenges

Requirements for a 32-bit processor

- Requirements
  - 10 MIPS, 1 MFLOPS, 1W/MIPS
  - 100 Krad, 50 Kgates
  - European source, non-proprietary
  - Software support (Ada)
- Foreseen missions
  - HERMES spaceplane
  - Columbus MTFF
  - Robotics & planetary exploration



Preparation 1989 - 1990

- Two precursory studies by Saab and Sagem
  - Outcome: THOR, SPARC and MIPS recommended
- Rejected architectures
  - AMD29K, M88K, 80x86, 80960, M68000 : proprietary
  - T800: difficult to port, slow
  - ARM : poor software support

Microprocessor round-table 1990

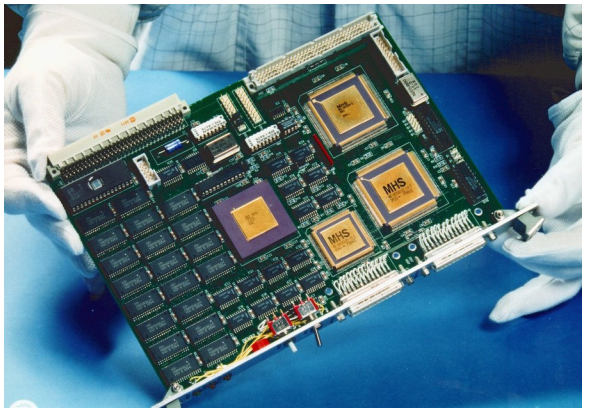
- Short-list for selection
  - SPARC, MIPS, THOR
- 50+ attendees from 25 companies/projects
  - MBB, Aerospatial, Selenia, HERMES, Contraves, Saab, Dornier, CNES, Matra Espace, Alcatel, Alsys, Rtech, MEDL, Sagem, Sextant, BAE, Logica, Laben, DDC, MHS, MSS ...
  - 2-day meeting
- Final choice SPARC
  - Open architecture, no copyrights or patents
  - Compatible with available technology (MHS 0.8 um CMOS)
  - Cache-less operation, breadboard demonstrator

ERC32 project 1992 - 1997

- Start 1992, expected duration 3 years
- 3-chip ERC32 on 0.8 um CMOS (MHS)
- Ada compiler
- Ada tasking accelerator (ATAC)
- Simulator and real-time tools
- VHDL models for board simulation

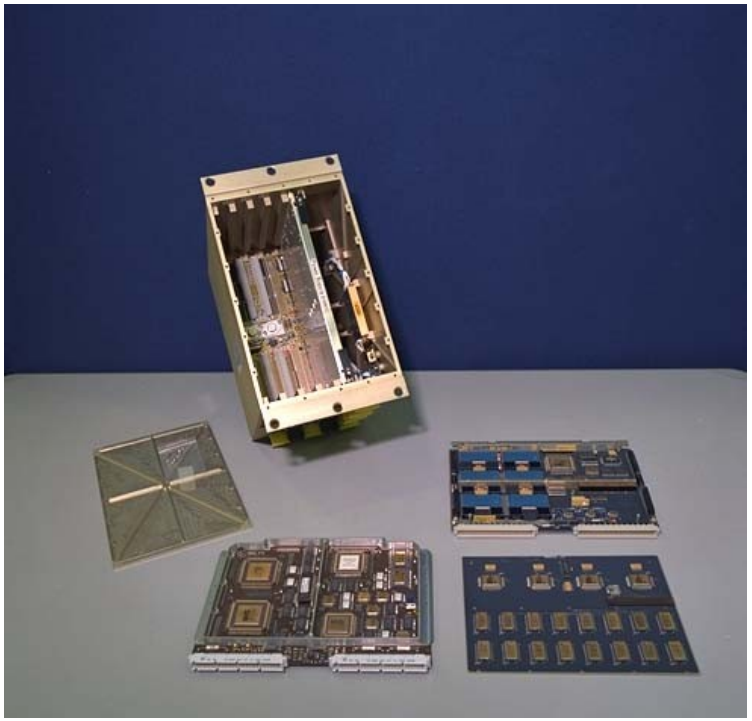
Outcome of ERC32 project

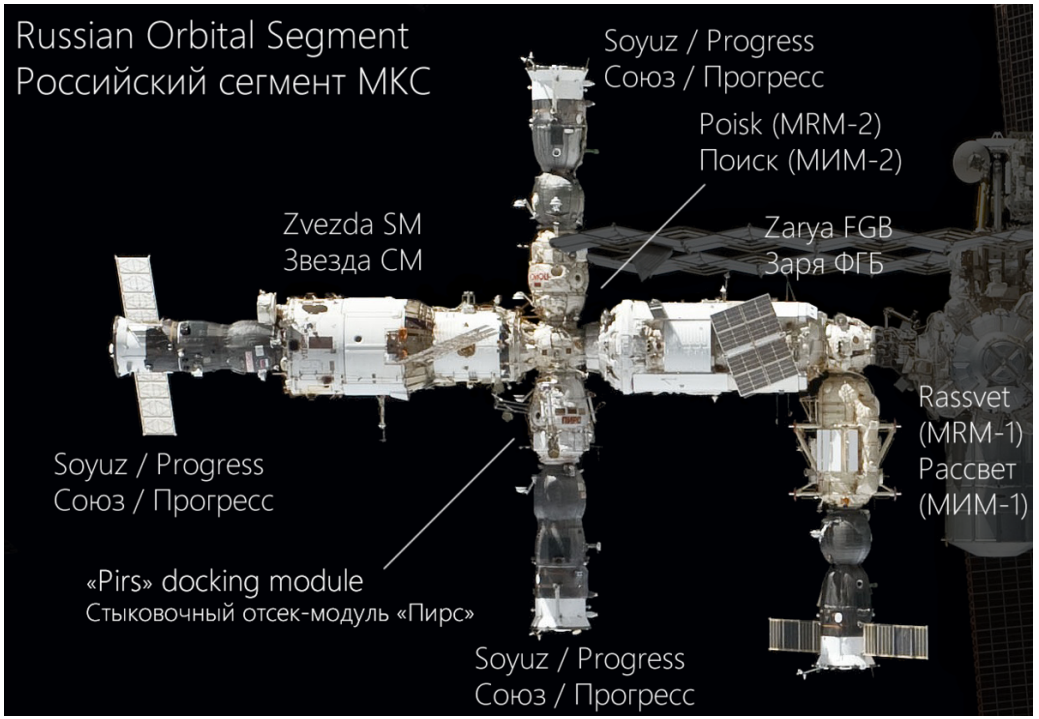
- Project goals mostly met
  - 10 MIPS, Rad-hard, European source
  - ~ 10 iteration of silicon, ATAC canceled
  - Cost of bugs significant to first project



- Interesting facts
  - TSC692E based on Meiko FPU from T800/microSPARC
  - Porting of RTEMS due to delays in Ada compiler development
  - Development of SIS simulator forced by delays in delivery of first ERC32 samples

First ERC32 project – DMS-R





ERC32 successor

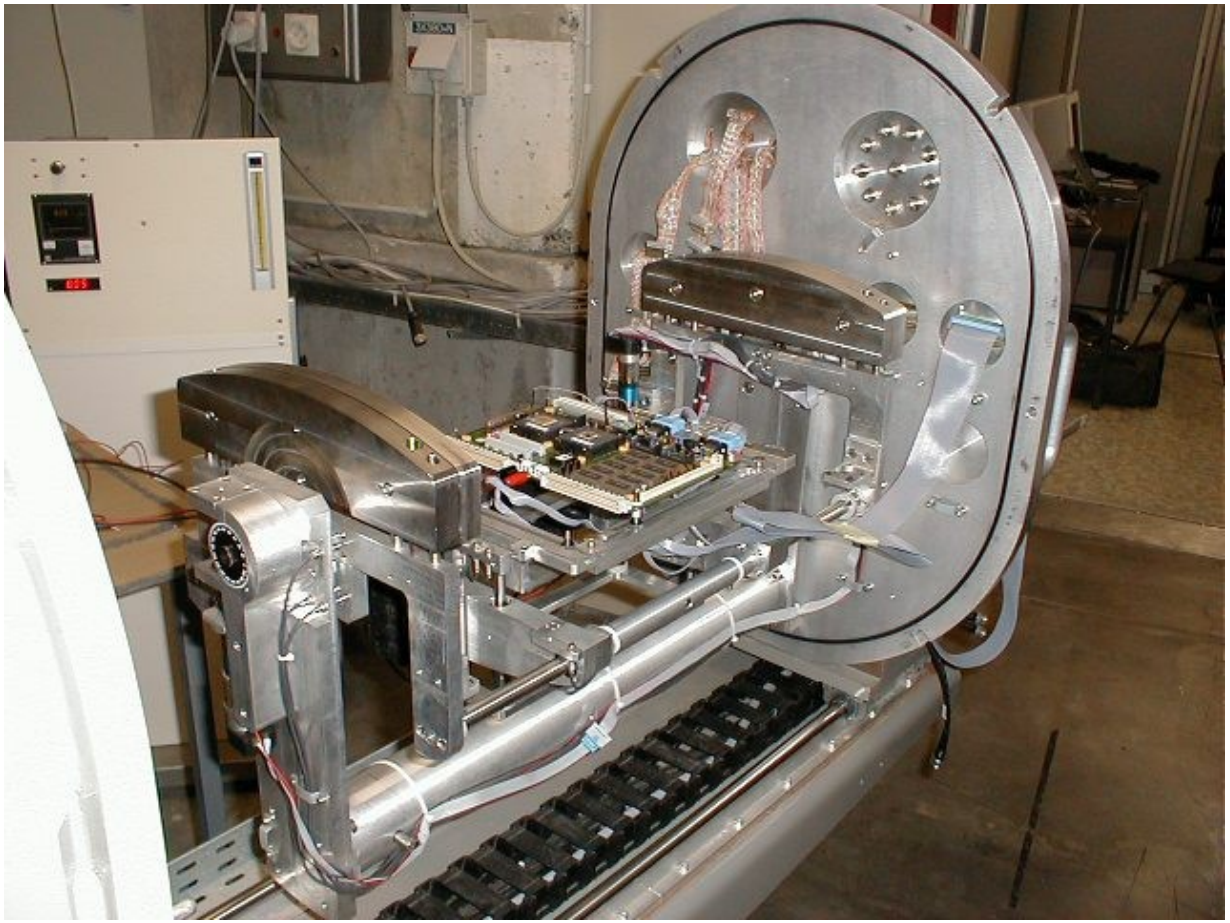
- Second round-table on processors held in 1996
  - Software compatibility with ERC32 main requirement
  - 100 – 500 MIPS desirable
  - Mostly seen as payload or instrument controller
  - No mentioning of SOC yet ...
- Outcome
  - Develop a single-chip ERC32
  - Define and design LEON1FT SPARC core
  - Development schedule ~ 2 years

LEON1FT project

- Develop a new SPARC V8 processor
  - Synthesizable and portable
  - 100 MIPS, 20 MFLOPS, 1 W
  - Fault-tolerant rather than hardened

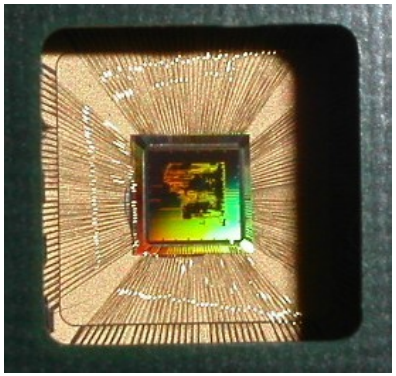
- Outcome
  - Developed under Douglas Marsh fellowship in 1997/8
  - Manufactured on Atmel 0.35 um RT process in 2000
  - FT scheme validated through extensive error-injection
  - Released in open-source in 1999 (non-FT)

LEON1FT SEU testing

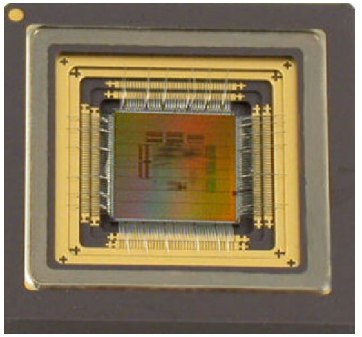


LEON2FT project (2002)

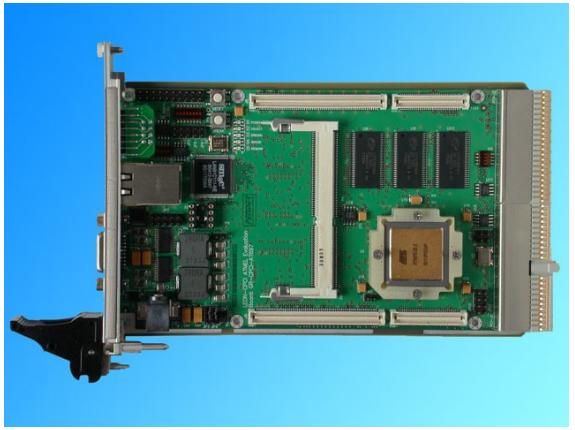
- Enhance the LEON1FT design
  - 4-way caches, MUL/DIV, DSU, AMBA, SDRAM
  - Designed by Gaisler Research, licensed to ESA
  - Open-sourced in LGPL (non-FT)
- Exclusive rights to Atmel for FT model



LEON2FT-UMC



AT697F



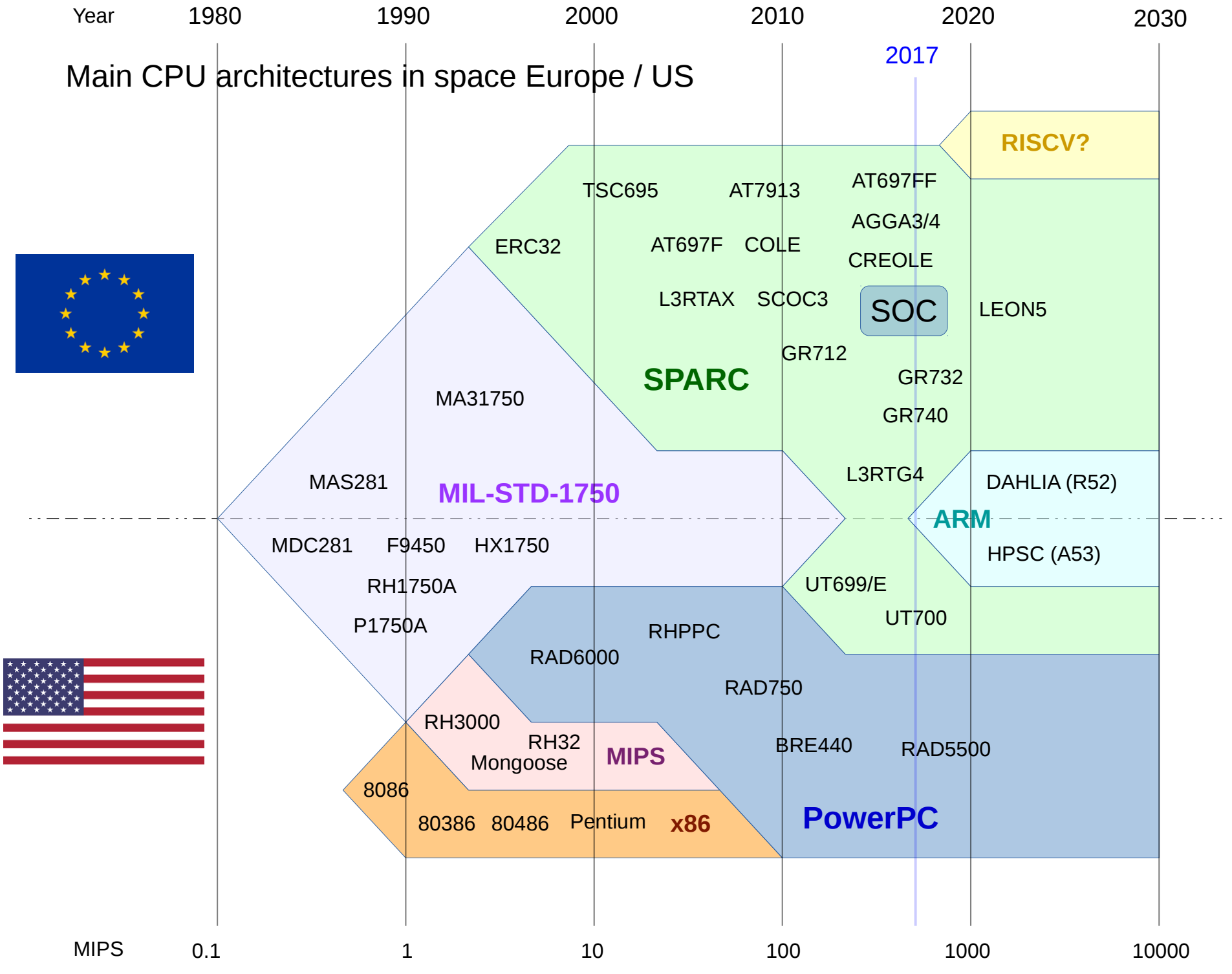
GR-PCI-AT697

GRLIB project (2004)

- Create a SOC platform rather than just a processor
  - LEON3 with deeper pipeline, GRFPU, MMU, SMP
  - Modular design with on-chip plug&play
  - Many additional IP cores
  - Fully owned by Gaisler
- Used in both commercial and space applications
  - LEON3FT-RTAX, GR712RC, UT699, SCOC3 …
  - LEON4 released in 2010

25 years of SPARC

- Open architecture → unrestricted use, no fees
- SPARC → Low complexity, stable specification
- Open-source →
  - Simple prototyping and evaluation
  - Synergy effects from +100 thesis and research projects based on LEON
- Implementation
  - Robust design style, portable, modular, low complexity, FT
  - Synergy effects from commercial non-space usage
  - Low cost
- Problem areas
  - Declining software support
  - Unnecessary fragmentation
  - Performance lack due to low investments
- **Did we make the right choice?**


Year
1980
1990
2000
2010
2020
2030
2017
Main CPU architectures in space Europe / US
RISCV?
TSC695
AT7913
AT697FF
AGGA3/4
ERC32
AT697F
COLE
CREOLE
L3RTAX
SCOC3
SOC
LEON5
GR712
SPARC
GR732
MA31750
GR740
L3RTG4
DAHLIA (R52)
MAS281
MIL-STD-1750
ARM
MDC281
F9450
HX1750
HPSC (A53)
RH1750A
UT699/E
P1750A
UT700
RHPPC
RAD6000
RAD750
RH3000
RH32
Mongoose
MIPS
BRE440
RAD5500
8086
80386
80486
Pentium
x86
PowerPC
MIPS
0.1
1
10
100
1000
10000