Micronodes

ADCSS 2017 18th October 2017 @ ESTEC

Harness Reduction Session

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ThalesAlenia Space
a Thales / Leonardo company

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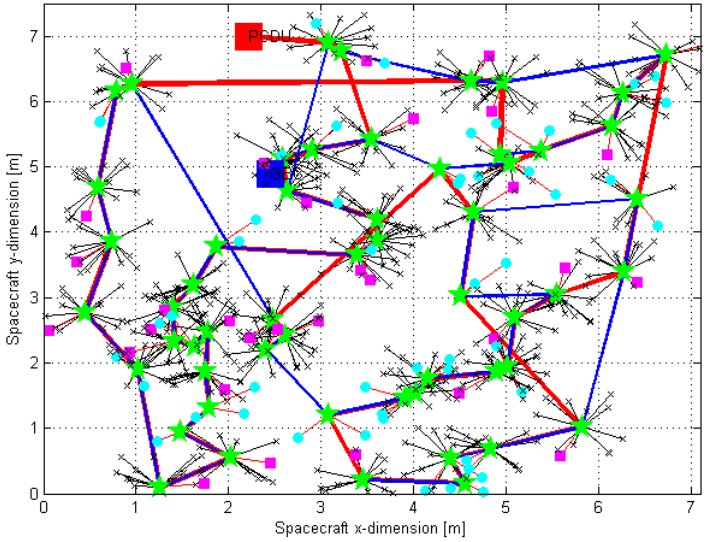
- System Modelling

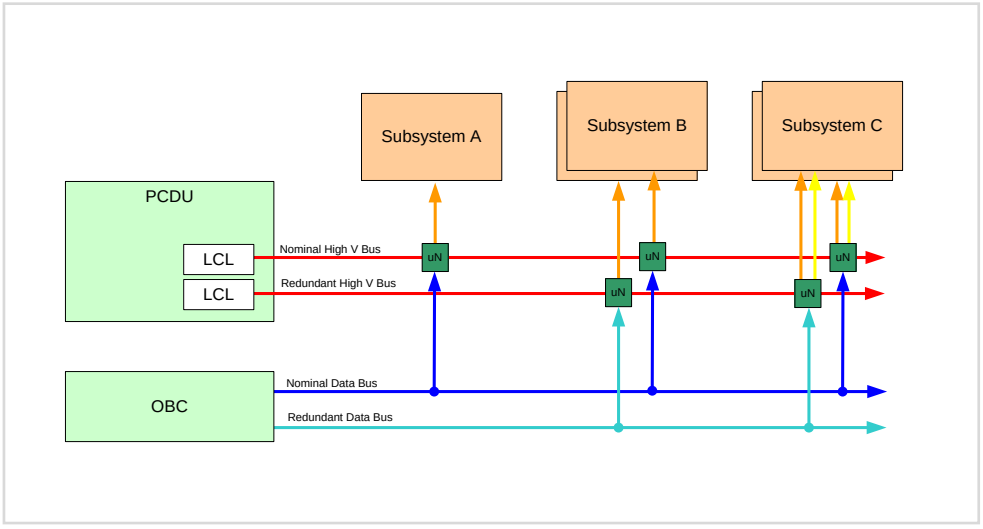
Project Overview

- Follow-on from ESA-funded study
  - "Smart Microsystems for Space Applications"
- Led by Thales Alenia Space in the UK
  - Thales Alenia Space (France)
  - AAC Microtec
  - Cobham Gaisler
- Requirements consolidation
  - Applicability for future missions
  - Retrospective assessment for past missions
- Design & manufacture
  - Dependency on GR716 programme
- Software development
- SAVOIR-aligned
- Targeted at ATHENA mission



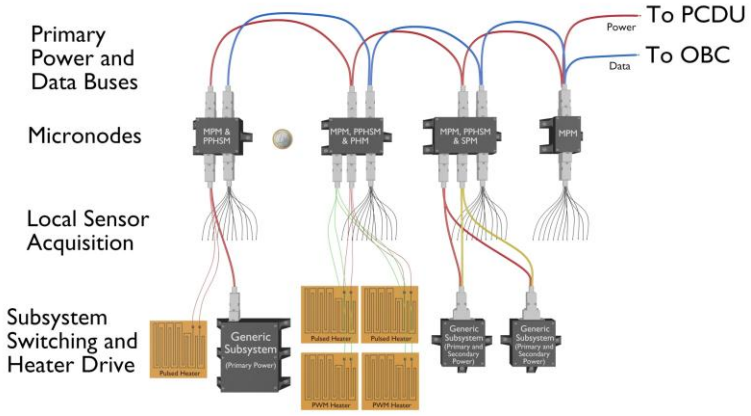
Micronodes Concept

- Low power
- Standard C&C bus
- Microcontroller CPU
- Analog/digital IO
- Power switching
- Heater PWM



Micronode Advantages

- Reduced harness mass
- Modular/standardised architecture
- New functional modes
  - Semi-autonomous
  - Partial operation
- Simplified AIT



Mission Applicability

- Athena
  - Mission driving the study, high complexity, need decentralized architecture, mass reduction necessary
- ExoMars TGO
  - Deep Space, thermal control based on important number of sensor/actuator, flight proven
- NEOSAT
  - Telecommunications, mass production
- TAS Generic RTU
  - Maturity level high, Earth Observation missions
- SAVOIR RTU and OBC
  - Gather functions expected from such components
  - OBC for its computing capability, RTU for its interfacing capability

Relation to SAVOIR

"The availability of microcontroller (as standalone ASIC or as IP core in a FPGA) could change the avionics architecture of a S/C allowing the decentralization of tasks very often done by the OBC, using an intelligent RTU."

SAVOIR Functional Reference Architecture

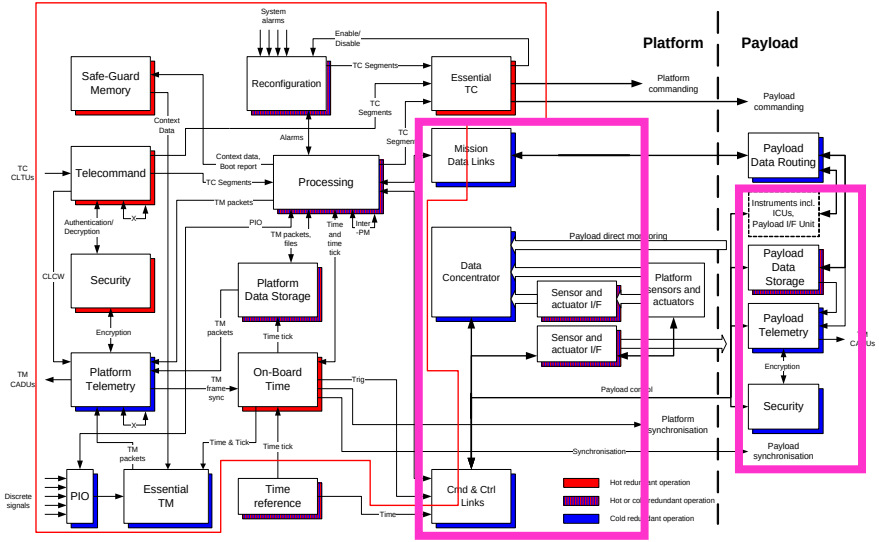


Diagram: ESA

Candidate Processors

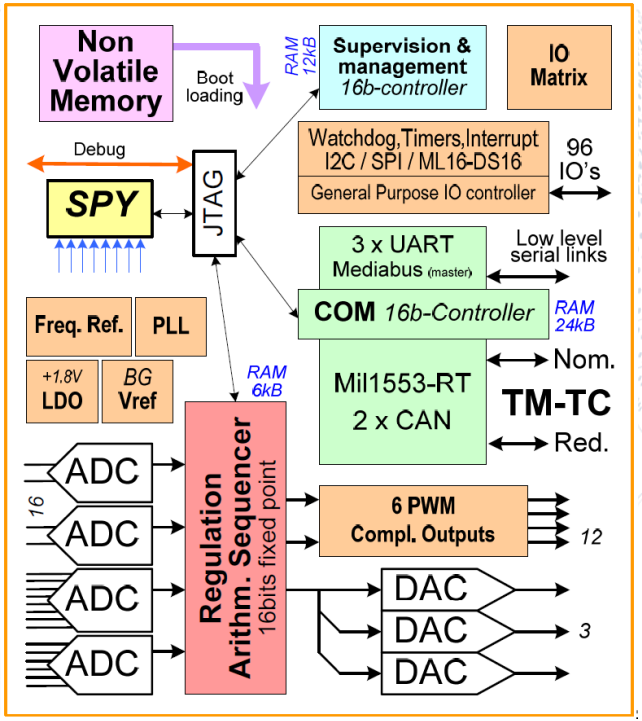
- GR716
  - LEON3 @ 50MHz
  - Baselined for Micronodes
- DPC
  - OpenMSP430 @ 40MHz
- SSDP
  - LEON3 @ 100MHz
  - Xentium DSP
- ARM
  - ATMEL
  - Cobham Gaisler

Digital Programmable Controller

- 40 MHz Maximum Clock Frequency
- Rad-hard, ESCC9000 qualified
- 3 x OpenMSP430 cores

- Onboard ADC + DAC + PWM + GPIO
- Redundant CANbus + Mil-1553
- Onboard 1.8V regulator
- Low power consumption
- Non-invasive debug facility

- Used in many TAS equipments (inc. SB-Neosat SDIU)
- Used by space community
  - DLR (robotics), Onera (Gyros), more to come
- Available for ESA projects without restriction
- No US content
- 200+ FM produced

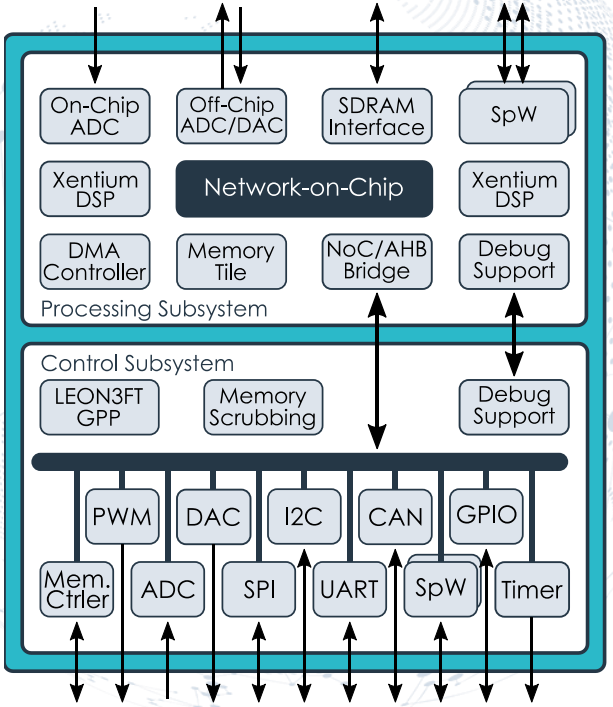


Scalable Sensor Data Processor

- 100 MHz Maximum Clock Frequency
- 300 krad
- High SEU hardness

- 1x LEON3FT with High-Performance Floating Point Unit
- Up to 64 MB SRAM & PROM

- 2x Xentium Fixed-Point DSPs
- Network-on-Chip Interconnect with DMA Controller
- On-Chip ADC, up to 50 Msps
- Interface for Off-chip ADC/DAC / Chip-to-Chip
- 2x SpaceWire with RMAP Target, up to 200 Mbps



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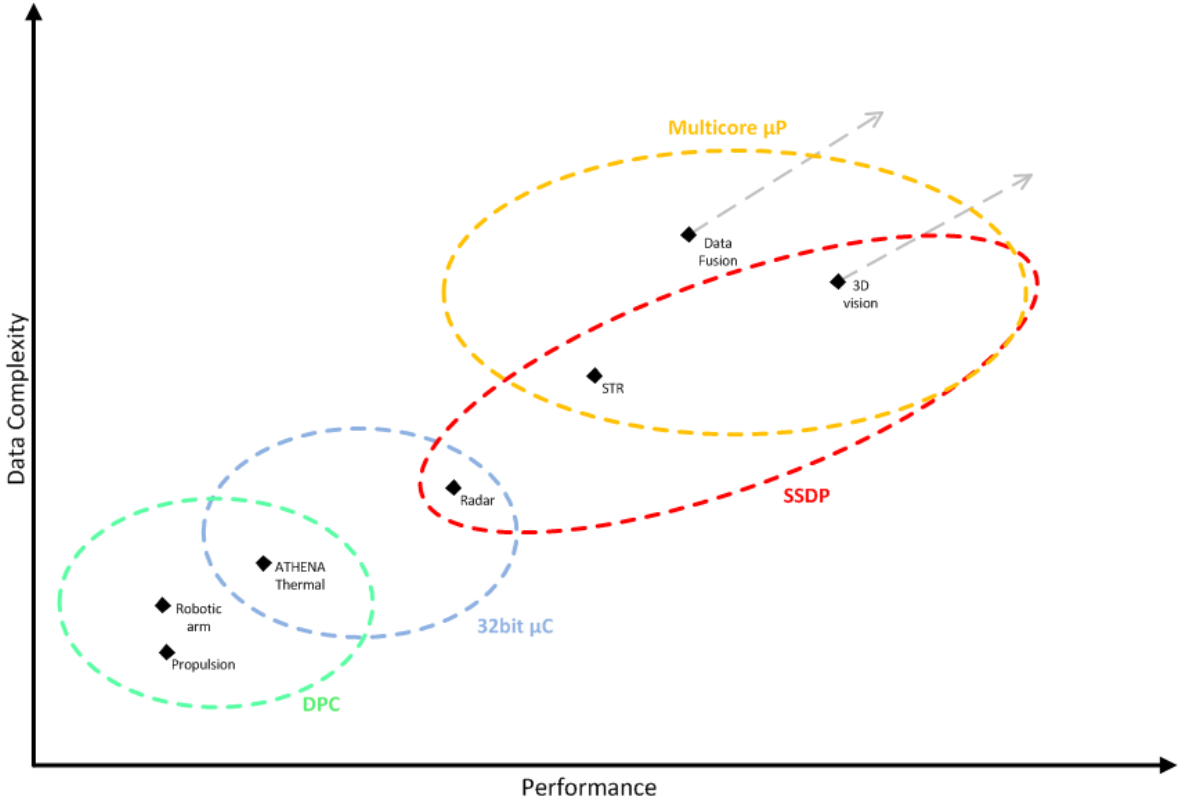
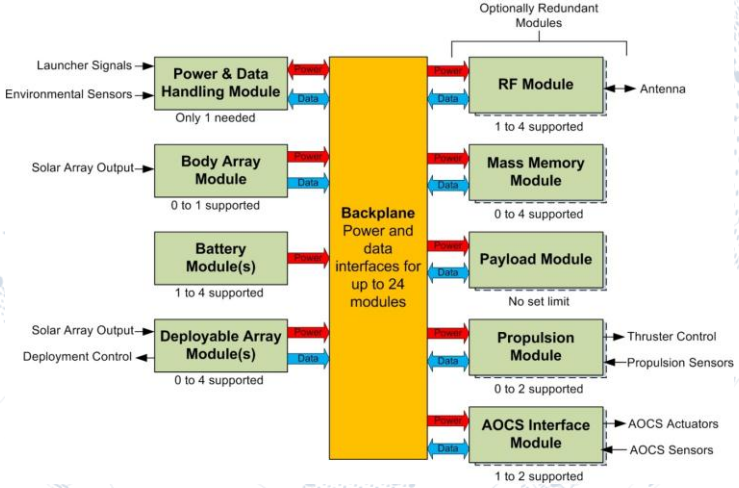
Ref. =
Ref. Modèle = 83230347-DOC-TAS-EN-004

Performance Spectrum



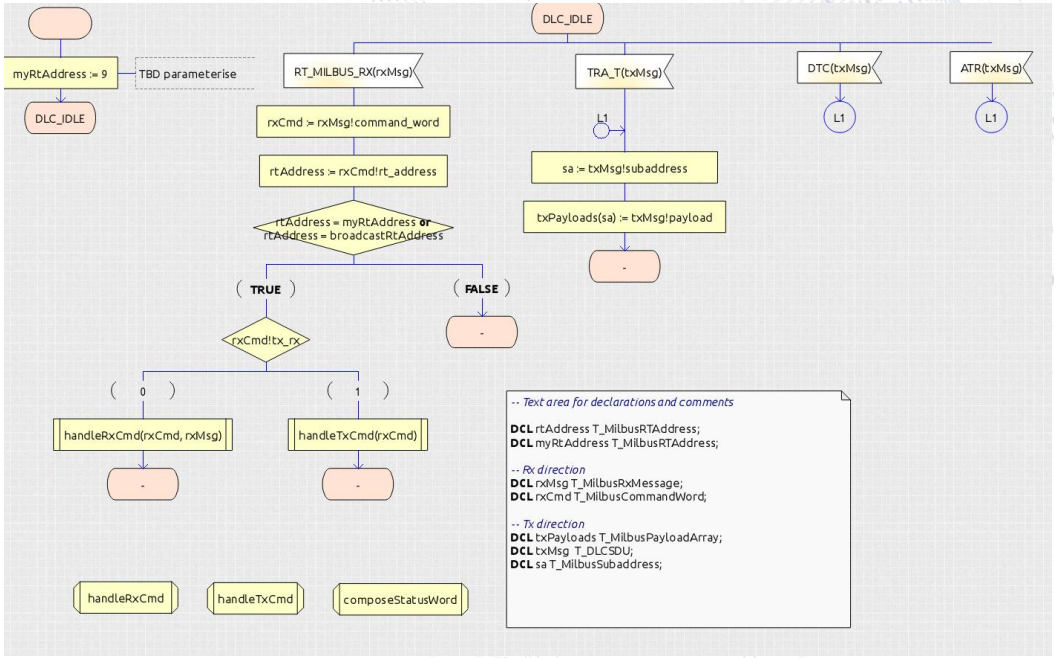
CANbus Protocol

- CANbus baselined for Micronodes
- Determinism may be required
  - Add scheduling
  - e.g. TDMA frames
- TAS in the UK developing an open CANbus backplane
  - UKSA funded activity
- Protocol based on ECSS-E-ST-50-15C
  - CANopen compliant
  - Deterministic
  - PDO
  - SDO
  - Suitable for Micronodes



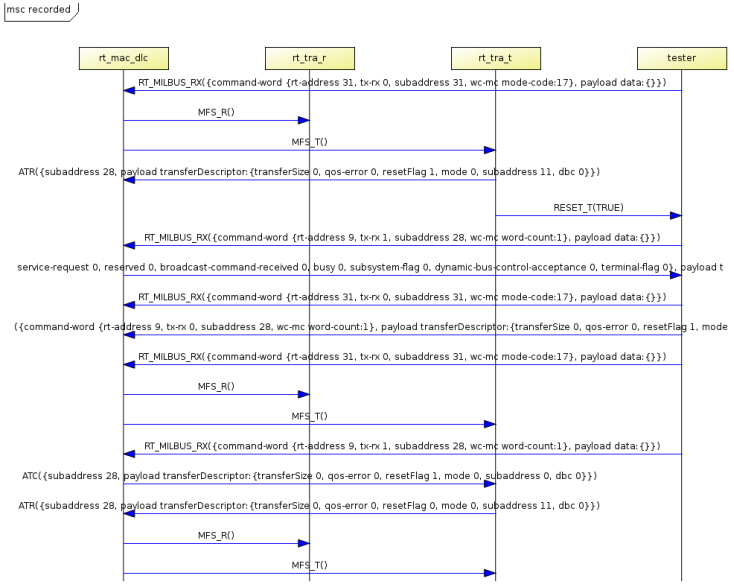
System Modelling

- Protocol validation
  - Correctness
  - Robustness
  - Schedulability
- SDL
  - Graphical language for protocol description
  - Used in telecoms since 1980s
  - Formally complete
  - Human readable
  - Executable
  - Provable



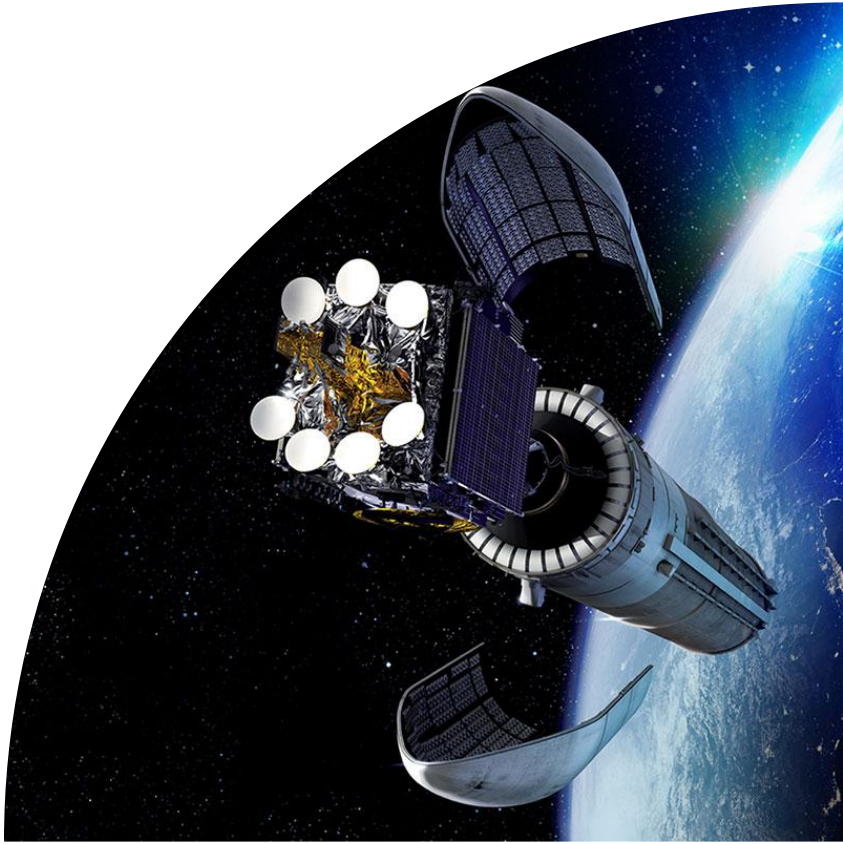
System Modelling (TASTE)

- SDL integrated in ESA TASTE toolset
  - OpenGEODE SDL editor
  - Data modelling via ASN.1
    - ICD generation
    - Autogen encoding/decoding
  - Output as C/Ada code
- TASTE VM executes SDL
  - Message sequence charts (MSC)
  - Record / replay / editing of message exchanges
  - Scripting of test cases (Python)



Thank you for listening ☺

Questions…



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