



Space Processors TAS View

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MISSIONS

GENERAL OVERVIEW



Constellation :
Low rec cost

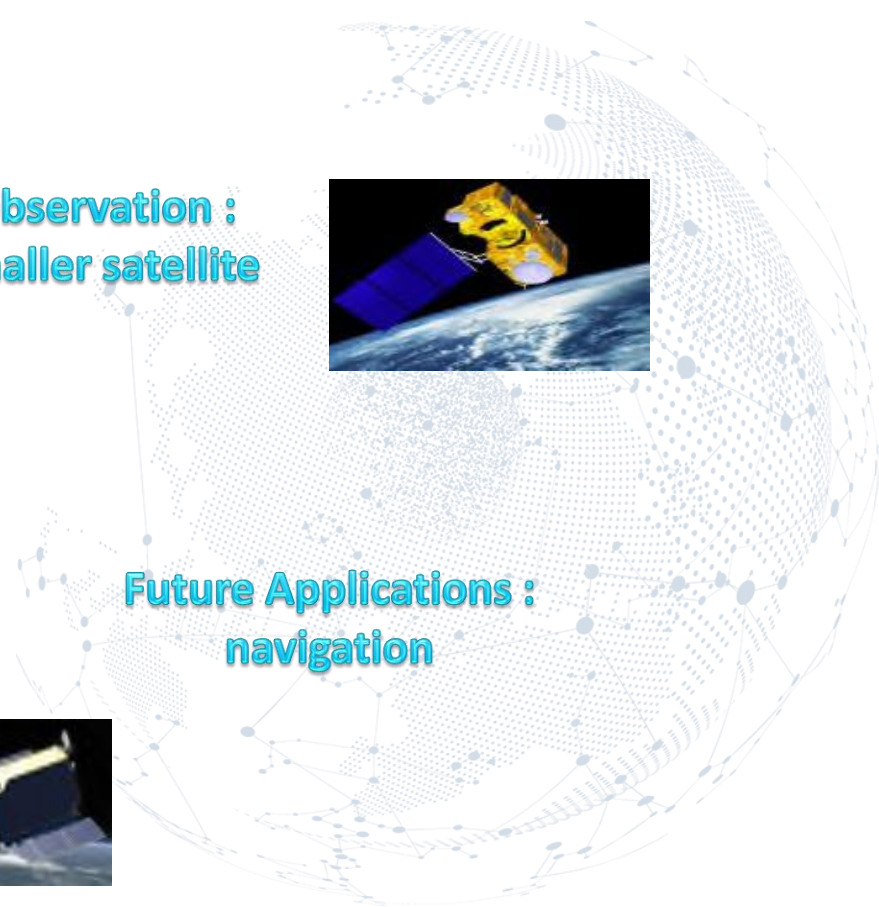
Science – exploration :
Rendez vous – capture -
landing



Observation :
smaller satellite



Future Applications :
navigation



AVIONICS

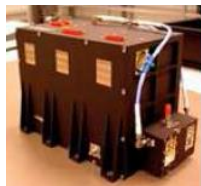
GENERAL OVERVIEW

Integrated Avionics

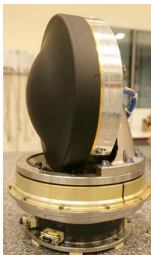
STR data processing



GNSS data processing



CMG control



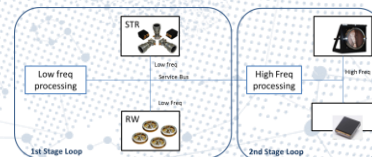
Payload management

Navigation sensors

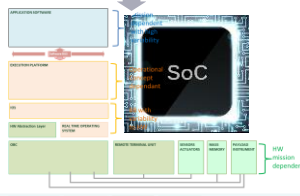
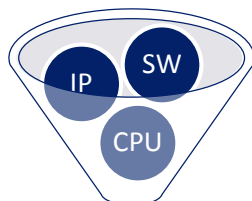


Additional functions

Multi stage control



Autonomous applications

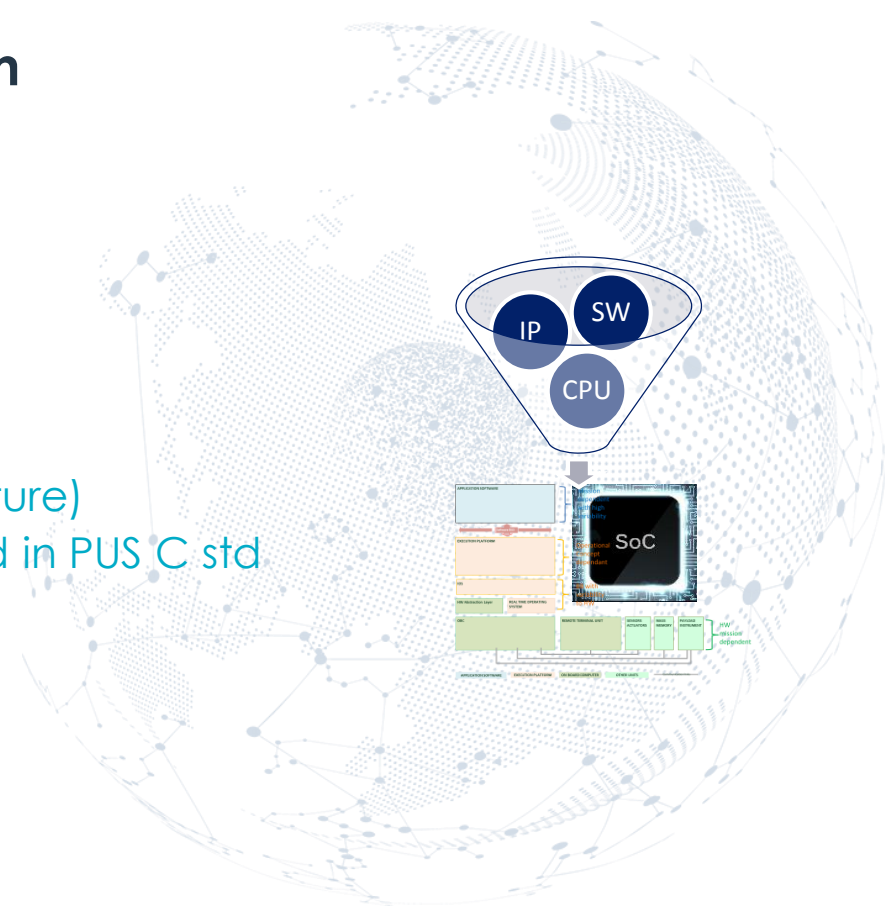


Operation Concept Evolution

GENERAL OVERVIEW

OBC to integrate

- File based operations
- CFDP protocol
- More OBCPs (FDIR/autonomy feature)
- PUSLIB to be converted/upgraded in PUS C std



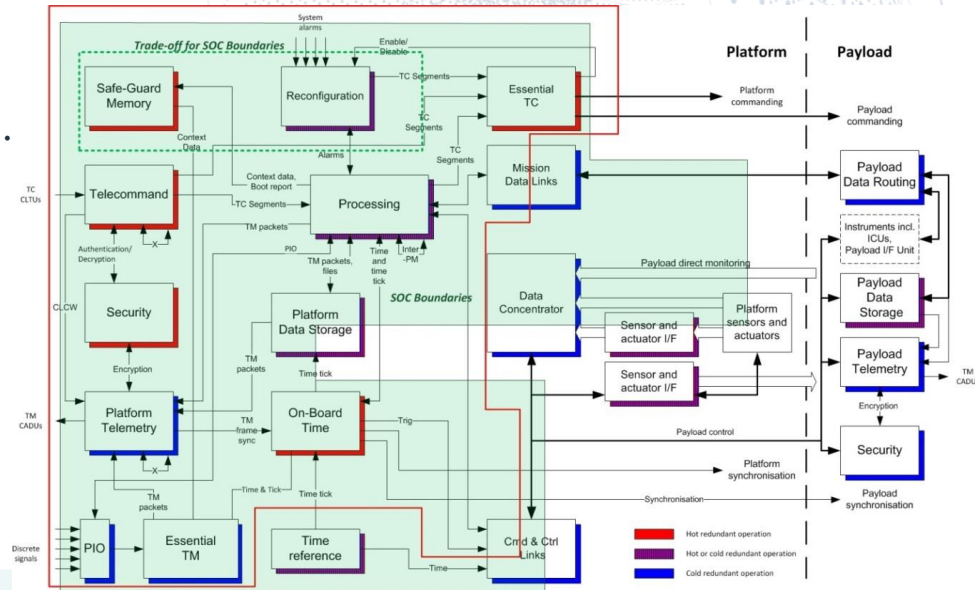
Operation Concept Evolution

GENERAL OVERVIEW

Evolution of FDIR strategy induced by :

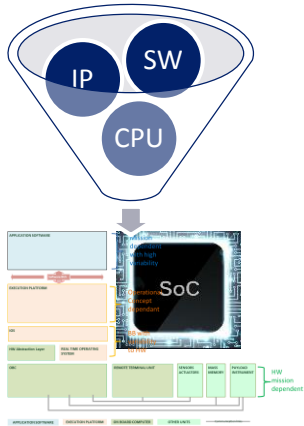
- Processing in one SOC
 - Most PF applications centralised (ASW, STR, GNSS, ...)
- Reconfiguration Module location
- SGM location
- Xstrap scheme simplified

➔ Could lead to “half platform” recovery.



Avionics Evolution

Performance Synthesis



Data acquisition and control:

From 1, 8/10, 32, up to 1000 Hz (ALS)

Network : minimum SpW – Ethernet – SpFi?

Communication bus : 1553 – CAN

Processing :

From 200/300 DMIPS, up to 2000 DMIPS (Vision, ALS)

PM Memory > 64 Mbytes – Mass Memory > 100 Gbits

Operation concept :

File – CFPD – DTN? – OBCP – PUS – Autonomous applications



AVIONICS development needs

GENERAL OVERVIEW

New space processor in Avionics require :

- 🌐 Debugging capabilities
 - 🌐 DSU – Profiling
- 🌐 Development models
 - 🌐 Development board to support SW migration
 - 🌐 Eventually Functional Model
- 🌐 Simulated core
 - 🌐 To be inserted in numerical Avionics core simulator
- 🌐 HDSW/Boot Sw development
- 🌐 Hypervisor/OS
 - 🌐 Supporting TSP
 - 🌐 Supporting Multicore
- 🌐 SVDE and SW migration



Significant Non recurring Activities associated to new space processor



AVIONICS development needs

Common BB

What could/should be shared by Space stakeholders with the objective of harmonisation

🌐 Development models

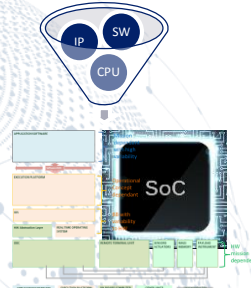
- 🌐 Development board to support SW migration preparation (bread boarding activities)

🌐 Simulated core

- 🌐 To be inserted in numerical Avionics core simulator

🌐 Hypervisor/OS

- 🌐 Qualified on the targeted Space processors



Space Agencies roles to support common BB



**THANK YOU FOR
YOUR ATTENTION**

ThalesAlenia
a Thales / Leonardo company **Space**

