Space Processors: Programs Views (Earth Observation)

Avionics, Data, Control and Software Systems (ADCSS)

Presented by J. Rosello (EOP-ΦMT , EO Future Missions Div.)

(19-Oct-2017)

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Overview of EO missions & which microprocessors in use

Challenges for the future

Definition of processor

On-going developments and emerging topics in the field of space processors.

The term processor comprises:

- Various architectures and performance classes:
  - single and multi-core,
  - symmetric and asymmetric processors,
  - microcontrollers and DSP's.
- Hardware + Software (development tools, compilers, operating systems, hypervisors etc.)
- Developments dedicated to space or (screened) COTS
- Developments of different maturity (from low TRL R&D up to In Orbit Demo.)

➔ Large investments and consortia to reach adequate and complete (HW and SW) "qualified" solutions.

Emerging applications: higher performances and/or integration of new functionalities.

Location of Microprocessors

Platforms:

- **OBC** or **SMU**: (On-Board Computers or Service Management Unit)
- **MMFU** (Mass Memory and Formatting Unit)
- **GNSS Receivers**
- **Star Trackers**
- **OCP** (Optical Communication Payload)
- Others (mini-IMU) - not covered in this presentation (lack of information)

Payload:

- ICU or CES or DPU : (Instrument Control Unit or Central Electronic System or Digital Processing Unit)

  ➔ not always with a microprocessor (SW required)

  ➔ different for each mission

ESA Earth Observation Missions

Colour Code:
Launched
To be launched

Living Planet

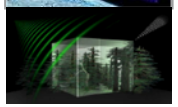
Earth Explorer
Research driven

Core Missions


GOCE
2009-2013


ADM-Aeolus
Jun 2018


EarthCARE
2019

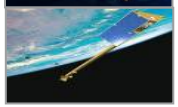

Biomass
(EE7) 2021

Call EE10 – (4Q-2017)
Select. For Ph.A 3Q-2018

Opportunity


CryoSat-2
8 April 10


SMOS
2 Nov 09


Swarm
22 Nov 13

Fast Track


FLEX (EE8)
2023

Call EE9 –
Select. for Ph.A
(Nov-2017)

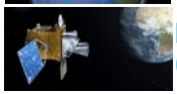
Earth Watch
Operational Service driven

Meteorology


Meteosat


MSG - GEO
(1 s/c x 4)


MetOp
1 s/c x 3)


MTG - GEE
(2 s/c x 3)


MetOp SG
(2 s/c x 3)

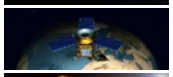
Copernicus


Sentinel 1 a/b/c/d


Sentinel 2 a/b/c/d


Sentinel 3 a/b/c/d


Sentinel 4 (on MTG)


Sentinel 5 precursor


Sentinel 5 (on MetOp SG)


Sentinel 6 (Jason)

Copernicus Space Component → Ph.A
Potential Expansion Sentinels (2018)

OBCs - SMUs

31750:

- SMOS

ERC-32:

- Goce, EarthCare, ADM, Cryosat-2, Swarm, Sent-1a/b, Sent-2, Sent-3, Sent-6
- In Sentinel-2: CPU peak = 65% (normally much lower); 8 Gbit SDRAM

Leon-2FT (AT697F, COLE):

- MTG-I, MTG-S,

Leon-3 (GR712RC, SCOC3, EPICA-Next):

- MetOp-SG, SeoSat, Sent-1c/d, Sent-5p
- MetOp-SG: 75% worst case CPU usage with 32 MHz (normally much lower)

If more processing power available:

- Increase functionality: e.g. FDIR
- Serve as processor for other functions : star trackers, GNSS, … (multi-core can be interesting)

MMFU (Mass Memory and Formatting Unit)

ERC-32:

- Sent-1, Sent-2, Sent-3, Sent-6
- In Sentinel-2: CPU peak = 6% ➔ with high CPU power, compression could be envisaged

Leon-2FT (AT697F, COLE):

- Biomass, EarthCare

LEON-3 (GR712RC, SCOC3, EPICA-Next):

- MetOp-SG, Sent-5p

FPGAs + OBC

- Goce, Swarm, ADM,

GNSS Receivers for Navigation and POD

Various microprocessors

- ADM, Seosat, Sent-5p (Mosaic SW Rx with DSP-20120)

AGGA-2 + LEON or DSP-21020:

- TAS-I (GOCE 21020), RUAG-A: (EarthCare, Swarm, Sentinels 1a/b, S2a/b, S3a/b with Leon2-FT)
- non-ESA: Radarsat-2, Cosmo-Skymed Note: GNSS-Radio Occ. Instrum. with AGGA-2: MetOp-a/b/c, Oceansat2, Megatropiques, SAC-C/D

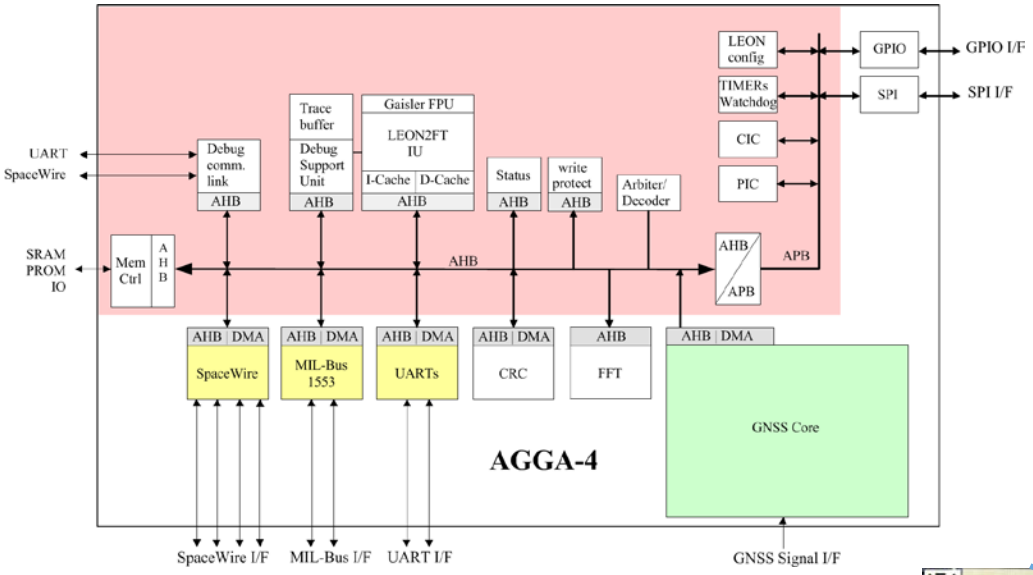
AGGA-4 (with Leon-2FT IP core on-chip @ 87 MHz) Note: PODRIX Rx board includes both AGGA-4 and AGGA-2.

- MetOp-SG, S1c/d, S2c/d, S3c/d, S6, Biomass ➔ CPU usage ~ 70%
- Non EO: Proba-3, Neosat
- non-ESA missions: CSO, SARah, Korean Comp.Adv Sat.500, prototyping for Vega-C

AGGA-5

- Feasibility study "under negotiation".
- Not decided which microprocessor, but very likely more powerful than for AGGA-4 ➔ **more flexibility, cope with multi-GNSS constellation**

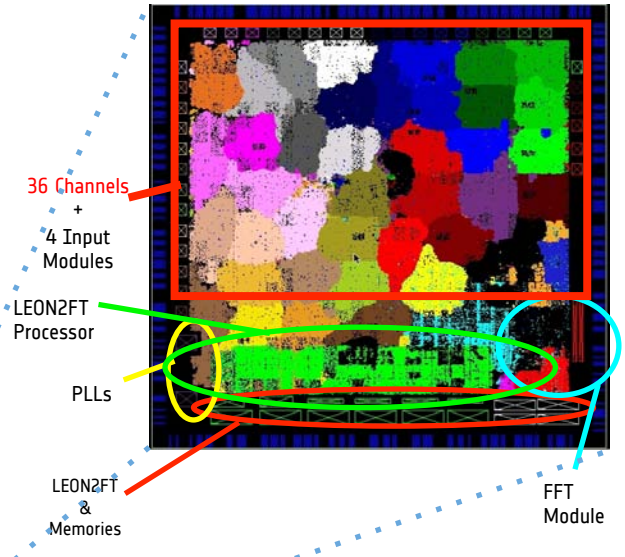
AGGA-4 (Advanced GPS-Galileo ASIC)

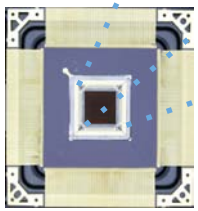


Designed by Airbus GmbH

Available as ASSP from Microchip ATMEL since 2014

Floorplan



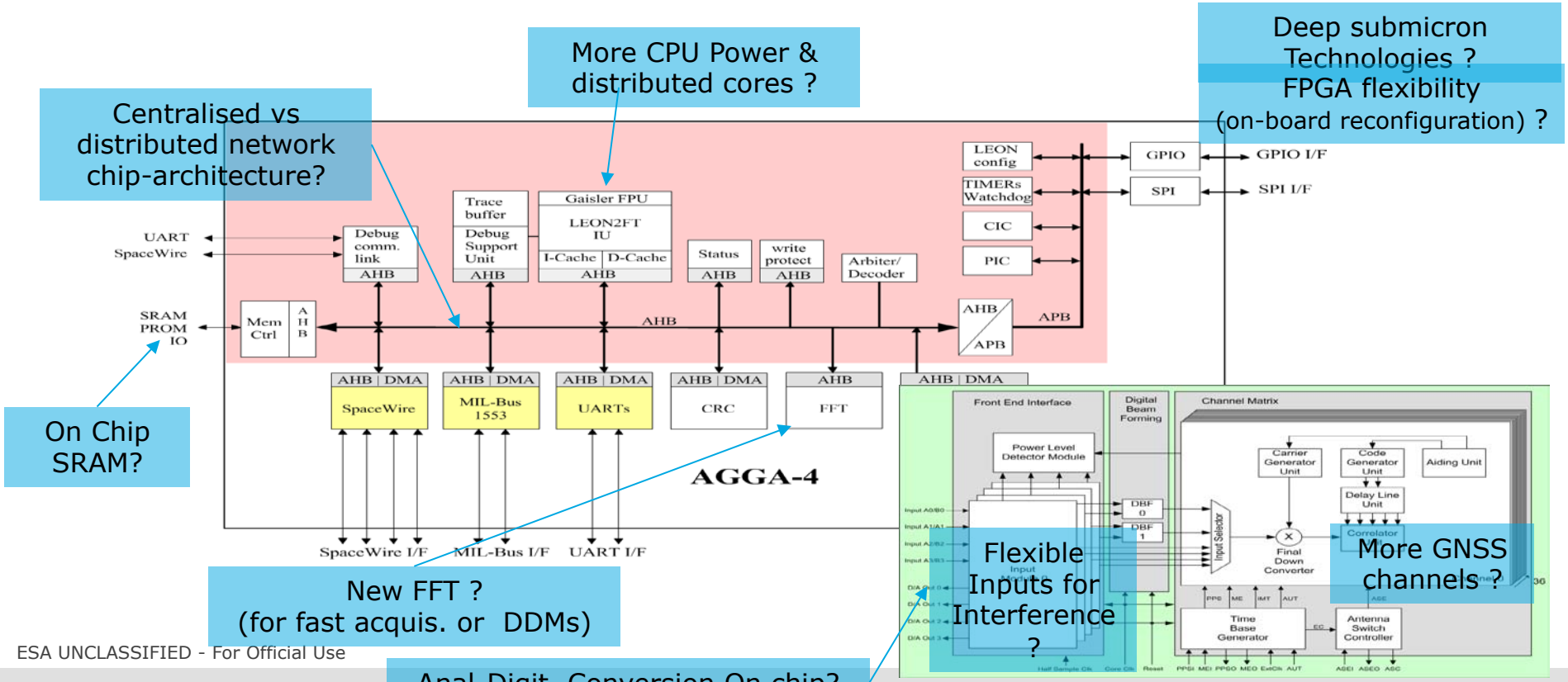


(Die size 13x13 mm, incl. Pads)

GNSS core :			2.7 Mgates
LEON2FT + GSFPU:	428 + 122 k gates	=	0.55 Mgates
Clocks + I/Fs+ backend :			1.35 Mgates
		Design :	4.6 Mgates
Pads+others :			1.4 Mgates
Total :	352 pins CQFP	and	6 Mgates

AGGA-5 feasibility study (EOP funded): Trade-offs

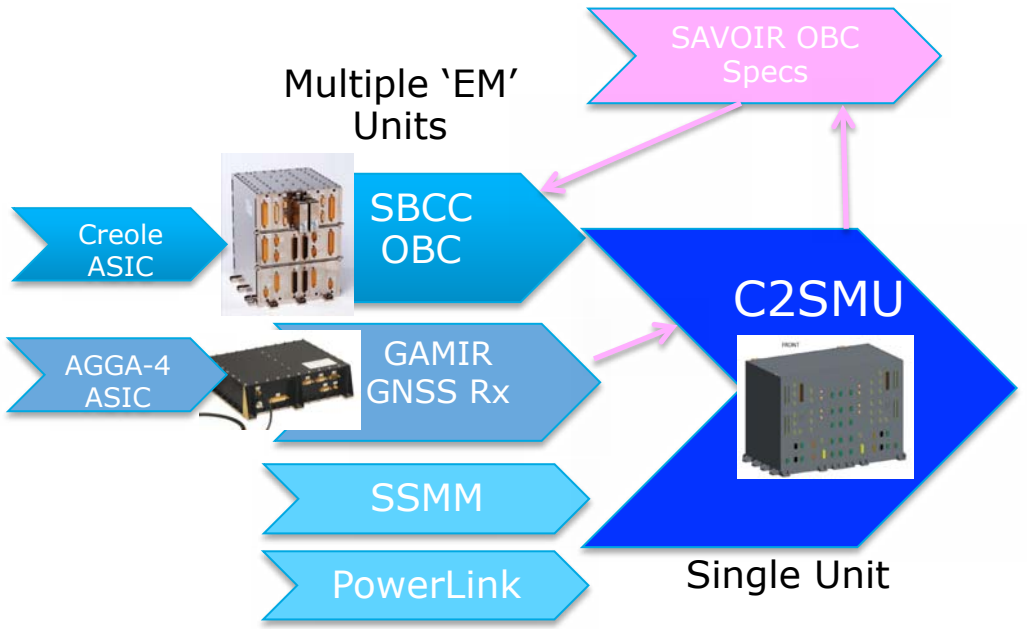
Status: Under Negotiation



Study Definition of C2SMU

Complex & Complete SMU and Critical BreadBoarding :

- integrating OBC + GNSS + SSMM + specs for S-PowerlLink



C2SMU Feasibility Study

- Requir. + Architectural Design
- Integration + Analysis/Testing key modules
- Development Plan

Development in follow-up study

Star Trackers

ERC32 (with Leonardo, former Selex)

- Sent-1, MTG (no OS, interrupt driven)

LEON2FT (with Sodern)

- Sent-3, Sent-5p, Seosat,

LEON2-FT (with Jena)

- EarthCare, Sent-2, Sent-6

COTS microprocessor

- ADM, Swarm, Cryosat-2. (TERMA or DTU)
- SMOS (with SED16 from Sodern)

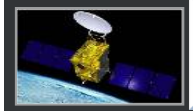
Highest CPU usage during acquisition (not during tracking). Reasonable usage (even during solar flare)

If more CPU becomes available ➔ robustness, higher performance

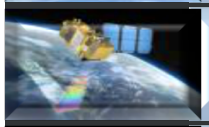
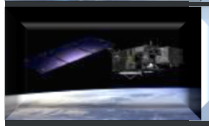
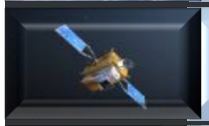
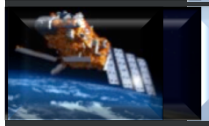
OCP (Optical Communication Payload)

- Only in Sent.1 and Sent.2: PowerPC 750

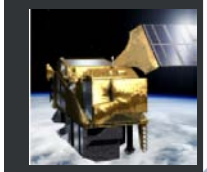
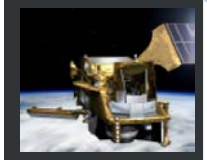
Earth Explorers : Instruments

	Mission	Launch	Main Instrument(s)	ICU – CES - DPU
	GOCE	2009	Graviometer Adv. Stellar Compass	DSP-2010 Intel 80486
	ADM-Aeolus	2018	Doppler Wind Lidar	No microprocessor (only FPGAs)
	EarthCare	2019	Atmospheric Lidar Cloud profiling radar Multi-spectral imager Broad-band radiometer	LEON2-FT Japanese μproc. LEON2-FT LEON2-FT
	Biomass	2021	P-Band SAR	Leon2-FT

Copernicus : actual sentinels and OBCs

	Sentinel	Launch	Instrument	ICU – CES - DPU
	**Sentinel-1 A** **Sentinel-1 B** (also C + D)	3 April 14 25 April 16 (Plan)	C-Band SAR	ERC-32
	**Sentinel-2 A** **Sentinel-2 B** (also C + D)	22 June 15 7 March 17 (Plan)	Multispectral	None (FPGAs)
	**Sentinel-3 A** **Sentinel-3 B** (also C + D)	16 Feb 16 Plan 2018 (Plan)	C/Ku Radar Altimeter 23.8/36.5 GHz radiometer OLCI spectrometer VIS-SWIR-TIR radiometer	DSP21020(A/B)–LEON2(C/D) None (FPGAs) LEON2-FT ERC-32
	**Sentinel-4 A** **Sentinel-4 B**	plan 2020 plan 2030	UVN-VIS-NIR Spectromet.	LEON-3FT (in MTG-S)
	**Sentinel-5 A** **Sentinel-5 B**	plan 2022 plan 2028	UVNS Spectrometer Infrared Sounder Multi-view/pol Imager	LEON2-FT (in MetOp-SG)
	**Sentinel-5 P**	Oct 2017	TROPOMI (passive imaging spectrometer)	LEON2-FT
	**Sentinel-6 A** **Sentinel-6 B**	plan 2021 plan 2025	C/Ku Radar Altimeter	LEON2-FT

Meteorological : Instruments

	Mission	Launch	Instrument	ICU – CES - DPU
	**MTG-I**	2021 2025 2029 2033	Flex.Comb.Imager (FCI) Lightning Imager (LI) Radiat.Monit.Unit (RMU)	ERC-32 ICU, Leon-2 SCA Power PC7448 LEON-3 (GR712)
	**MTG-S**	2023 2031	IR Sounder (IRS) UV-VIS-NIR Sounder (UVN) (=Sentinel-4) Radiat.Monit.Unit (RMU)	ERC-32 ICU, Leon-2 SCA LEON-FT2 (COLE) LEON-3FT (GR712)
	**MetOp-SG (A)**	plan 2021 plan 2028 plan 2035	METimage (VIS-IR) IASI-NG MW Sounding Radio Occ. 3MI Sent.5	Leon-2FT (MDPA) (not ESA) Leon2-FT (MDPA) Leon2-FT (AGGA-4) Leon2-FT (MDPA) Leon2-FT (MDPA)
	**MetOp-SG (B)**	plan 2022 plan 2029 plan 2036	Scatterometter MS Imager (radiom.) Radio Occ. Ice Cloud Imager (radiom) Argos-4	Leon-2FT (MDPA) No Leon2-FT (AGGA-4) ?? (NOT ESA)

Increasing functionality SoC

LEON-based Core computer architectures & System on a Chip (SoC), incl. microprocessor+I/Fs:

- ADS: MDPA with LEON-2FT & SCOC3 with LEON-3
- RUAG: CREOLE and COLE with LEON-2FT
- TAS: EPICA-Next with LEON3-FT

and also coming up

- CG: NGMP with multi-core LEON-4 and SpW router
- ARM IP-cores being embedded in new FPGA/ASIC devices (in multiple versions, Mo+, M7, R5, R9, …)

➔Big legacy so far of single-core LEON family for platform applications

➔LEON also dominates in payloads (ICU), but other options found

Multi-core: Will increase processing power, and possibly cover well future growth.

- Common in on-ground apps., but yet in space
- **EOP needs one full (HW-SW) set solution,** possibly starting with payload applications (and combined with FPGA/ASICs).
  (Compilers, OS, etc.)

LEON vs ARM (both in the ESA Harmonisation process): Two key questions / challenges :

- Does one of them get substantial better performance / reliability ?
- Does anybody have the budget to fully develop both ?

➔ Let's wait for the following presentations !!

Recap trends if more powerful processors

Platforms:

- **OBC** or **SMU**: larger functionality & robustness (FDIR, …) , possibly more integration of functions (SoC)
- **MMFU** : very often same as OBC. CPU Room for more (e.g. compression)
- **GNSS Receivers** : getting integrated in OBC Units and SAVOIR OBC specs
- **Star Trackers :** if more CPU, higher robustness / performance
- **OCP** : (Optical Communication Payload) - currently using PowerPC in S1/S2

Payload:

- ICU or CES or DPU : (Instrument Control Unit or Central Electronic System or Digital Processing Unit)
  - most ESA missions have a microprocessor (SW required). ICUs might be shared between instruments
  - More processing power, combined with OB reconfigurable FPGAs can be very attractive
- a bit more of flexibility (in terms of quality) than for Platform Critical functions.

Conclusion

Overview of EO missions & which microprocessors in use (platform & payload)

- Clearly dominated by LEON family and SoC incorporating more functionality (I/Fs)
- Availability of IP cores is very important for SoC

Trends

- More processing power will be available (with multi-core), but also complexity (OS, Compiler) increases
  - for OBC : could allow processing functions today done by other microprocessors
  - for MMFU : could allow compression or other functions
  - for payloads : very interesting, specially if combined with reconfigurable FPGAs/ASICs

- LEON vs ARM ? (technical and also resources issues)