Comprehensive SEE Qualification

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Outline

- Project Outline
- Select Parts
  - SRAMs
  - FPGA – Xilinx Ultrascale+ ZU3CG
  - SoC – Atmel SAMV71
- Initial Results
- Looking ahead

Project Outline

SEE Testing of Six Components

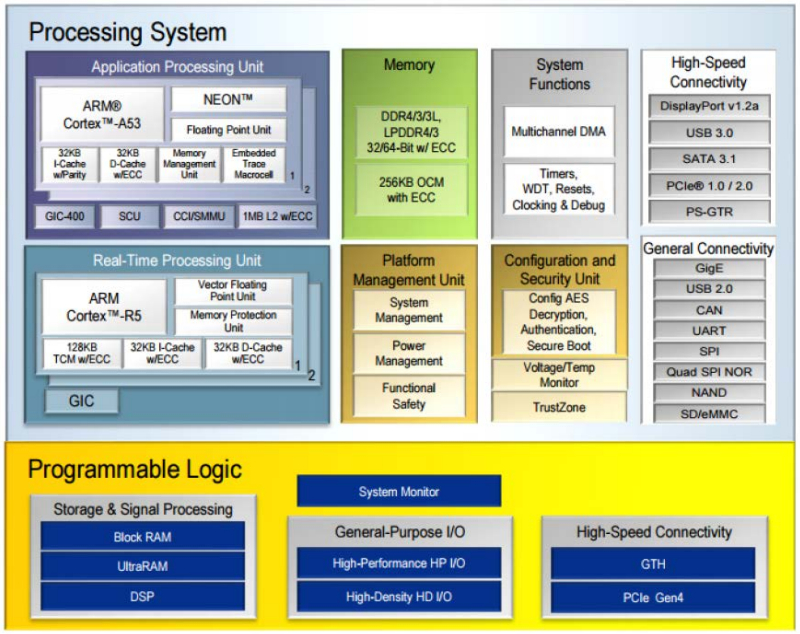
Type	Manufacturer	Part	Techno	HI	Proton	Electron
FPGA	Xilinx	ZU3CG	TSMC 16FF	✓	✓	✓
SoC	Atmel	SAMV71 Space	130 nm	✓	✓	
SRAM	Renesas	R1RW0416DSB	180 nm	✓	✓	✓
SRAM	ISSI	IS61WV20488BLL-10TLI	65 nm	✓		
SRAM	Cypress	CY7C2562XV18-450BZXC-ND	65 nm	✓		
SRAM	OnSemi	N01S830HAT22I	na	✓		
SRAM	anonymous	anonymous	28 nm	✓	✓	✓

- 1 FPGA, 1 SoC and 4+1 SRAMs to be tested
- Those marked in black are completed

Selected Parts

Xilinx - ZU3CG

TSMC 16nm FF



<u>Processing System (PS)</u>

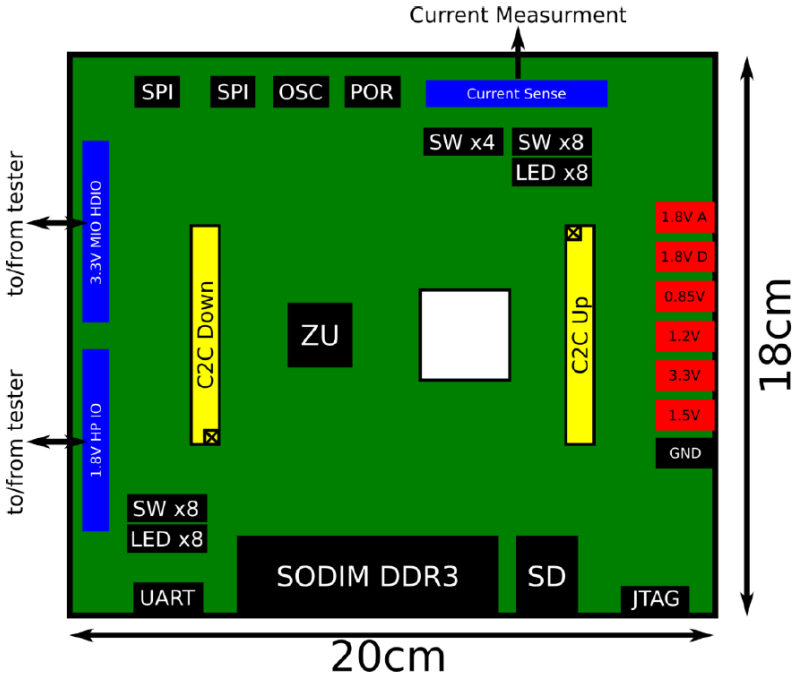
4xCortex A53 (1.2 GHz), 32KB L1I$, 32KB L1D$, 1MB L2$

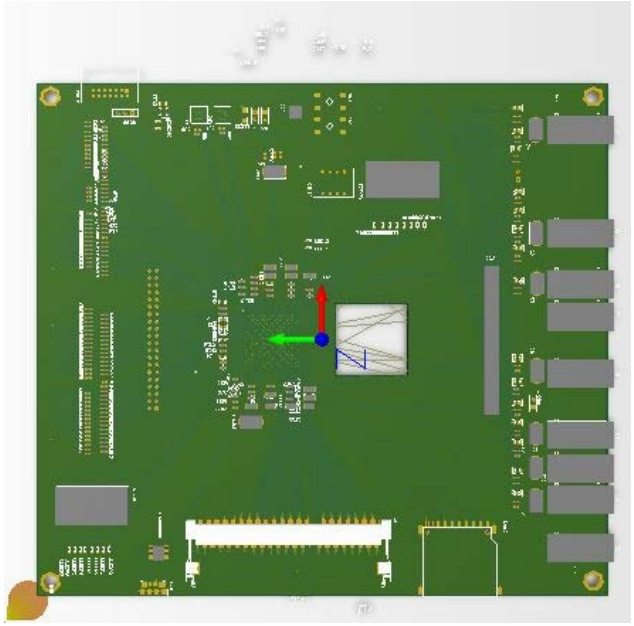
2xCortex-R5 (500 MHz), 32KB L1$, 128KB TCM

<u>Programmable Logic (PL)</u>

154K CLBs, 7.6Mb BRAM

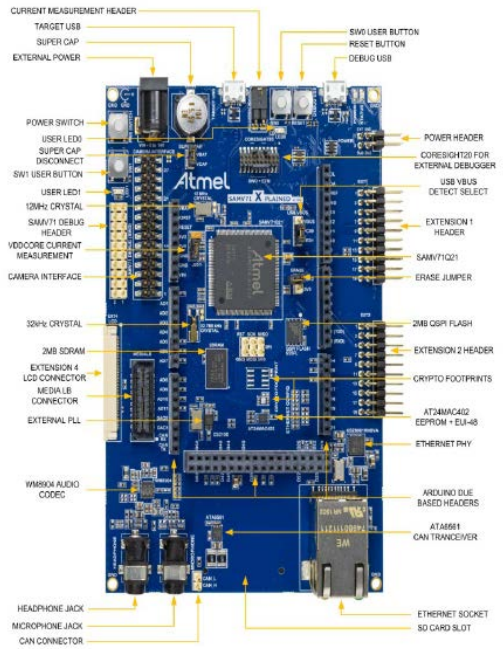
Xilinx - ZU3CG Card

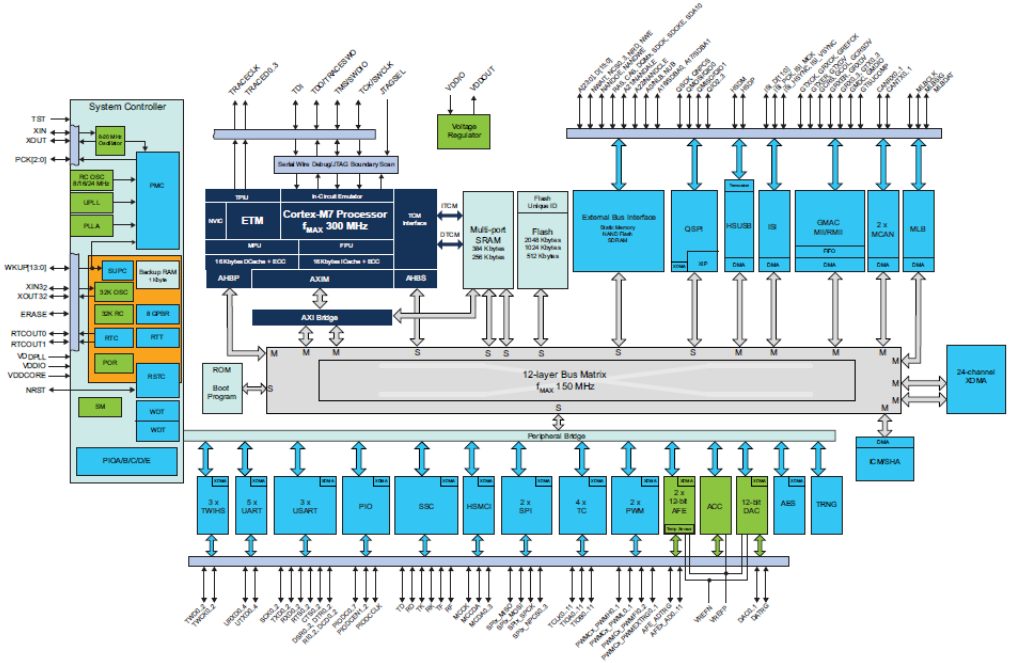




- 5 different supply voltages
- 15 different channels for current monitoring
- Dedicated IOs for processor and PS and PL to tester
- Support for DDR3 SODIM
- Designed so 2 cards can be stacked to increase event counts

Atmel SAMV71

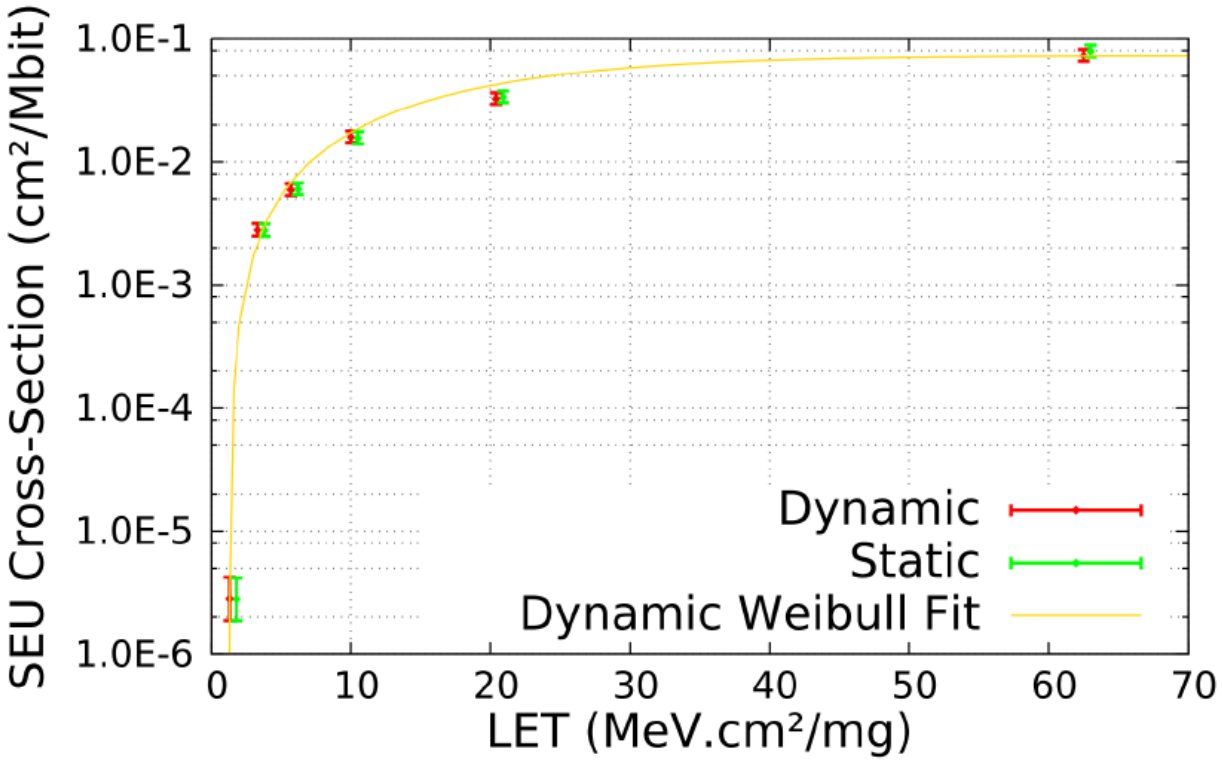




- Automotive version partially hardened for space application
- ARM M7 @ 300 MHz, 16 KB I$(ECC), 16 KB D$(ECC), FPU
- 2MB Embedded Flash
- 128KB TCM
- ENET MAC, USB 2.0, 2xCAN-FD, UARTs, I2C, QPSI, RTC, RTT

Initial Results

Renesas R1RW0416DSB



- SEU test results (UCL)
- Static and dynamic test algorithms – very similar

Unusual Failure Modes

SEFI type failure mode

Transient MBU Read (TMBUR):

- MBUs on burst of consecutive reads (35..100 clks @40MHz)
- After the burst, read data is good
- No need to re-write cells for data to be corrected
- Input address during the burst does not matter

Transient MBU Write (TMBUW):

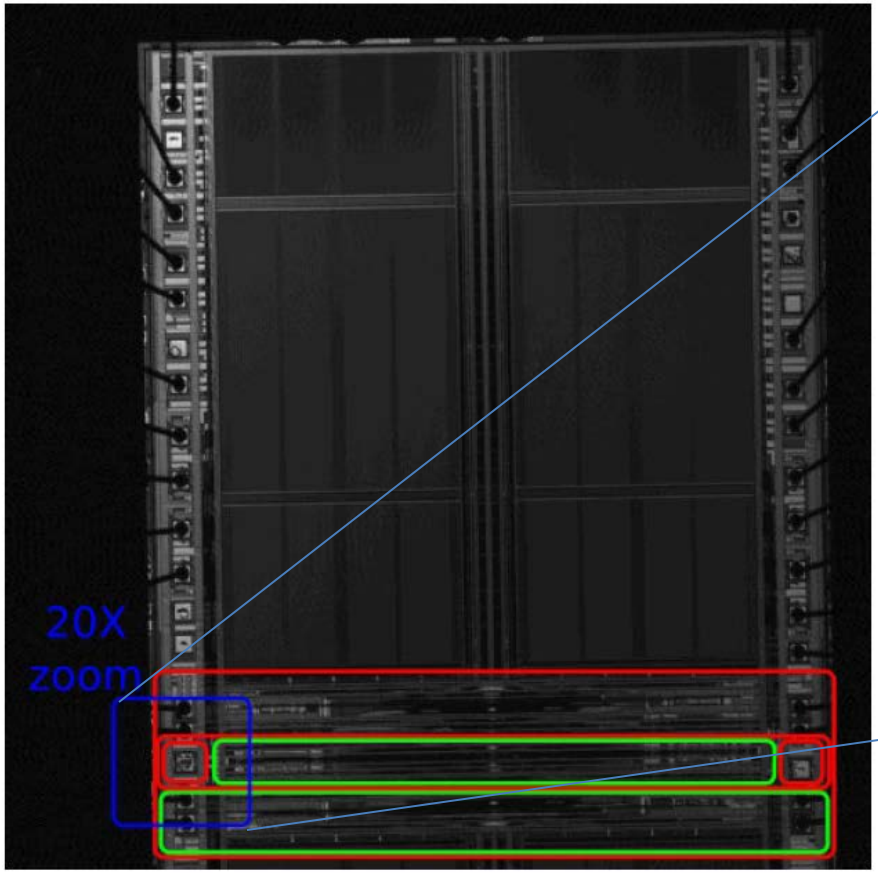
- MBUs occur while writing a range of addresses (≈30)
- Even if these addresses are read much later, MBUs still present
- Writing new data removes the problem

Only observed at LET ≥20 MeV·cm^2/mg

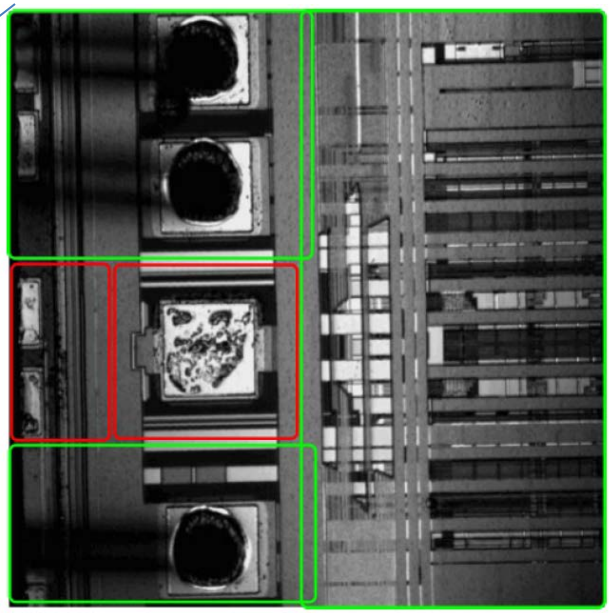
Example TMBUR Sequence

```
2016-12-15    14:39:01.521   WRITE                          #Write memory from address 0 to 3FFFF
2016-12-15    14:39:01.544   READ_START
2016-12-15    14:39:01.544   READ_ERROR     1FF8B   0008      #SEU
2016-12-15    14:39:01.550   READ_ERROR     2C470   0800      #SEU
2016-12-15    14:39:01.550   READ_ERROR     2C570   0800      #SEU
2016-12-15    14:39:01.551   READ_ERROR     2E7F7   4000      #SEU
2016-12-15    14:39:01.560   READ_FINISH
2016-12-15    14:39:01.560   READ_START
2016-12-15    14:39:01.562   READ_ERROR     0DDDA   2020      #TMBUR Begin
2016-12-15    14:39:01.562   READ_ERROR     0DDDB   2020      #TMBUR
2016-12-15    14:39:01.562   READ_ERROR     0DDDC   2020      #TMBUR
2016-12-15    14:39:01.562   READ_ERROR     0DDDD   2020      #TMBUR
2016-12-15    14:39:01.562   READ_ERROR     0DDDE   AAAA      #TMBUR
2016-12-15    14:39:01.562   READ_ERROR     0DDDF   AAAA      #TMBUR
29 similar line with address from 0DDE0 to 0DDFC snipped
2016-12-15    14:39:01.562   READ_ERROR     0DDFD   AAAA      #TMBUR
2016-12-15    14:39:01.562   READ_ERROR     0DDFE   AAAA      #TMBUR
2016-12-15    14:39:01.562   READ_ERROR     0DDFF   AAAA      #TMBUR
2016-12-15    14:39:01.562   READ_ERROR     0DE2C   8A88      #TMBUR End
2016-12-15    14:39:01.562   READ_ERROR     0DF51   0008      #SEU - new SEU that appeared
2016-12-15    14:39:01.564   READ_ERROR     1FF8B   0008      #SEU - repeated from previous iteration
2016-12-15    14:39:01.565   READ_ERROR     2C470   0800      #SEU - repeated from previous iteration
2016-12-15    14:39:01.565   READ_ERROR     2C570   0800      #SEU - repeated from previous iteration
2016-12-15    14:39:01.565   READ_ERROR     2DC51   0008      #SEU - new SEU that appeared
2016-12-15    14:39:01.565   READ_ERROR     2E7F7   4000      #SEU - repeated from previous iteration
2016-12-15    14:39:01.567   READ_FINISH
2016-12-15    14:39:01.567   READ_START                       # MBUs from 0DDDA..0DE2C no longer appear
2016-12-15    14:39:01.568   READ_ERROR     0DF51   0008      #SEU - repeated from previous iteration
2016-12-15    14:39:01.569   READ_ERROR     18226   0800      #SEU - new SEU that appeared
2016-12-15    14:39:01.570   READ_ERROR     1C226   0800      #SEU - new SEU that appeared
2016-12-15    14:39:01.570   READ_ERROR     1FF8B   0008      #SEU - repeated from previous iterations
2016-12-15    14:39:01.571   READ_ERROR     2C470   0800      #SEU - repeated from previous iterations
2016-12-15    14:39:01.571   READ_ERROR     2C570   0800      #SEU - repeated from previous iterations
2016-12-15    14:39:01.572   READ_ERROR     2DC51   0008      #SEU - repeated from previous iterations
2016-12-15    14:39:01.572   READ_ERROR     2E7F7   4000      #SEU - repeated from previous iterations
2016-12-15    14:39:01.573   READ_ERROR     3A846   4000      #SEU - new SEU that appeared
2016-12-15    14:39:01.573   READ_ERROR     3F8F8   0400      #SEU - new SEU that appeared
2016-12-15    14:39:01.573   READ_FINISH
```

Laser Investigation



20x zoom



- Red area – TMBUR observed
- Green area – no errors observed
- Sensitive area -> unbonded pad
- Root Cause Analysis underway

Looking Ahead

Looking Ahead

- Completion of test-setup for Xilinx UltraScale+ and SAMV71
- HI and proton testing of these parts in May-June 2017
- Electron testing in fall 2017