

Comprehensive SEE Qualification

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Outline

Project Outline

Select Parts

- > SRAMs
- FPGA Xilinx Ultrascale+ ZU3CG
- SoC Atmel SAMV71
- Initial Results
- Looking ahead



Project Outline



SEE Testing of Six Components

Туре	Manufacturer	Part	Techno	н	Proton	Electron
FPGA	Xilinx	ZU3CG	TSMC 16FF	\checkmark	\checkmark	\checkmark
SoC	Atmel	SAMV71 Space	130 nm	\checkmark	\checkmark	
SRAM	Renesas	R1RW0416DSB	180 nm	\checkmark	√	\checkmark
SRAM	ISSI	IS61WV20488BLL- 10TLI	65 nm	√		
SRAM	Cypress	CY7C2562XV18- 450BZXC-ND	65 nm	✓		
SRAM	OnSemi	N01S830HAT22I	na	\checkmark		
SRAM	anonymous	anonymous	28 nm	√	✓	\checkmark

- > 1 FPGA, 1 SoC and 4+1 SRAMs to be tested
- Those marked in black are completed



Selected Parts



Xilinx - ZU3CG

TSMC 16nm FF

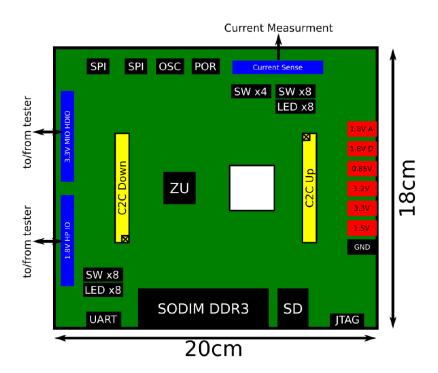
Application Processing Unit	Memory	System Functions	High-Speed Connectivity	
ARM® Cortex™-A53 Floating Point Unit 32KB 32KB Memory Embedded	DDR4/3/3L, LPDDR4/3 32/64-Bit w/ ECC	Multichannel DMA	DisplayPort v1.2a USB 3.0 SATA 3.1	
HCache D-Cache Management Trace Mercocel Unit Macrocel GIC-400 SCU CCI/SMIMU 1MB L2 v	2 256KB OCM with ECC	Timers, WDT, Resets, Clocking & Debug	PCIe® 1.0 / 2.0 PS-GTR	
Vector Floating Point Unit ARM Cortex™-R5 Vector Floating Point Unit 128KB TCM wECC 32KB I-Cache wECC 32KB D-Cache wECC GIC 32KB D-Cache 32KB D-Cache	1 2 Platform Management Unit System Management Power Management Functional Safety	Configuration and Security Unit Config AES Decryption, Authentication, Secure Boot Voltage/Temp Monitor TrustZone	General Connecti GigE USB 2.0 CAN UART SPI Quad SPI NOR NAND SD/eMMC	
rogrammable Logic Storage & Signal Processing Block RAM	System Monitor General-Purpose I/O	High-Spe	eed Connectivity	
UltraRAM	High-Performance HP I/O		GTH	

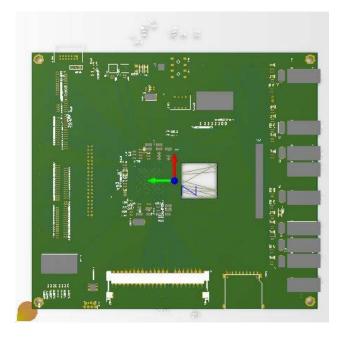
Processing System (PS) 4xCortex A53 (1.2 GHz), 32KB L1I\$, 32KB L1D\$, 1MB L2\$ 2xCortex-R5 (500 MHz), 32KB L1\$, 128KB TCM

Programmable Logic (PL) 154K CLBs, 7.6Mb BRAM



Xilinx - ZU3CG Card

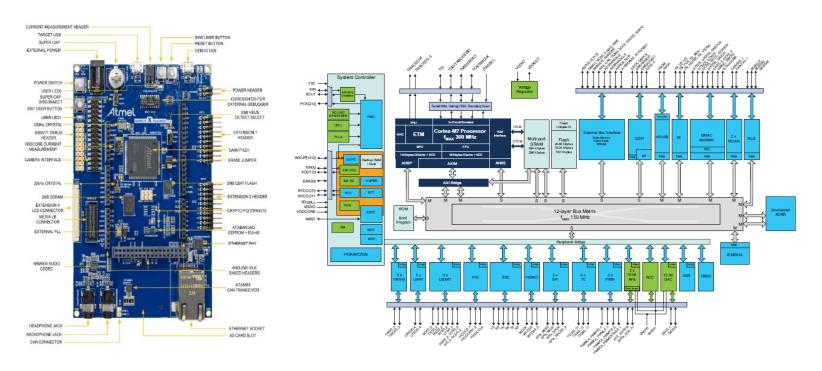




- 5 different supply voltages
- 15 different channels for current monitoring
- Dedicated IOs for processor and PS and PL to tester
- Support for DDR3 SODIM
- Designed so 2 cards can be stacked to increase event counts



Atmel SAMV71



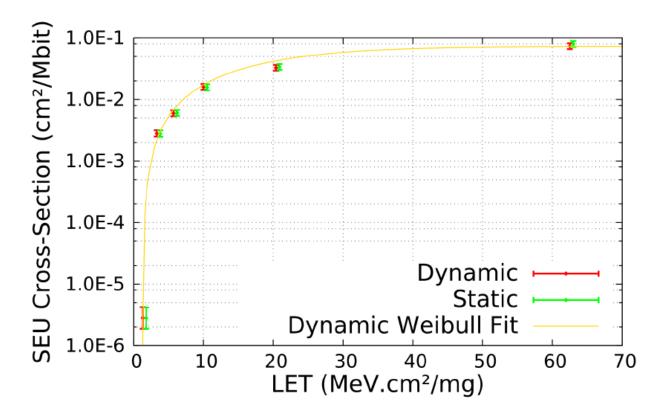
- > Automotive version partially hardened for space application
- > ARM M7 @ 300 MHz, 16 KB I\$(ECC), 16 KB D\$(ECC), FPU
- 2MB Embedded Flash
- ▶ 128KB TCM
- ► ENET MAC, USB 2.0, 2xCAN-FD, UARTs, I2C, QPSI, RTC, RTT



Initial Results



Renesas R1RW0416DSB



SEU test results (UCL)

Static and dynamic test algorithms – very similar



Unusual Failure Modes

SEFI type failure mode

Transient MBU Read (TMBUR):

- ➢ MBUs on burst of consecutive reads (35..100 clks @40MHz)
- After the burst, read data is good
- > No need to re-write cells for data to be corrected
- Input address during the burst does not matter

Transient MBU Write (TMBUW):

- MBUs occur while writing a range of addresses (≈30)
- Even if these addresses are read much later, MBUs still present
- Writing new data removes the problem

Only observed at LET ≥20 MeV·cm²/mg



Example TMBUR Sequence

2016-12-15	14:39:01.521	WRITE			#Write n
2016-12-15	14:39:01.544	READ_START			
2016-12-15	14:39:01.544	READ_ERROR	1FF8B	0008	#SEU
2016-12-15	14:39:01.550	READ_ERROR	2C470	0800	#SEU
2016-12-15	14:39:01.550	READ_ERROR	2C570	0800	#SEU
2016-12-15	14:39:01.551	READ_ERROR	2E7F7	4000	#SEU
2016-12-15	14:39:01.560	READ_FINISH			
2016-12-15	14:39:01.560	READ_START			
2016-12-15	14:39:01.562	READ_ERROR	0 DDDA	2020	#TMBU
2016-12-15	14:39:01.562	READ_ERROR	0 DDDB	2020	#TMBU
2016-12-15	14:39:01.562	READ_ERROR	0 DDDC	2020	#TMBU
2016-12-15	14:39:01.562	READ_ERROR	ODDDD	2020	#TMBU
2016-12-15	14:39:01.562	READ_ERROR	ODDDE	AAAA	#TMBU
2016-12-15	14:39:01.562	READ_ERROR	ODDDF	AAAA	#TMBU
	line with address	from ODDE0 to	ODDFC sn		
2016-12-15	14:39:01.562	READ_ERROR	ODDFD	AAAA	#TMBU
2016-12-15	14:39:01.562	READ_ERROR	ODDFE	AAAA	#TMBU
2016-12-15	14:39:01.562	READ_ERROR	ODDFF	AAAA	#TMBU
2016-12-15	14:39:01.562	READ_ERROR	0DE2C	8A88	#TMBU
2016-12-15	14:39:01.562	READ_ERROR	0DF51	0008	#SEU
2016-12-15	14:39:01.564	READ_ERROR	1FF8B	0008	#SEU
2016-12-15	14:39:01.565	READ_ERROR	2C470	0800	#SEU
2016-12-15	14:39:01.565	READ_ERROR	2C570	0800	#SEU
2016-12-15	14:39:01.565	READ_ERROR	2DC51	0008	#SEU
2016-12-15	14:39:01.565	READ_ERROR	2E7F7	4000	#SEU
2016-12-15	14:39:01.567	READ_FINISH			
2016-12-15	14:39:01.567	READ_START			# MB1
2016-12-15	14:39:01.568	READ_ERROR	0DF51	0008	#SEU
2016-12-15	14:39:01.569	READ_ERROR	18226	0800	#SEU
2016-12-15	14:39:01.570	READ_ERROR	1C226	0800	#SEU
2016-12-15	14:39:01.570	READ_ERROR	1FF8B	0008	#SEU
2016-12-15	14:39:01.571	READ_ERROR	2C470	0800	#SEU
2016-12-15	14:39:01.571	READ_ERROR	2C570	0800	#SEU
2016-12-15	14:39:01.572	READ_ERROR	2DC51	0008	#SEU
2016-12-15	14:39:01.572	READ_ERROR	2E7F7	4000	#SEU
2016-12-15	14:39:01.573	READ_ERROR	3A846	4000	#SEU
2016-12-15	14:39:01.573	READ_ERROR	3F8F8	0400	#SEU
2016-12-15	14:39:01.573	READ_FINISH			

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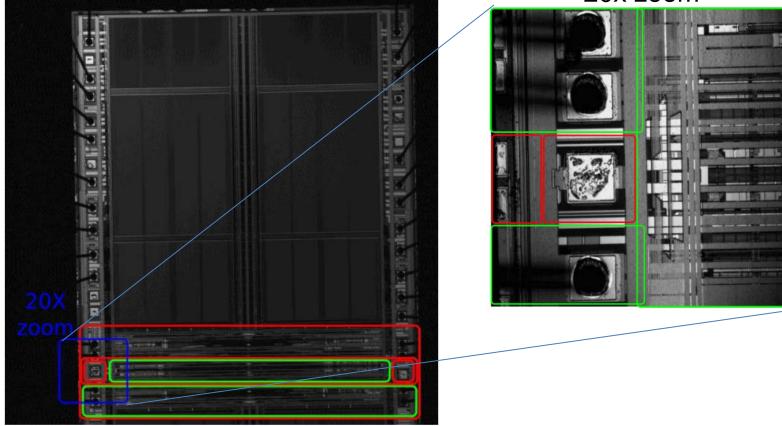
#Write memory from address 0 to 3FFFF

#SEU	
#SEU	
#SEU	
#SEU	
#TMBUR	Begin
#TMBUR	
#TMBUR	
#TMBUR	
#TMBUR	
#TMBUR	End
#SEU -	new SEU that appeared
#SEU -	repeated from previous iteration
#SEU -	repeated from previous iteration
#SEU -	repeated from previous iteration
#SEU -	new SEU that appeared
#SEU -	repeated from previous iteration
# MBUs	from ODDDAODE2C no longer appear
	repeated from previous iteration
#SEU -	new SEU that appeared
#SEU -	new SEU that appeared
#SEU -	repeated from previous iterations
#SEU -	repeated from previous iterations
#SEU -	repeated from previous iterations
#SEU -	repeated from previous iterations
#SEU -	repeated from previous iterations
#SEU -	new SEU that appeared
	new SEU that appeared



Laser Investigation





- Red area TMBUR observed
- Green area no errors observed
- Sensitive area -> unbonded pad
- Root Cause Analysis underway



Looking Ahead



Looking Ahead

- Completion of test-setup for Xilinx UltraScale+ and SAMV71
- ➢ HI and proton testing of these parts in May-June 2017
- Electron testing in fall 2017