JUICE NAND FLASHs Total dose radiation tolerance

ESA-CNES Radiation Final Presentation Days on Space Environments and Radiation Effects on EEE components

ITT AO/1-7740/13/NL/HB - Radiation testing of memories for the JUICE Mission

Main objective: Assess commercial state-of-the art memories radiation tolerance for JUICE mission.

Presentation focused on **Nand Flash total dose radiations tolerance**

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March 2017

Outline

- Parts selection
- Reverse Construction Analysis
- Test plan
- Test tooling description
- Results
- Conclusion

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NAND FLASH parts selection

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Parts Selection and criteria

- **Key drivers for memory selection:**
  - Mission lifetime is more than 11 years in space (7.6 years cruise and 3.5 years in the Jovian system).
  - Without massive shielding mass, total ionizing dose required 200 kRad(Si).
  - Minimum total dose tolerance should be 50 kRad(Si) with sufficient shielding mass.
  - Storage capacity as a minimum 60 Gb and up to 500 Gb
  - Download data rate < 100 Mbps

- **Parts selection has been performed according to the following criteria :**
  - State of the art technology (end of 2015, beginning of 2016).
  - Non obsolescence of the memory and new devices that haven't been already tested against radiations.
  - Size and architecture.
  - SLC (Single Level Cell) only for radiation tolerance purpose.
  - Package

	Hynix	*Toshiba*	*Macronix*	*Spansion*	*Winbond*
Part type	H27U4G8F2D	TC58NVG2S0HTAI0	MX30LF4G18AC	S34ML04G200TFI00	W29N01GVSIAA
Type	SLC Nand Flash Memory	SLC Nand Flash Memory	SLC Nand Flash Memory	SLC Nand Flash Memory	SLC Nand Flash Memory
Capacity / Organization	4 GB / 512M x 8BIT 1 bit ECC/528 bytes	4 GB / 512M x 8BIT 8 bit ECC/512 bytes	4 GB / 512M x 8 BIT 4 bit ECC	4 GB / 512M x 8 BIT 4 bit ECC	1 GB / 128M x 8 BIT 1 bit ECC/528 bytes
Date code	1503	1509	1444	1442	1437
Package	TSOP48 (12x20mm)	TSOP48 (12x20mm)	TSOP48 (12x20mm)	TSOP48 (12x20mm)	TSOP48 (12x20mm)

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Reverse Construction Analysis

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NAND FLASHs
Construction Analysis summary

- Main challenge for this type of technology is the process capability with the die manufacturing lithography and etching tools. **Repeatability of cell spacing Air Gap and minimum Critical Dimension (CD's) patterns definition are most likely the main yield detractors on these parts.**

Hard Mask – Allow to keep the lithography resolution during etching (deals with selectivity photo resist poly when Etch process)

World line control gate Polysilicon

ONO : Oxide Nitride Oxide for charge trapping

Floating gate Polysilicon

Tunnel oxide

50 nm

WL Air-gap

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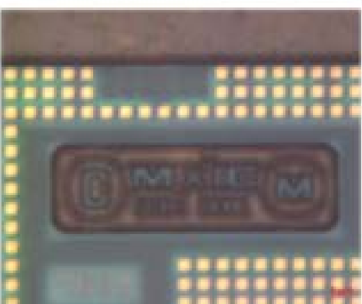
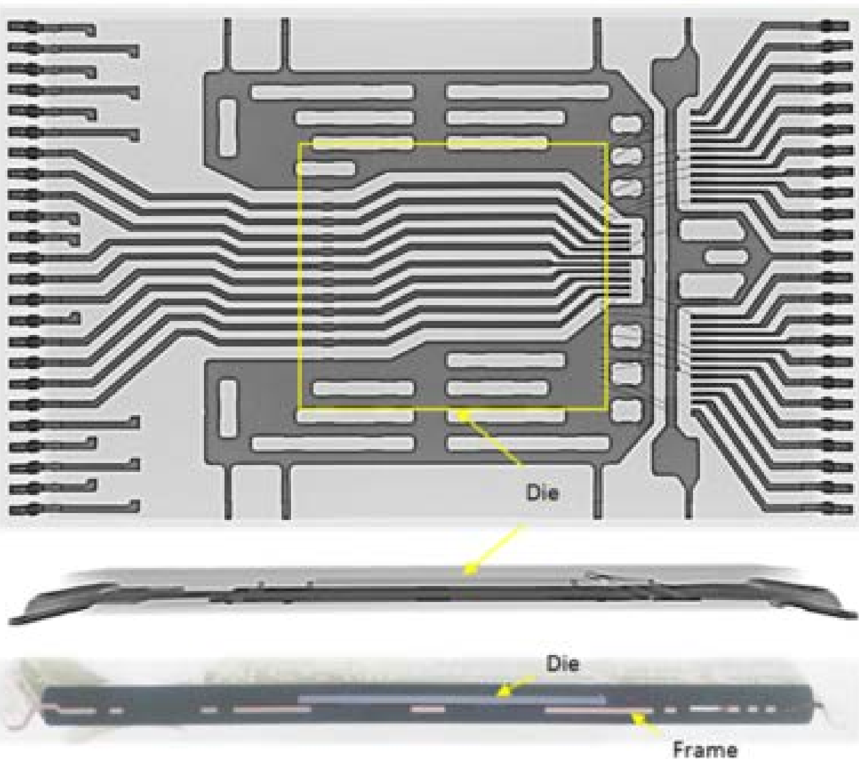
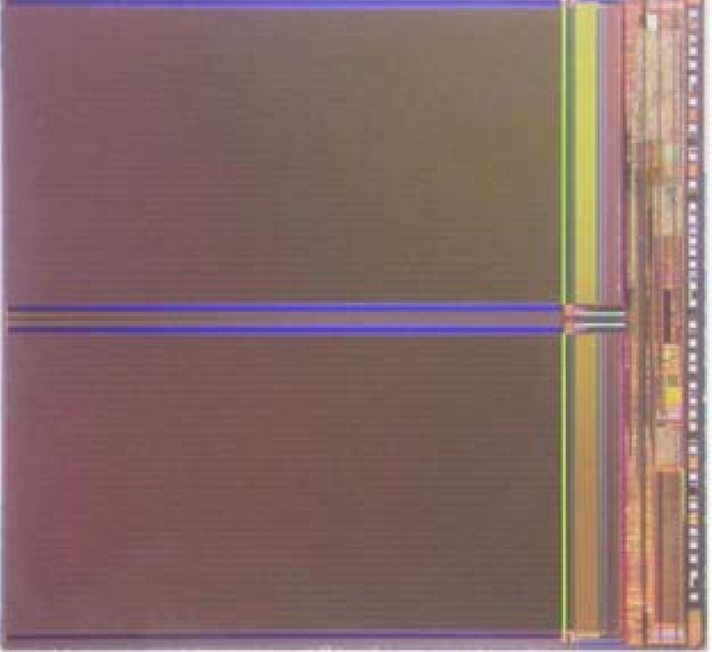
NAND FLASHs

Construction Analysis (Ex: Macronix Nand Flash)



Part type :	MX30LF4G18AC
Marking :	MXIC S144411 MX30LF4G18AC-TI 84112708
Date code :	1444
Packaging :	TSOP48 12 x 20 mm
Die size :	6.9 mm x 7.4 mm
Assembly type :	Top single die, bottom frame bus





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NAND FLASHs
Construction Analysis comparison

	Hynix	*Toshiba*	*Macronix*	*Spansion*	*Winbond*
Die size mm (area mm²)	7.3 x 9.1 (66.4)	4.9 x 6.2 (30.4)	6.9 x 7.4 (51.1)	6.5 x 7.8 (50.7)	5.3 x 5.5 (29.2)
Assembly type	Top single die + Top frame bus	Flip single die + Top frame bus	Top single die + bottom frame bus	Top single die + bottom frame bus	Top single die + bottom frame bus
Serial word lines	34	66	34	34	32
Memory/Digital area (%)	62% / 38%	47% / 53%	74% / 26%	56% / 44%	43% / 57%
Memory cell area (µm²)	0.0071	0.0025	0.0056	0.0042	0.0083
Minimum pitch (nm)	83	48	65	64	91
Critical dimension (nm)	41	24	32	32	45
Air gap (top cells level)	Yes	No	Partial	Yes	No
Cells (bit line axis)					

Bit line
Ground Select (*) | Word L0 | Word L1 | Word L2 | Word L64 | Word L65 | Word L66 | Bit L Select (*)

(*) Access transistors Ground select and Bit line select without ONO

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NAND FLASHs
Construction Analysis comparison

Die and Cell Areas on Nand Flash Memory

Die Area (mm²): 0, 10, 20, 30, 40, 50, 60, 70

Cell Area (µm²): 0, 0.001, 0.002, 0.003, 0.004, 0.005, 0.006, 0.007, 0.008, 0.009

Hynix *Toshiba* *Macronix* *Spansion* *Winbond*

Memory Die Area (mm²) Digital Die Area (mm²) Cell Area (µm²)

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Test plan

- For each reference :
  - 10 devices in HDC (High Duty Cycle) bias
  - 10 devices in LDC (Low Duty Cycle) bias
  - 10 OFF devices (pins connected to ground)
- Devices are irradiated up to 200 Krad (Si) with Co60
- Power monitoring of DUT bias board
- Electric Measurements steps are performed at 20, 30, 50, 100, 150 and 200 Krad (Si)
- After irradiation, 24h @25°C and 168h @100°C annealing are performed on devices
- Electric Measurements steps are performed after each annealing

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In situ: FPGA based tester and biasing boards
Software description HDC (High Duty Cycle)

Check factory Bad blocks

Start Block 1 to 2047

Erase Block

Write Program #55 (H)

Check (Read & compare) pattern #55 (H)

Erase Block

Write Program #AA (H)

Check (Read & compare) pattern #AA (H)

Start Block 2048 to 4095

Erase Block

Write Program #AA(H)

Check (Read & compare) pattern #AA (H)

Retention check

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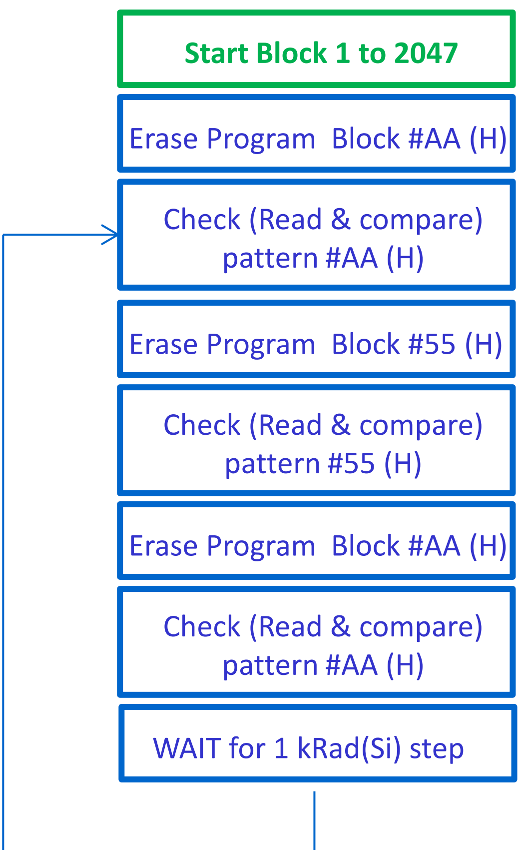
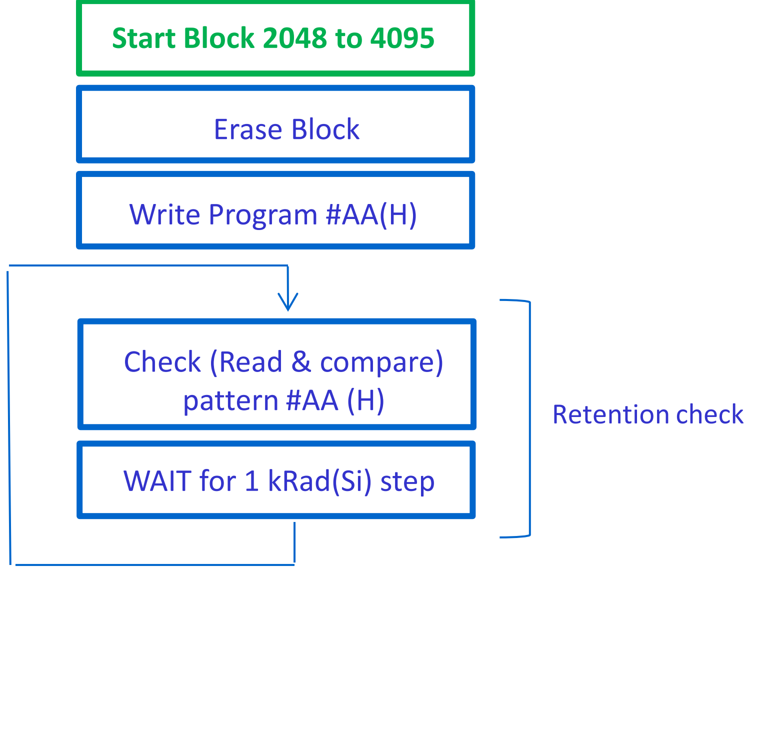
In situ: FPGA based tester and biasing boards
Software description LDC (Low Duty Cycle)

Check factory Bad blocks





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Electrical test system description

Parameter tests list table (Macronix as an example)

PARAMETERS	SYMBOLS	TEST CONDITIONS	MIN	MAX	UNITS
DC					
Continuity Neg	Cont_Neg	Iin=-100uA	-1.5	-0.2	V
Input Leakage Current Low	ILIL	Vin=0V , VCC= VCCmax (3.6V)	-10	10	µA
Input Leakage Current High	ILIH	Vin= VCC= VCCmax (3.6V)	-10	10	µA
Output Leakage Current Low	ILOL	Vout=0V , Vcc = 3.6V DQ are disabled	-10	10	µA
Output Leakage Current High	ILOH	Vout=VCCmax, Vcc = 3.6V DQ are disabled	-10	10	µA
Output Low Voltage	VOL	IOL=2.1mA, Vcc = 3.3V	0.4	-	V
Output High Voltage	VOH	IOH=-400uA Vcc = 3.3V	-	2.4	V
Input Low Voltage	VIL	Vcc = 3.3V	-	0.66	V
Input High Voltage	VIH	Vcc = 3.3V	2.64	-	V
Power supply (VCC =3.3V)					
Operating Current, Page Read	ICC1_CODE	trc=25ns CE/=Vil, Iout=0mA	-	30	mA
Operating Current, Program	ICC2_CODE	-	-	30	mA
Operating Current, Erase	ICC3_CODE	-	-	30	mA
Standby Current TTL	ISB_ICC4	CE/=VIH , WP/=0V/VCC, VCC & VCCQ	-	1	mA
Standby Current CMOS	ISB_ICC5	CE/=VCC-0.2V , WP/=0V/VCC, VCC & VCCQ	-	50	µA

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Electrical test system description

Parameter tests list table (Macronix as an example)

AC (VCC=3.3V, Input Pulse Levels =0V to VCC , Input and Output Timing Levels=VCC/2) Mode 0 Load 1 TTL gate					
Program Time	tProg	PROGRAM PAGE operation time, internal ECC disabled, GO NOGO	-	600	µs
Block Erase Time	tBers	BLOCK ERASE operation time , GO NOGO	-	3.5	ms
CLE Setup Time	tCLS	-	-	10	ns
CLE Hold Time	tCLH	-	-	5	ns
CE/ Setup Time	tCS	-	-	15	ns
CE/ Hold Time	tCH	GO NOGO	-	5	ns
WE/ Pulse Width	tWP	-	-	10	ns
ALE Setup Time	tALS	-	-	10	ns
ALE Hold Time	tALH	-	-	5	ns
Data Setup Time	tDS	-	-	7	ns
Data Hold Time	tDH	-	-	5	ns
Write Cycle Time	tWC	-	-	20	ns
WE/ High Hold Time	tWH	GONOGO	-	7	ns
ALE to RE/ Delay	tAR	GO NOGO	-	10	ns
CLE to RE/ Delay	tCLR	GO NOGO	-	10	ns
RE/ Pulse Width	tRP	-	-	10	ns
Read Cycle Time	tRC	-	-	20	ns
RE/ Access Time	tREA	-	-	16	ns
WE High to Busy	tWB	-	-	100	ns
CE/ Access Time	tCEA	-	-	25	ns
RE/ High Hold Time	tREH	GO NOGO	-	7	ns
WP/ High to WE/ Low	tWW	GO NOGO	-	100	ns
Functionality					
Checkerboard	Func_ChkBrd	Erase memory Write , Read pattern Checkerboard Block#0 Note 1	-	-	Pass/Fail
SLC-March	Func_SLC_March	Erase memory Write , Read with SLC March Algorithm Block#0	-	-	Pass/Fail
Retention Check	Func_READ_ChkBrd_Retention	Read with $55 $AA on Block#81 (OFF samples only)	-	-	Pass/Fail

Note 1: Pattern checkerboard is made of Erase, Write 55 & AA, Read 55 & AA, Erase, Write AA & 55, Read AA & 55, Erase

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Electrical test system description
Specific SLC – March detection Algorithm

- **Specific March algorithm fore NAND FLASH for :**
  - TF: Transition Fault Detection
  - AF: Address Fault Detection
  - DF: Data Fault Detection

SLC-March employs march algorithm and pattern-based approach to detect all faults.

- The march algorithm detects faults by controlling the operation address order.
- The pattern P_{SLC} detects faults happened in a page

SAF, SOF

$$SLC - March = \{(e);\Uparrow(r1, w0, r0);\Updownarrow(r0); (e);\Downarrow(r1, wP_{SLC}, rP_{SLC});\Updownarrow(rP_{SLC}); (e);\Downarrow(r1, w\overline{P_{SLC}}, r\overline{P_{SLC}});\Updownarrow(r\overline{P_{SLC}})\}$$

TF **AF** **DF**

w0 : a write operation on a page of all-0's pattern
r0/r1: a read operation on a page, expecting all-0's/all-1's pattern

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Test tooling descriptions
Hardware and Software

- In situ (FPGA based tester and biasing boards)
- Electrical test system using an ATE (Automatic Test Equipment)

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In situ: FPGA based tester and biasing boards Hardware description

Bias board

Digital IOs

Control board SMX32C

Ethernet cable

External computer

Power Monitoring

Control board SMX32C

SMX32 Board

300 IO

BUS DRIVER

SPARTAN6 FPGA

PIC32MX

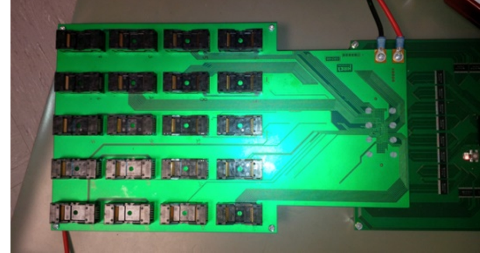
24 FPGA IO

CAN 2.0B

CPU peripherals

USB

ETHERNET 100Mbits



Bias board

➢ User interface app. on PC

- Configures test sequence
- Sends test sequence commands to Control board
- Records error data, status data and log data received from Control board

➢ Control board

- Controls and commands DUTs in parallel
- Sends status and error data to the PC

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Electrical test system Hardware description

Test Program

POGO Tower connection

DUT Board connection

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Overall Campaign Results

- In situ (FPGA based tester and biasing boards).
- Electrical test system using an ATE (Automatic Test Equipment).

- Based on results we have differentiated two families
  - Preselected references for SEE irradiation campaigns
  - Non selected references for SEE irradiation campaigns

HRX – Non selected references (Hynix, Spansion, Winbond)

HRX - Preselected references (Toshiba, Macronix)

	Hynix	Toshiba	Macronix	Spansion	Winbond
Part type	H27U4G8F2D	TC58NVG2S0HTAI0	MX30LF4G18AC	S34ML04G200TFI00	W29N01GVSIAA
Type	SLC Nand Flash Memory	SLC Nand Flash Memory	SLC Nand Flash Memory	SLC Nand Flash Memory	SLC Nand Flash Memory
Capacity / Organization	4 GB / 512M x 8BIT 1 bit ECC/528 bytes	4 GB / 512M x 8BIT 8 bit ECC/512 bytes	4 GB / 512M x 8 BIT 4 bit ECC	4 GB / 512M x 8 BIT 4 bit ECC	1 GB / 128M x 8 BIT 1 bit ECC/528 bytes
Date code	1503	1509	1444	1442	1437
Package	TSOP48 (12x20mm)	TSOP48 (12x20mm)	TSOP48 (12x20mm)	TSOP48 (12x20mm)	TSOP48 (12x20mm)

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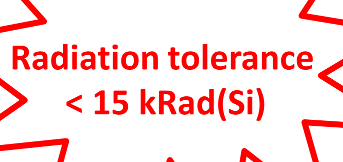
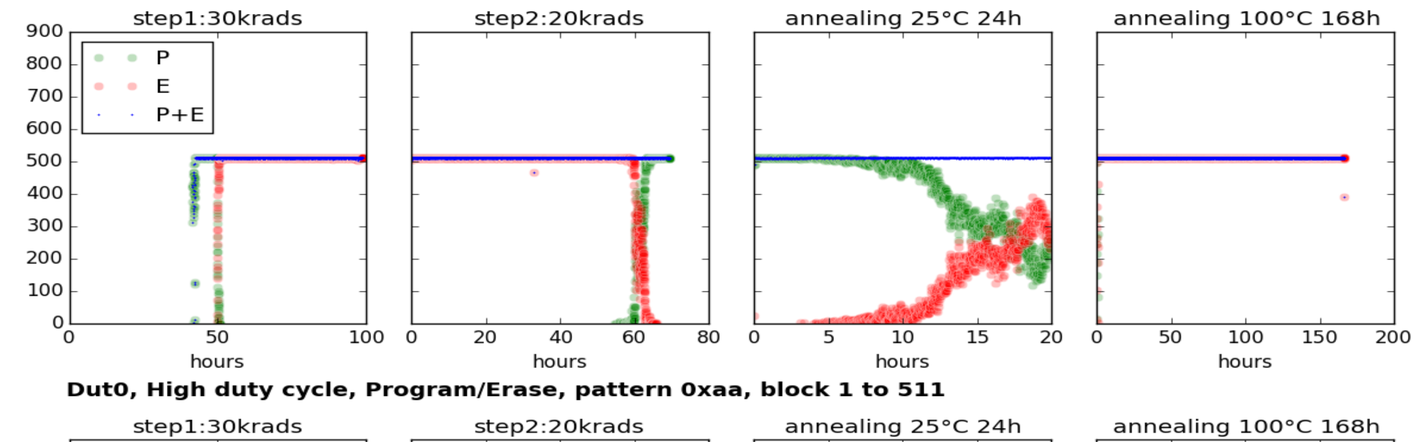
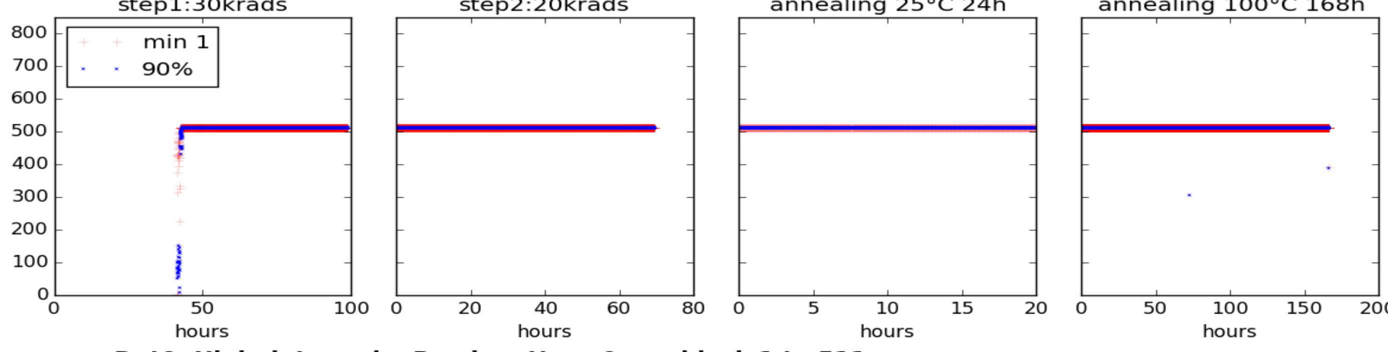
In situ: HDC non selected references results

Winbond
W29N01GVSIAA
SLC Nand Flash Memory
1 GB / 128M x 8 BIT 1 bit ECC/528 bytes
1437
TSOP48 (12x20mm)

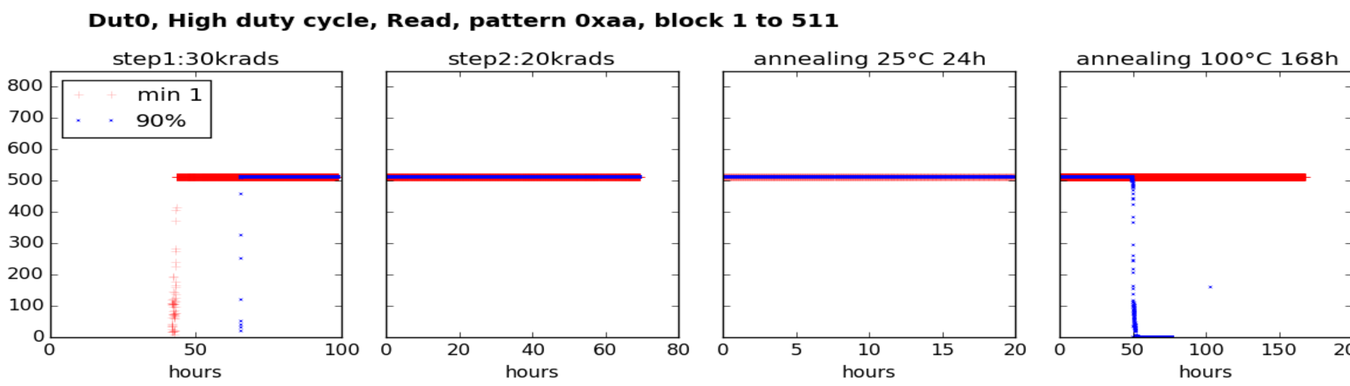




Dut0, High duty cycle, Program/Erase, pattern 0xaa, block 1 to 511



Dut0, High duty cycle, Read, pattern 0xaa, block 1 to 511



Dut0, High duty cycle, Read, pattern 0xaa, block 512 to 1023

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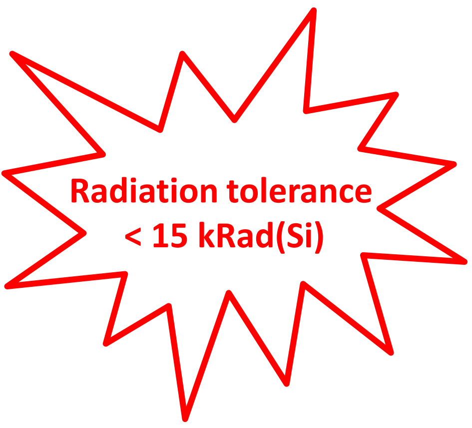
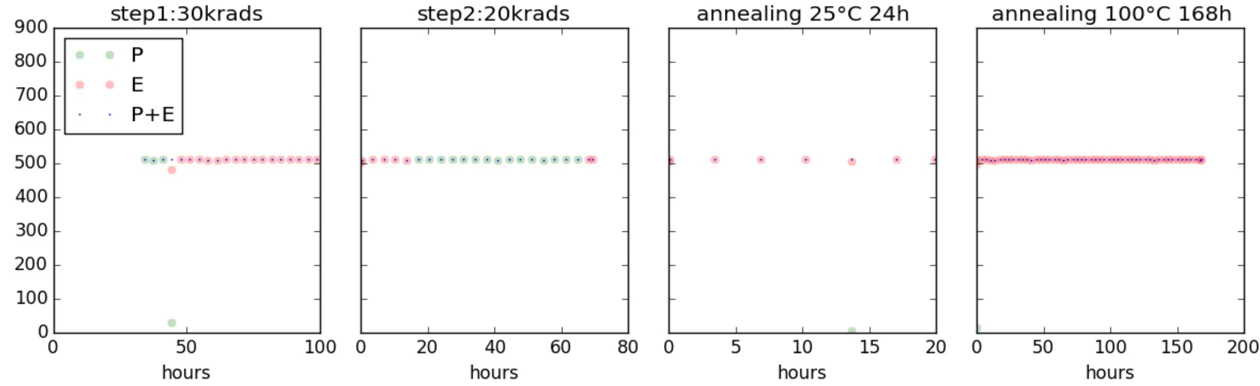
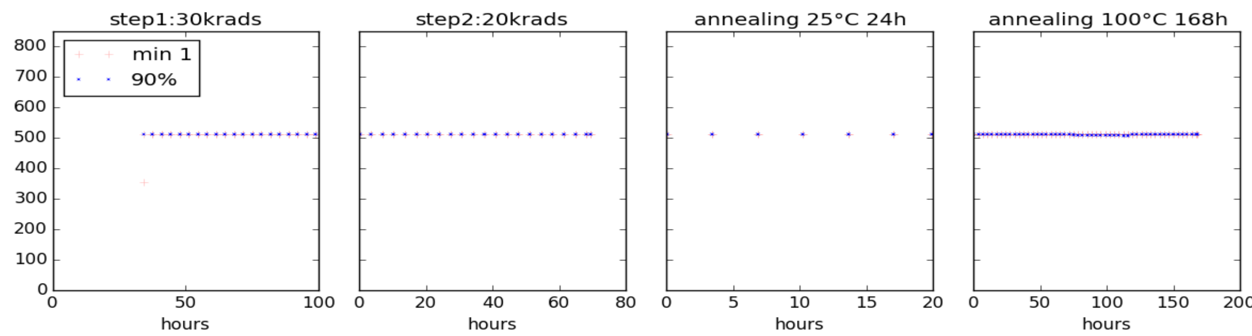
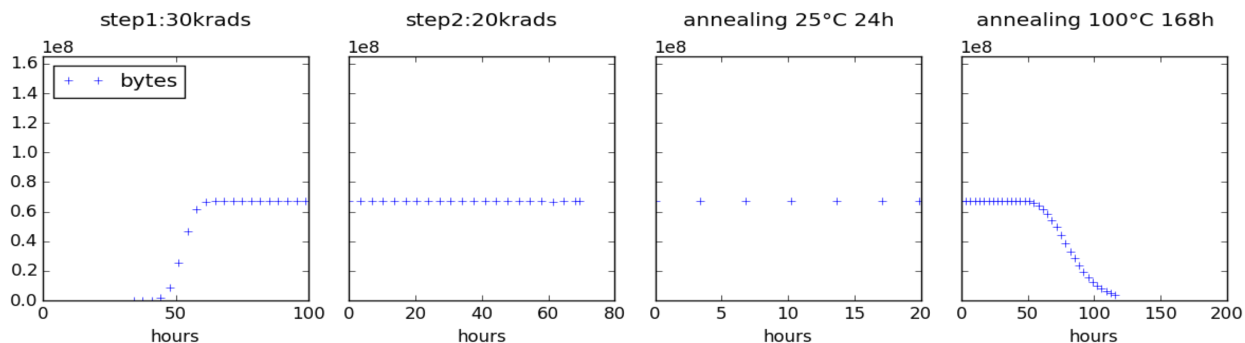
In situ: LDC non selected references results

Winbond
W29N01GVSIAA
SLC Nand Flash Memory
1 GB / 128M x 8 BIT 1 bit ECC/528 bytes
1437
TSOP48 (12x20mm)









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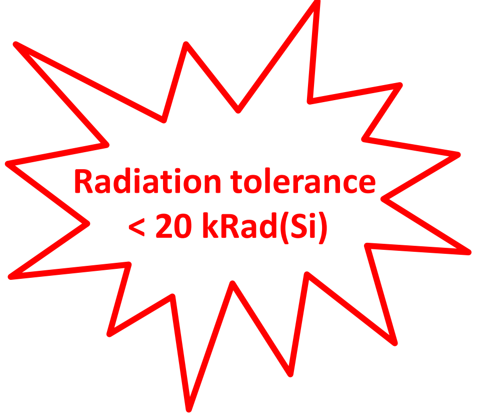
In situ: HDC non selected references results

S34ML04G200TFI00
SLC Nand Flash Memory
4 GB / 512M x 8 BIT 4 bit ECC
1442
TSOP48 (12x20mm)



step1:30krads | step2:20krads | step3:50krads | annealing 25°C 24h | annealing 100°C 168h

Legend: P, E, P+E; x-axis: hours

Dut0, High duty cycle, Program/Erase, pattern 0xaa, block 1 to 2047

step1:30krads | step2:20krads | step3:50krads | annealing 25°C 24h | annealing 100°C 168h

Legend: min 1, 90%; x-axis: hours

Dut0, High duty cycle, Read, pattern 0xaa, block 1 to 2047

step1:30krads | step2:20krads | step3:50krads | annealing 25°C 24h | annealing 100°C 168h

Legend: min 1, 90%; x-axis: hours

Dut0, High duty cycle, Read, pattern 0xaa, block 2048 to 4095

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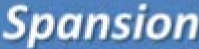
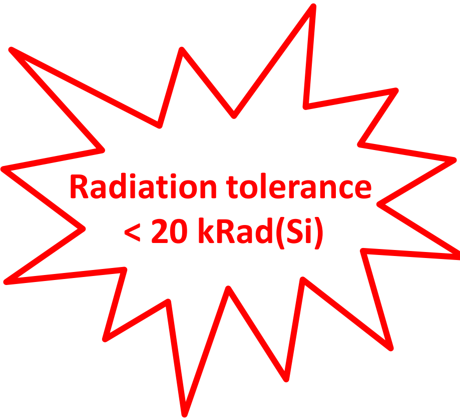
In situ: LDC non selected references results



S34ML04G200TFI00
SLC Nand Flash Memory
4 GB / 512M x 8 BIT 4 bit ECC
1442
TSOP48 (12x20mm)



step1:30krads | step2:20krads | step3:50krads | annealing 25°C 24h | annealing 100°C 168h

P / E / P+E — hours

Dut0, Low duty cycle, Program/Erase, pattern 0xaa, block 1 to 2047

step1:30krads | step2:20krads | step3:50krads | annealing 25°C 24h | annealing 100°C 168h

min 1 / 90% — hours

Dut0, Low duty cycle, Read, pattern 0xaa, block 1 to 2047

step1:30krads | step2:20krads | step3:50krads | annealing 25°C 24h | annealing 100°C 168h

1e8 bytes — hours

Dut0, Low duty cycle, Read, pattern 0xaa, block 1 to 4095

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In situ: HDC non selected references results

Hynix
H27U4G8F2D
SLC Nand Flash Memory
4 GB / 512M x 8BIT 1 bit ECC/528 bytes
1503
TSOP48 (12x20mm)

failed erase blocks (E) · failed program blocks (P) · failed blocks (E+P)

step1 20krads | step2 10krads | step3 20krads | annealing1 25°C 24h | annealing2 100°C 168h | annealing3 100°C 238h

Dut0, High duty cycle, erase/program, pattern 0xaa, block 1 to 2047

hirex eng.

blocks with minimum 1 byte in error · blocks with 90% bytes in error

step1 20krads | step2 10krads | step3 20krads | annealing1 25°C 24h | annealing2 100°C 168h | annealing3 100°C 238h

Dut0, High duty cycle, Read, pattern 0xaa, block 1 to 2047

hirex eng.

blocks with minimum 1 byte in error · blocks with 90% bytes in error

step1 20krads | step2 10krads | step3 20krads | annealing1 25°C 24h | annealing2 100°C 168h | annealing3 100°C 238h

Dut0, High duty cycle, Read, pattern 0xaa, block 2048 to 4095

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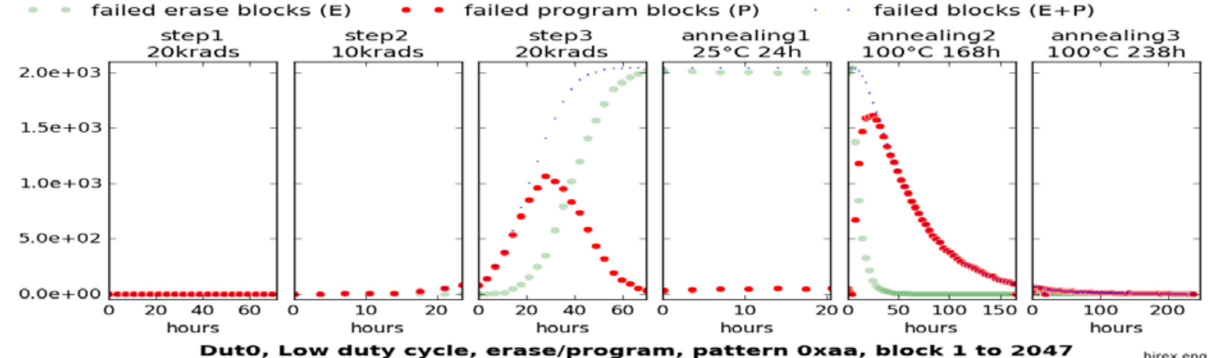
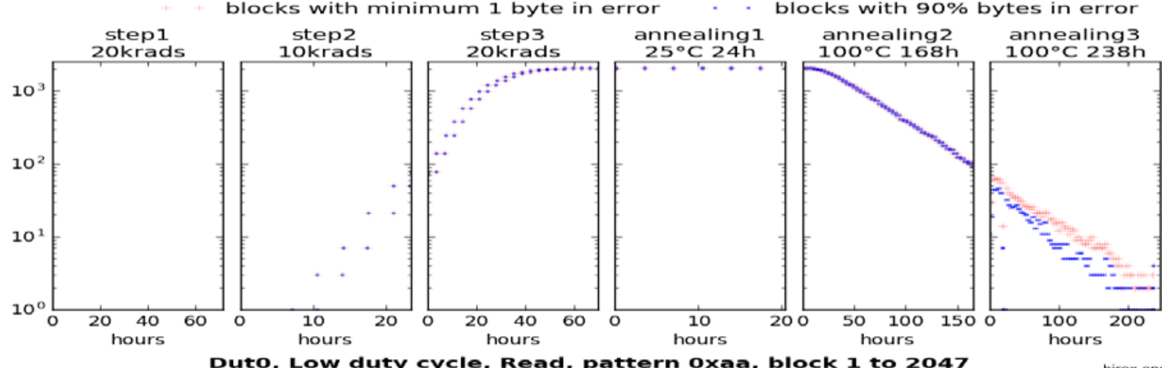
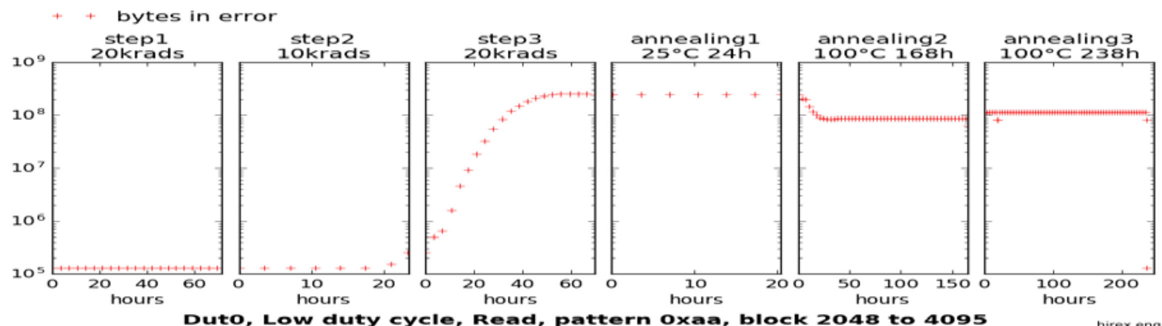
In situ: LDC non selected references results

Hynix
H27U4G8F2D
SLC Nand Flash Memory
4 GB / 512M x 8BIT 1 bit ECC/528 bytes
1503
TSOP48 (12x20mm)







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ATE: HDC and LDC non selected references results

BIAS HDC (HIGH DUTY CYCLE)

Manufacturer	Product	DC		Power Supply		AC (timings)		Functional	
		Steps	Annealing 24h/168h	Steps	Annealing 24h/168h	Steps	Annealing 24h/168h	Steps	Annealing 24h/168h
Winbond	W29N01GVSIAA	30 kRad(Si)	Complete	50 kRad(Si)	Complete	30 kRad(Si)	Complete	30 kRad(Si)	Complete
Spansion	S34ML04G200TFI00	No Failure up to 100kRad(Si)	Complete	No Failure up to 100kRad(Si)	Complete	30 kRad(Si)	No Recovery	30 kRad(Si)	No Recovery
Hynix	H27U4G8F2D	30 kRad(Si)	Partial	No Failure up to 50kRad(Si)	Complete	30 kRad(Si)	Partial	30 kRad(Si)	Partial

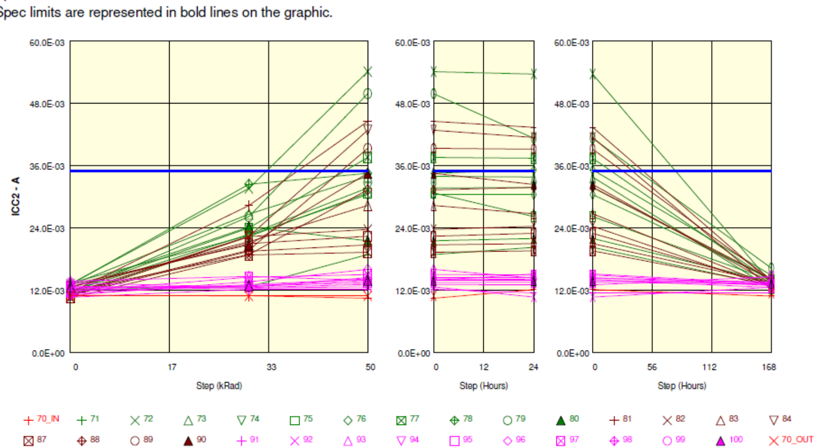
BIAS LDC (LOW DUTY CYCLE)

Manufacturer	Product	DC		Power Supply		AC (timings)		Functional	
		Steps	Annealing 24h/168h	Steps	Annealing 24h/168h	Steps	Annealing 24h/168h	Steps	Annealing 24h/168h
Winbond	W29N01GVSIAA	30 kRad(Si)	Complete	50 kRad(Si)	Complete	30 kRad(Si)	Complete	30 kRad(Si)	Complete
Spansion	S34ML04G200TFI00	No Failure up to 100kRad(Si)	Complete	No Failure up to 100kRad(Si)	Complete	30 kRad(Si)	No Recovery	30 kRad(Si)	No Recovery
Hynix	H27U4G8F2D	30 kRad(Si)	Partial	No Failure up to 50kRad(Si)	Complete	30 kRad(Si)	Partial	30 kRad(Si)	Partial

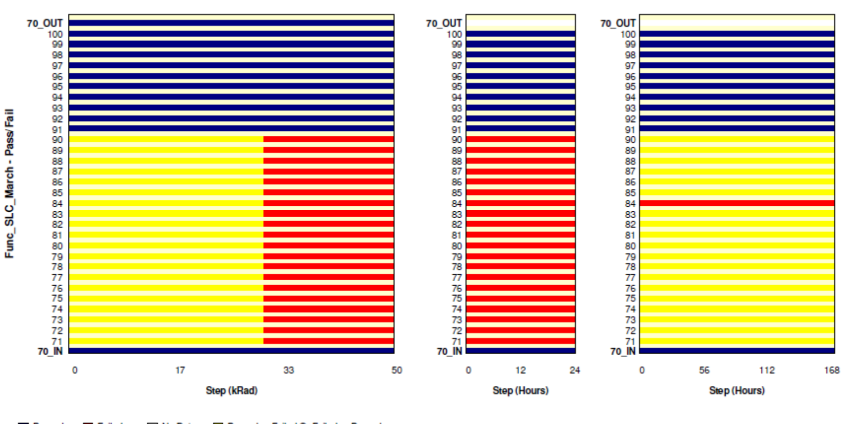
BIAS OFF

Manufacturer	Product	DC		Power Supply		AC (timings)		Functional		Retention	
		Steps	Annealing 24h/168h	Steps	Annealing 24h/168h	Steps	Annealing 24h/168h	Steps	Annealing 24h/168h	Steps	Annealing 24h/168h
Winbond	W29N01GVSIAA	No Failure up to 50kRad(Si)	Complete	50 kRad(Si)	Complete	No Failure up to 50kRad(Si)	Complete	No Failure up to 50kRad(Si)	Complete	No Failure up to 50kRad(Si)	Complete
Spansion	S34ML04G200TFI00	No Failure up to 100kRad(Si)	Complete	No Failure up to 100kRad(Si)	Complete	100 kRad(Si)	No Recovery	100 kRad(Si)	No Recovery	50 kRad(Si)	No Recovery
Hynix	H27U4G8F2D	No Failure up to 100kRad(Si)	Complete	No Failure up to 100kRad(Si)	Complete	No Failure up to 100kRad(Si)	Complete	100 kRad(Si)	Partial	100 kRad(Si)	No Recovery

Parameter : Operating Current. Program : ICC2
Test conditions :
Unit : A
Spec Limit Max : 35.0E-03
Spec limits are represented in bold lines on the graphic.



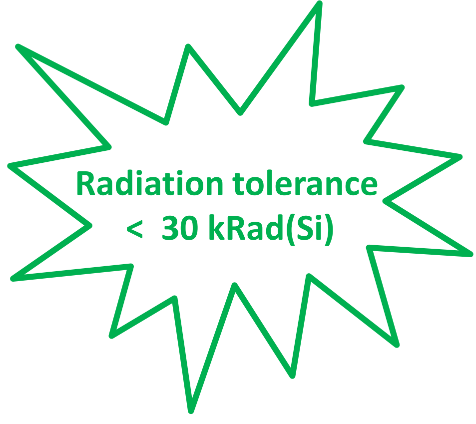
Parameter : SLC-March : Func_SLC_March
Test conditions : Erase memory Write . Read with SLC March Algorithm Block#0
Unit : Pass/Fail
No spec limit specified.



Examples: Winbond ICC and SLC_March functional test

In situ: HDC selected references results

Toshiba
TC58NVG2S0HTAI0
SLC Nand Flash Memory
4 GB / 512M x 8BIT 8 bit ECC/512 bytes
1509
TSOP48 (12x20mm)



failed erase blocks (E) · failed program blocks (P) · failed blocks (E+P)

step1 21krads · step2 22krads · step3 21krads · annealing1 25°C 24h · annealing2 100°C 168h

hours

Dut0, High duty cycle, erase/program, pattern 0xaa, block 1 to 1023

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blocks with minimum 1 byte in error · blocks with 90% bytes in error

step1 21krads · step2 22krads · step3 21krads · annealing1 25°C 24h · annealing2 100°C 168h

hours

Dut0, High duty cycle, Read, pattern 0xaa, block 1 to 1023

hirex eng.

blocks with minimum 1 byte in error · blocks with 90% bytes in error

step1 21krads · step2 22krads · step3 21krads · annealing1 25°C 24h · annealing2 100°C 168h

hours

Dut0, High duty cycle, Read, pattern 0xaa, block 1024 to 2047

hirex eng.

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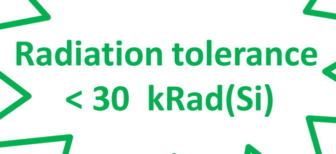
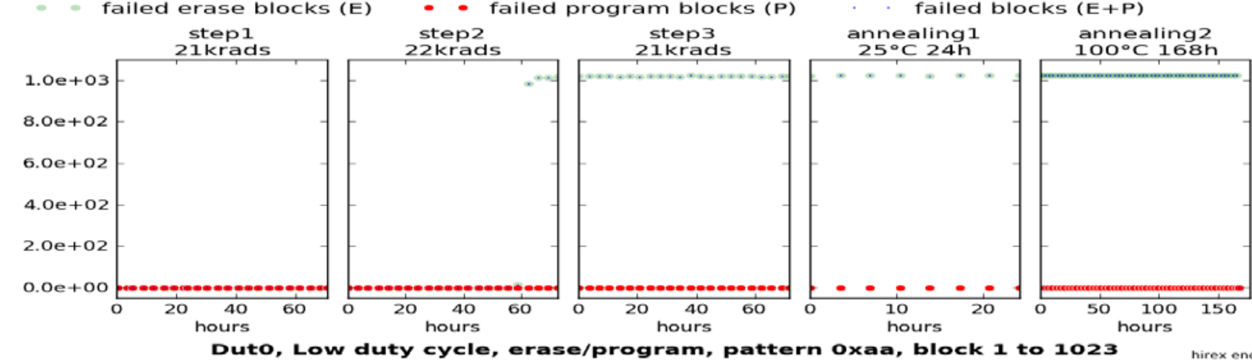
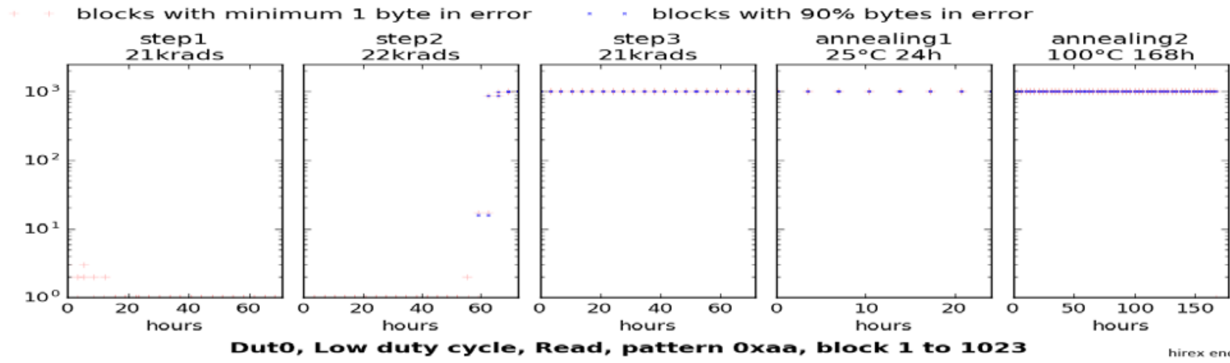
In situ: LDC selected references results

Toshiba
TC58NVG2S0HTAI0
SLC Nand Flash Memory
4 GB / 512M x 8BIT 8 bit ECC/512 bytes
1509
TSOP48 (12x20mm)







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In situ: HDC selected references results

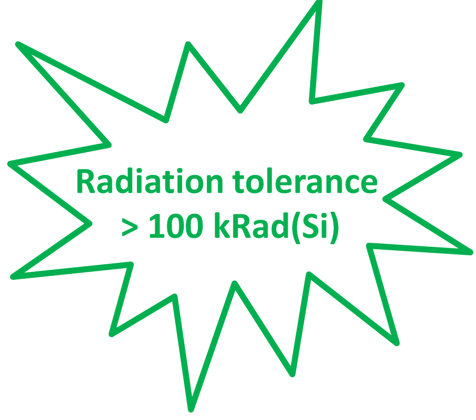
MX30LF4G18AC

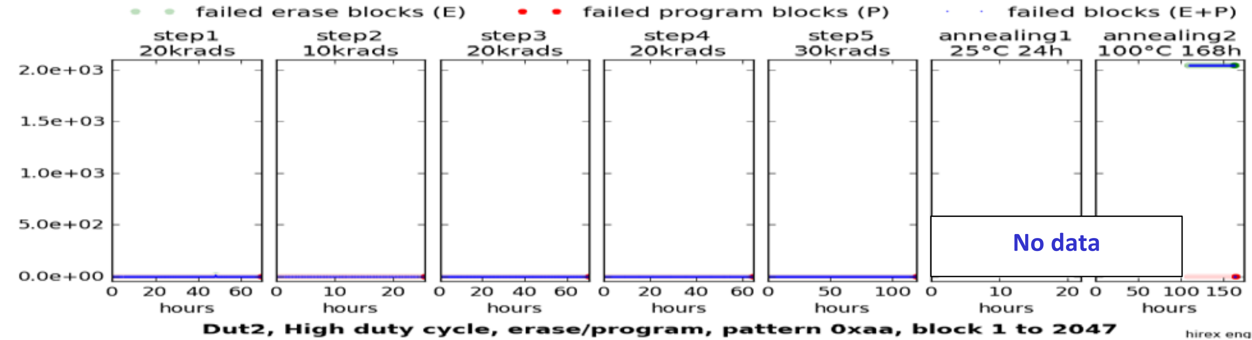
SLC Nand Flash Memory

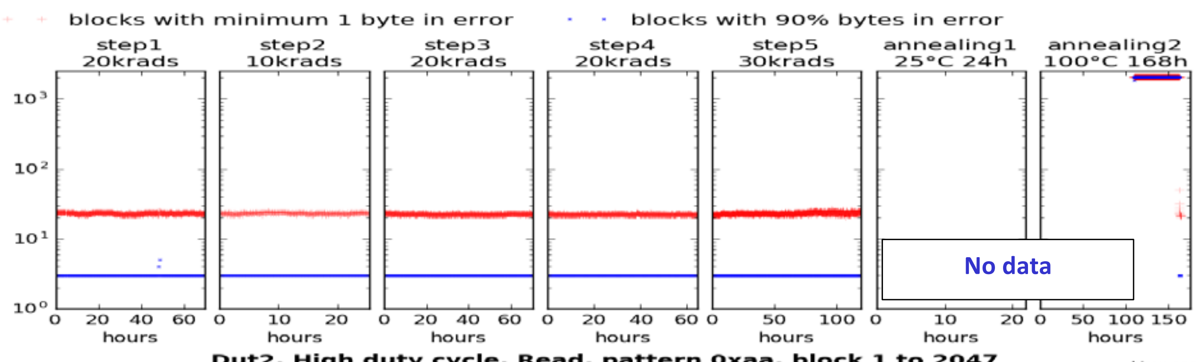
4 GB / 512M x 8 BIT
4 bit ECC

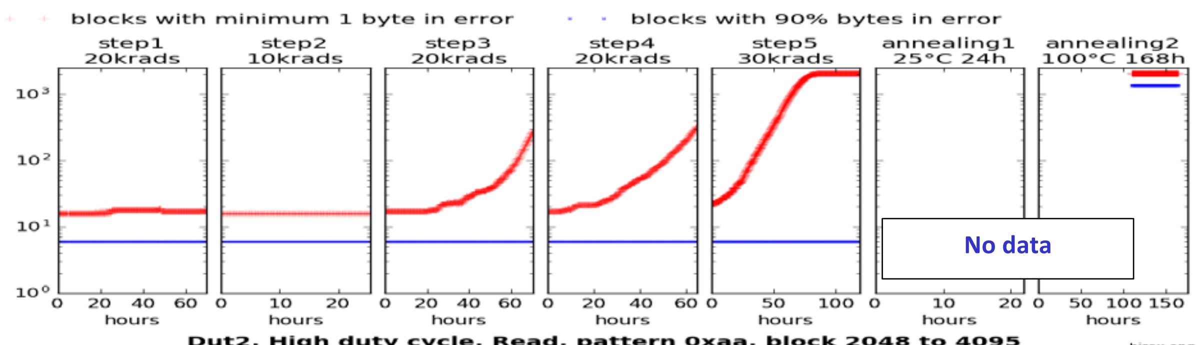
1444

TSOP48 (12x20mm)









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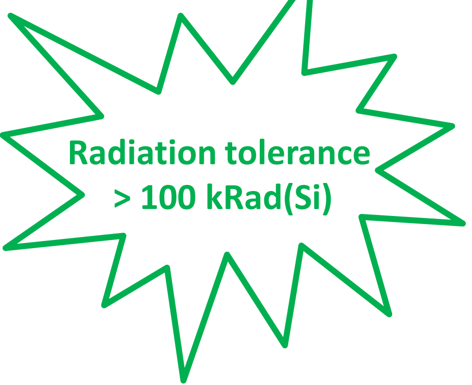
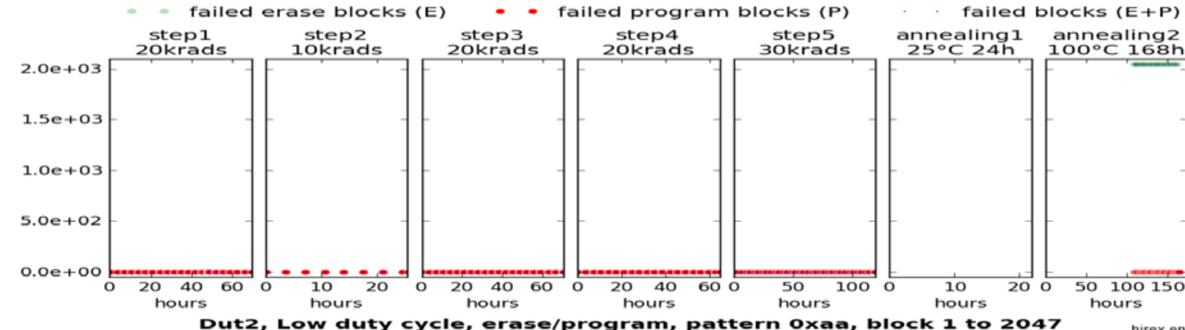
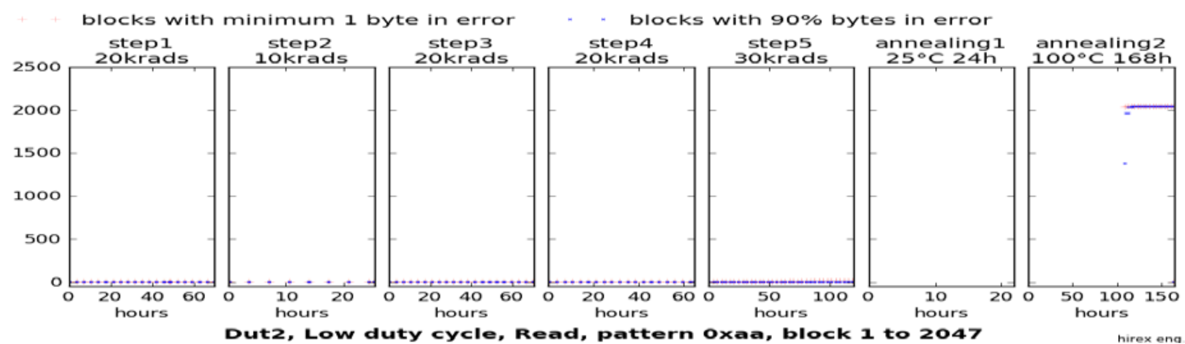
In situ: LDC selected references results

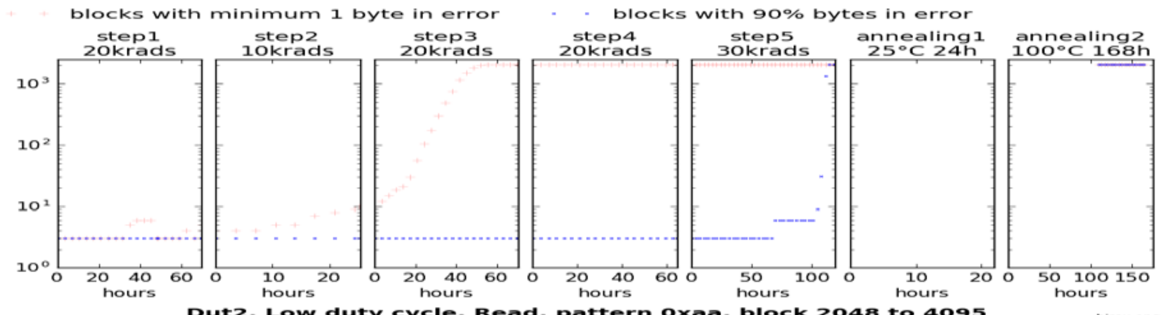
No data

Macronix
MX30LF4G18AC
SLC Nand Flash Memory
4 GB / 512M x 8 BIT 4 bit ECC
1444
TSOP48 (12x20mm)









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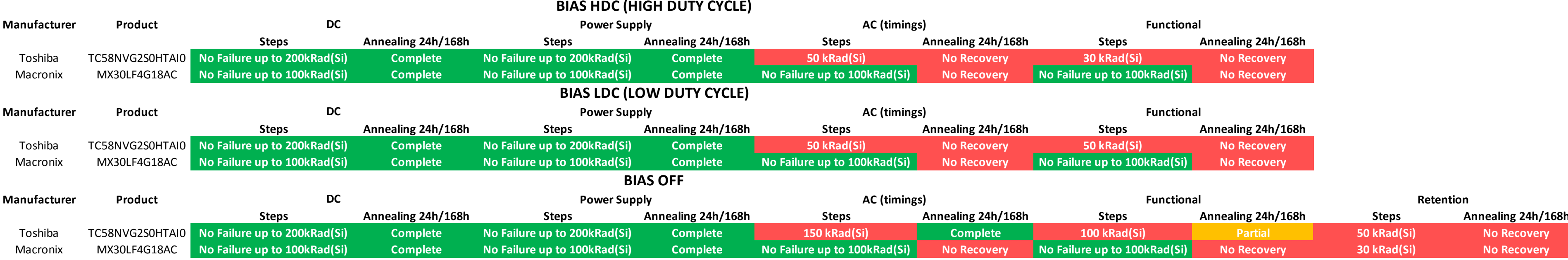
ATE: HDC and LDC selected references results



BIAS HDC (HIGH DUTY CYCLE)

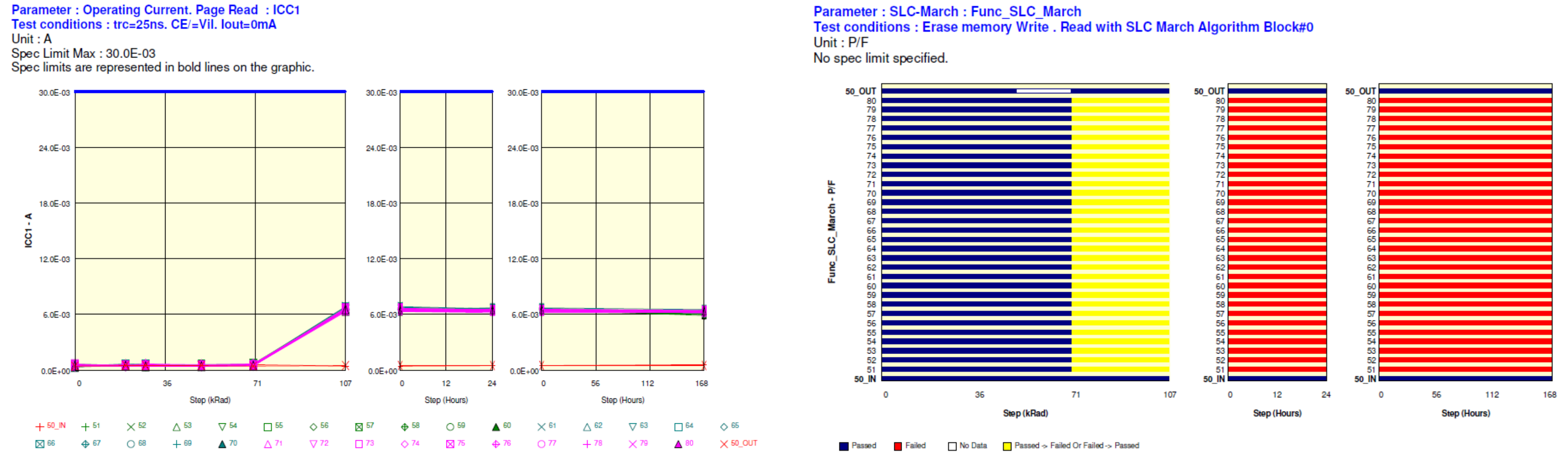
Manufacturer	Product	DC Steps	DC Annealing 24h/168h	Power Supply Steps	Power Supply Annealing 24h/168h	AC (timings) Steps	AC (timings) Annealing 24h/168h	Functional Steps	Functional Annealing 24h/168h
Toshiba	TC58NVG2S0HTAI0	No Failure up to 200kRad(Si)	Complete	No Failure up to 200kRad(Si)	Complete	50 kRad(Si)	No Recovery	30 kRad(Si)	No Recovery
Macronix	MX30LF4G18AC	No Failure up to 100kRad(Si)	Complete	No Failure up to 100kRad(Si)	Complete	No Failure up to 100kRad(Si)	No Recovery	No Failure up to 100kRad(Si)	No Recovery

BIAS LDC (LOW DUTY CYCLE)

Manufacturer	Product	DC Steps	DC Annealing 24h/168h	Power Supply Steps	Power Supply Annealing 24h/168h	AC (timings) Steps	AC (timings) Annealing 24h/168h	Functional Steps	Functional Annealing 24h/168h
Toshiba	TC58NVG2S0HTAI0	No Failure up to 200kRad(Si)	Complete	No Failure up to 200kRad(Si)	Complete	50 kRad(Si)	No Recovery	50 kRad(Si)	No Recovery
Macronix	MX30LF4G18AC	No Failure up to 100kRad(Si)	Complete	No Failure up to 100kRad(Si)	Complete	No Failure up to 100kRad(Si)	No Recovery	No Failure up to 100kRad(Si)	No Recovery

BIAS OFF

Manufacturer	Product	DC Steps	DC Annealing 24h/168h	Power Supply Steps	Power Supply Annealing 24h/168h	AC (timings) Steps	AC (timings) Annealing 24h/168h	Functional Steps	Functional Annealing 24h/168h	Retention Steps	Retention Annealing 24h/168h
Toshiba	TC58NVG2S0HTAI0	No Failure up to 200kRad(Si)	Complete	No Failure up to 200kRad(Si)	Complete	150 kRad(Si)	Complete	100 kRad(Si)	Partial	50 kRad(Si)	No Recovery
Macronix	MX30LF4G18AC	No Failure up to 100kRad(Si)	Complete	No Failure up to 100kRad(Si)	Complete	No Failure up to 100kRad(Si)	No Recovery	No Failure up to 100kRad(Si)	No Recovery	30 kRad(Si)	No Recovery



Examples: Macronix ICC and SLC_March functional test

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Lessons Learning forces for further investigations

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Lessons Learning forces For further investigations

- We have observed that after a certain cumulated dose rate (#100 kRad(Si), the power reset (ON/OFF) has an **influence on the device functionality (MACRONIX)**.
- This phenomenon is detected during the continuous BIAS current monitoring along the irradiation and annealing steps.

3V3 current (A)

step1 20krads | step2 10krads | step3 20krads | step4 20krads | step5 30krads | annealing1 25°C 24h | annealing2 100°C 168h

hours

High duty cycle, 3V3 board supply current

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failed erase blocks (E) | failed program blocks (P) | failed blocks (E+P)

step1 20krads | step2 10krads | step3 20krads | step4 20krads | step5 30krads | annealing1 25°C 24h | annealing2 100°C 168h

No data

hours

Dut0, High duty cycle, erase/program, pattern 0xaa, block 1 to 2047

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2nd irradiation campaign description

- Performed on MACRONIX selected part for heavy ion test.
  - 20 additional parts have been irradiated.
    - 10 parts using HDC (High Duty Cycle) bias.
    - 10 parts using LDC (Low Duty Cycle) bias.
  - No Power ON/OFF.
  - 1 single irradiation step followed by 24h @ 25°C and 168h @ 100°C:
    - From 0 kRad(Si) up to 150 kRad(Si) for the MACRONIX parts.
  - A cycle of READ/WRITE will be performed at each “virtual irradiation” steps (each 20 kRad(Si).
  - Electrical measurements performed at the end of the irradiation steps and after each annealing.

Campaign									
Macronix - 2ème essai									
Step	Dose Rate (Rad/H)	Dose (Rad(Si))	Start Date		End Date		Total Dose	Step	Comment
#1	-	-	Jeudi	02/02/2017 16:00	Jeudi	02/02/2017 16:00	-	Init	Installation
#2	300	20100	Jeudi	02/02/2017 16:00	Dimanche	05/02/2017 11:00	20100	R/W	
#3	300	21600	Dimanche	05/02/2017 11:00	Mercredi	08/02/2017 11:00	41700	R/W	
#4	300	21600	Mercredi	08/02/2017 11:00	Samedi	11/02/2017 11:00	63300	R/W	
#5	300	21600	Samedi	11/02/2017 11:00	Mardi	14/02/2017 11:00	84900	R/W	
#6	300	21600	Mardi	14/02/2017 11:00	Vendredi	17/02/2017 11:00	106500	R/W	
#7	300	21600	Vendredi	17/02/2017 11:00	lundi	20/02/2017 11:00	128100	R/W	
#8	300	22500	Lundi	20/02/2017 11:00	Jeudi	23/02/2017 14:00	150600	150K	Out for Annealing
#9	24	-	Jeudi	23/02/2017 16:00	Vendredi	24/02/2017 16:00	Room/24H	24H	
#10	166	-	Vendredi	24/02/2017 18:00	Vendredi	03/03/2017 16:00	100°C/168H	168H	End RVT

Macronix 2nd TID campaign

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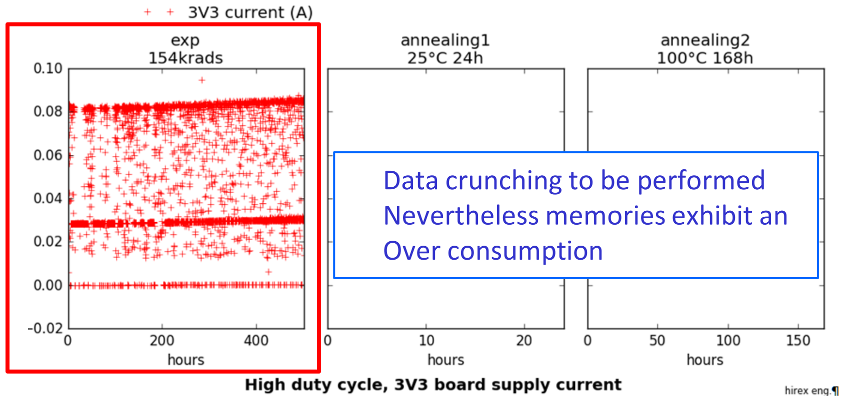
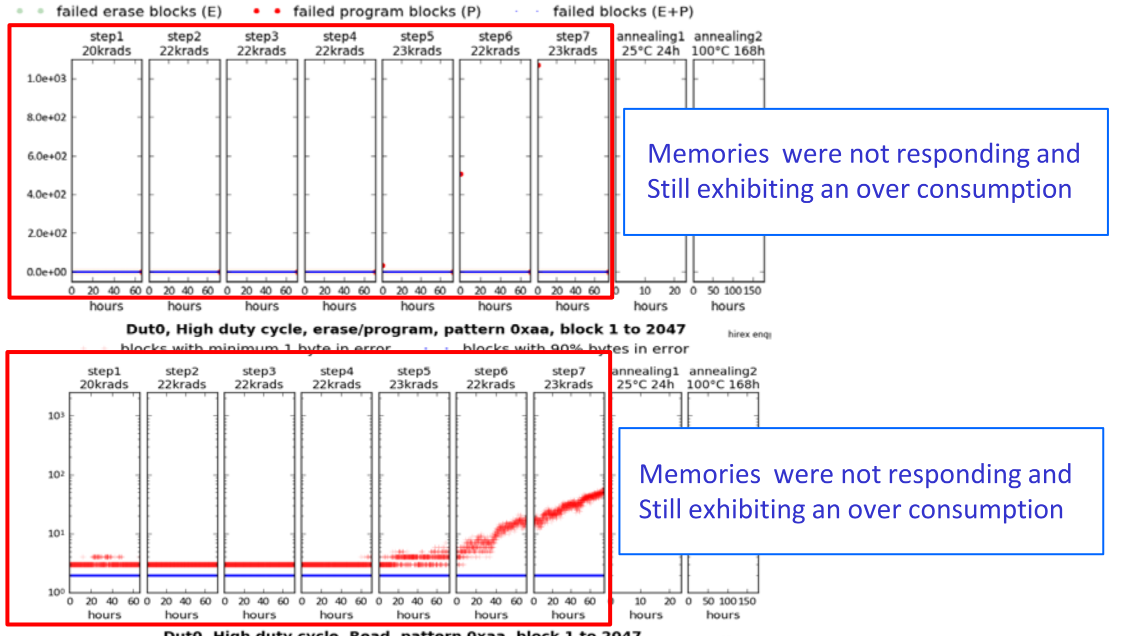
2nd irradiation campaign HDC results

Erase/Program Read pattern :





- Without power ON/OFF memories are functional up to 150 kRad(Si).
- Still exhibiting an over consumption after the POWER OFF.
- After POWER OFF same phenomenon, memories are not responding.
- 168h are not enough to allow memories to recover.
- Few memory errors occur around 100 kRad(Si).
- Less than 100 blocks are concerned with these memory errors at 150 Krad(Si)

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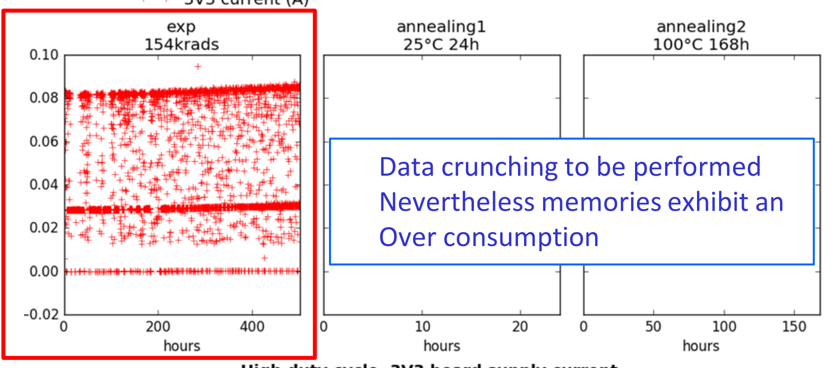
2nd irradiation campaign HDC results

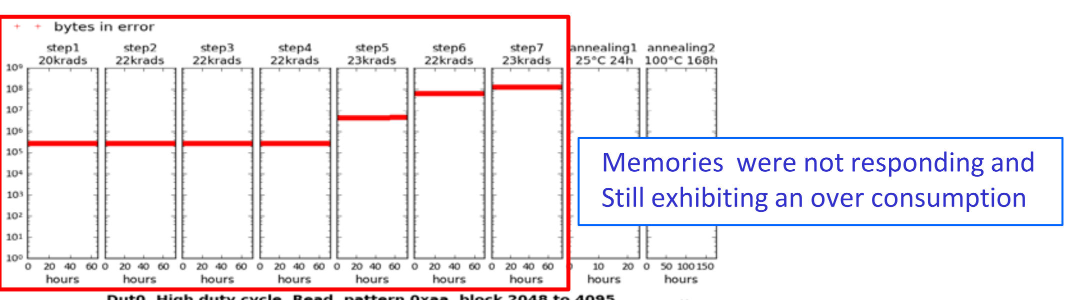
Read pattern :



Data crunching to be performed
Nevertheless memories exhibit an
Over consumption

blocks with minimum 1 byte in error · blocks with 90% bytes in error
step1 20krads · step2 22krads · step3 22krads · step4 22krads · step5 23krads · step6 22krads · step7 23krads · annealing1 25°C 24h · annealing2 100°C 168h
Dut0, High duty cycle, Read, pattern 0xaa, block 2048 to 4095

Memories were not responding and
Still exhibiting an over consumption



Memories were not responding and
Still exhibiting an over consumption

- Without power ON/OFF memories are functional up to 150 kRad(Si).
- Up to 86 krad(Si) no major block errors at 90%.
- From 86 kRad(Si) up to 109 kRad(Si) less than 50 block errors at 90%.
- From 109 kRad(Si) up to 154 kRad(Si) less than 600 block errors at 90%.
- WRITE sequence after each 20 kRad(Si) allows to partially heal the memory errors.
- Still exhibiting an over consumption after the POWER OFF.
- After POWER OFF same phenomenon, memories are not responding.
- 168h are not enough to allow memories to recover.

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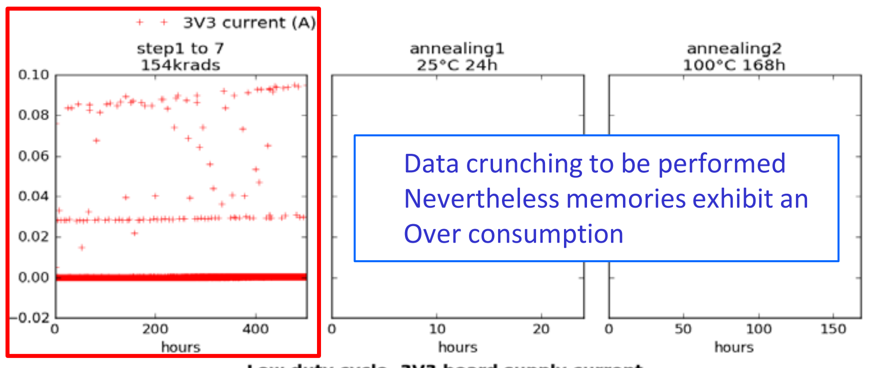
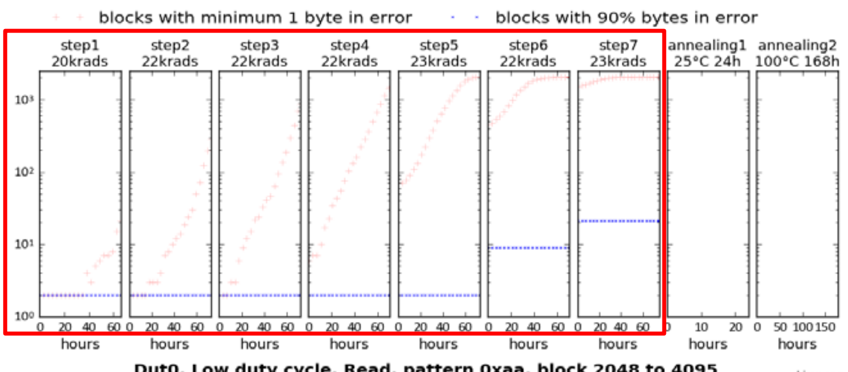
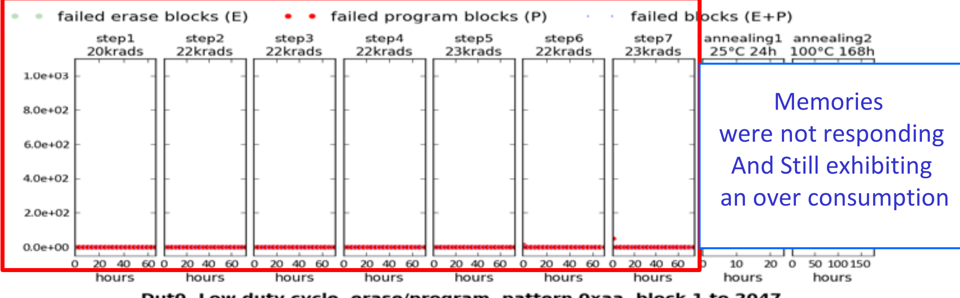
2nd irradiation campaign LDC results

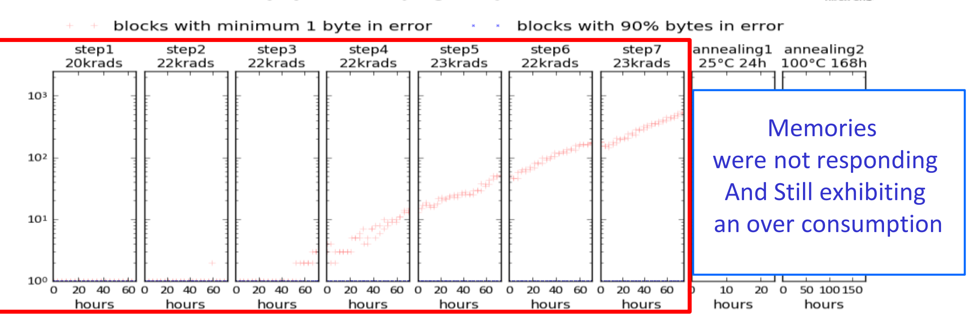
Erase/Program Read pattern :

Read pattern :









Erase/Program Read pattern :

- Without power ON/OFF memories are functional up to 150 kRad(Si).
- Still exhibiting an over consumption after the POWER OFF.
- After POWER OFF same phenomenon, memories are not responding.
- 168h are not enough to allow memories to recover.
- Memory block errors occur around 86 kRad(Si).
- Less than 600 blocks are concerned with these memory errors at 150 Krad(Si)

Read pattern :

- Same behavior as the HDC Read pattern but with much less block errors (150 kRad(Si) → less than 10 blocks in error at 90%.

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Conclusions

- Despite the fact that technologies are similar, radiation tolerance across the 5 selected NAND FLASH is different.
- Charge pump block seems to be the critical element for all the memories except MACRONIX as it's involved in ERASE/PROGRAM operation.
- One out of the 5 selected devices seems suitable for JUICE mission (MACRONIX) at least for Total dose radiation.
- POWER ON/OFF has an impact on total dose radiation tolerance.
- Much less memory errors when ERASE/PROGRAM cycles are implemented periodically compare to the READ only test sequence.
- For the READ only test, number of errors is related to number of reads (more reads, more errors)

Proposed Next Steps

- For MACRONIX device extend the 168h @ 100°C annealing to check if memory reach a complete recovery.
- After partial or complete recovery, read memory erroneous bytes and check the number of bits in error per byte to verify how much ECC is able to correct erroneous data.
- Perform a failure analysis to understand if the over consumption issue is related to a specific element/area or if it's spread across the full die.

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Backup Slides

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Company Overview

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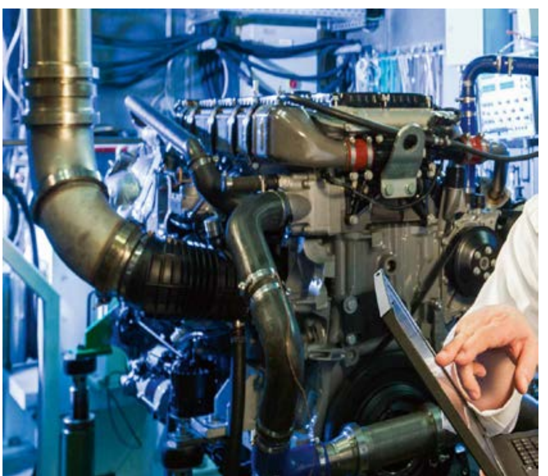
TÜV NORD Group main areas

ENERGY

IT



MOBILITY

HEALTH AND NUTRITION

NATURAL RESOURCES

AEROSPACE & ELECTRONIC

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Aerospace & Electronic Business Unit

Alter technology group: with **30** years experience in the sector.

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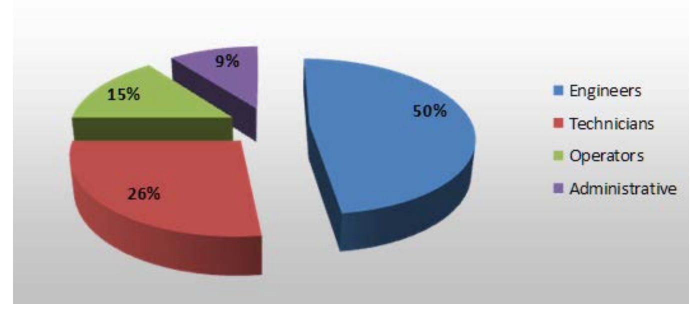
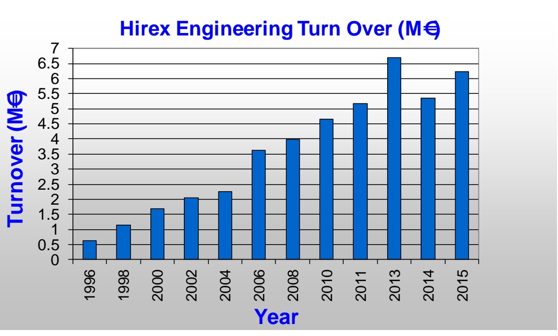
Hirex Profile

- Hirex Engineering founded in January 1993.
- Hirex Engineering joined ALTER Technology Group in January 2007.
  - ATN based in Madrid, Seville, Roma, Portsmouth and Shanghai.
  - ATN employees 230 as of today.
  - ATN Turn-over 65 M€.
- 100% Privately owned by TÜV NORD since 29th June 2011.
- Hirex Engineering :
  - Based in Toulouse.
  - 48 employees as of today.
  - 1800 m² Facility.
  - Certified ISO 9001, EN 9100 and ISO 14001.





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Expertise & Activities

3 labs for a focused organization:

- SEE: Radiation lab.
- LAT: Semiconductor Technology lab.
- LTE: Electrical & environmental test lab

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