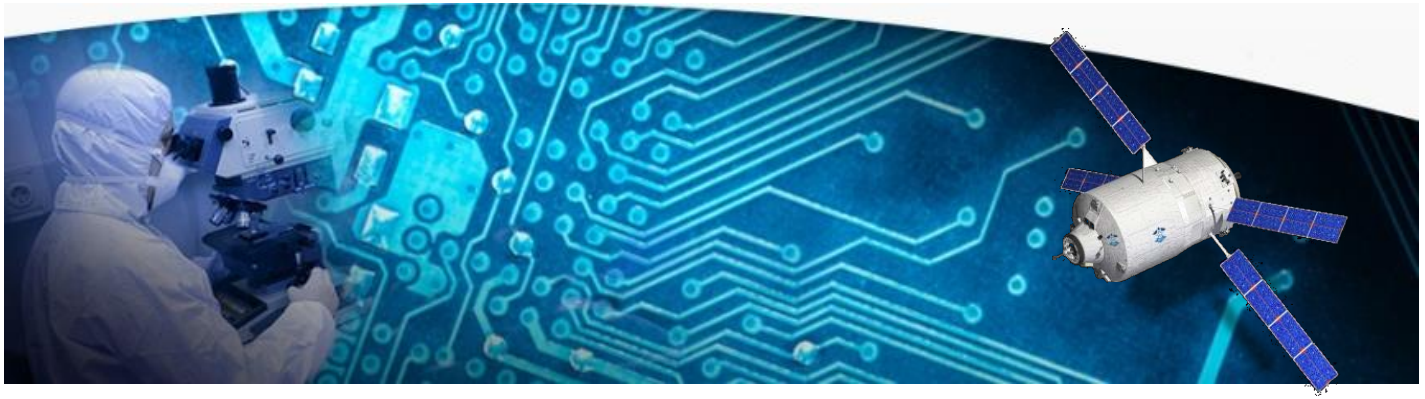


Test methods for SEE evaluations of ADCs and DACs

ESA-CNES Radiation Final Presentation Days on Space Environments and Radiation Effects on EEE components

ESTEC contract- No4000105495/12/NL/SFe

Main objective:

- Evaluate 3 ADCs and 1DAC as candidates for space applications
- Compare different test methods for SEE testing

Parts Selection and criteria

- **Key drivers for converter selection:**
  - ADC128S102 and RHF1401 required in the study
  - 16 bits ADC or higher resolution
  - Space quality level availability

- **Parts selection has been performed according to the following criteria :**
  - Selection of different A/D converter architectures.

reference	Manufacturer	type	Resolution	Sampling frequency	Comment	Architecture
AD976A	Analog Devices	A/D	16-bit	200kSPS	BICMOS	Successive approximation, switched capacitor
ADC128S102	Texas Instruments	A/D	12-bit	50kSPS to 1MSPS	8 Channel	Successive approximation, switched capacitor
RHF1401	STMicroelectronics	A/D	14-bit	20MSPS	Rad-hard	Pipelined
ADS1278	Texas Instruments	A/D	24-bit	Up to 144kSPS	Octal simultaneous sampling	Delta Sigma
DAC5675A	Texas Instruments	D/A	14-bit	400MSPS	Class V	current-source-array

SEE Test methods

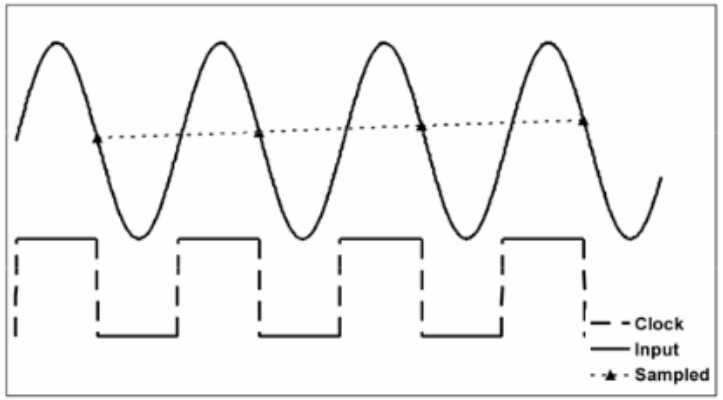
- ✓ **Beat Frequency**
- ✓ **4 Points (4P)**
- ✓ **“hirex”**

(1) : Enhancing Observability of Signal Composition and Error Signatures during SEE Analog to Digital Testing’ – M. Berg et Al, IEEE Transactions on Nuclear Science, Volume 57, Issue: 4

ADC: Beat frequency

- With the input frequency f_{in} set very close to the sampling frequency fs, the output code of the ADC is a slow moving digital sine wave, changing at a rate of 1 LSB per clock cycle.

$f_{in}=f_s/(2^N*PI)$ with N=A/D resolution



Trig condition:

|output at clk-1 – output at clk| > EB

EB= given Error Bound

Event record:

If event trig → 4096 points are recorded including pretrig points

ADC: 4 points (4P) test method

DUT sampling frequency being fixed, the selected frequency of the sinewave input is such that only 4 points of the sinewave input are converted continuously.

$$f_{in} = f_s/4$$

Trig condition:

|output at clk-4 – output at clk| > EB

Differs from 4P test method presented in (1) where each of the 4 points have its own EB

Pro:

- Same EB for any point
- No need of specific algorithm to recover from an upset in clocking system
- No need to record the DRY DUT signal

Con:

- Use of possibly larger margin in EB

Event record:

If event trig → 4096 points are recorded including pretrig points

(1) : Enhancing Observability of Signal Composition and Error Signatures during SEE Analog to Digital Testing' – M. Berg et Al, IEEE Transactions on Nuclear Science, Volume 57, Issue: 4

ADC: "hirex" test method

DUT sampling frequency being fixed, input frequency f_{in} is set to a much lower value than f_s with f_s a multiple of $f_{in,}$ leading to a significant number of points converted by sinewave input period (typically 100 to 2000 points)

$$f_{in} = f_s/m \text{ with } m \text{ integer}$$

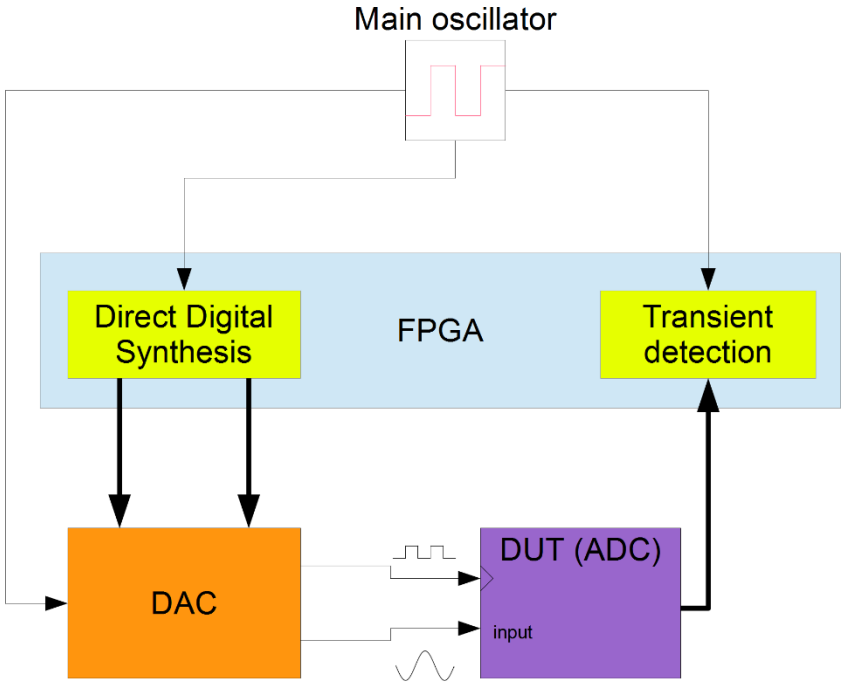
Trig condition:

|output at clk-m – output at clk| > EB

Event record:

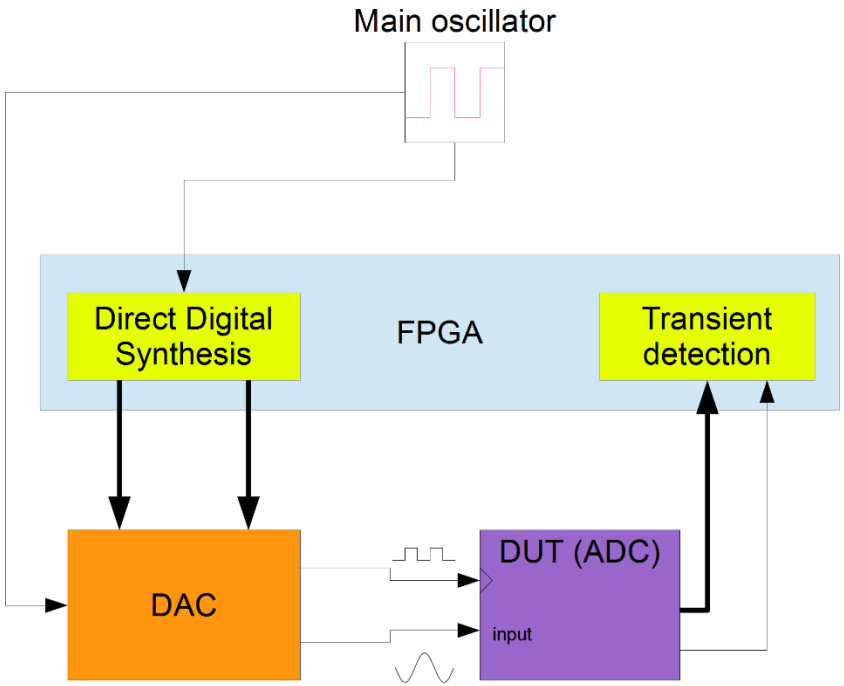
If event trig → 4096 points are recorded including pretrig points

ADC SETUP principle



DUT without Data ready signal

- ADS1278
- ADC128S102



DUT with Data ready signal

- AD976A
- RHF1401

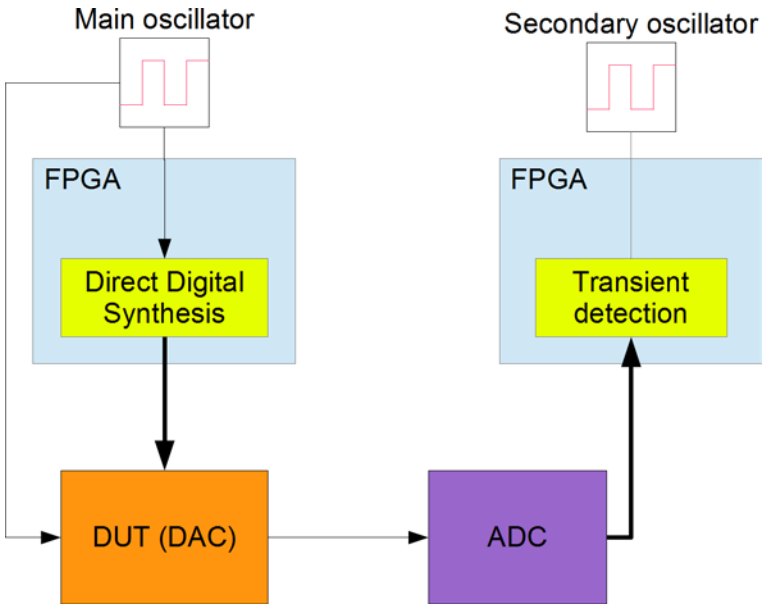
DAC test method

DAC output is chained with a 10-bit 400 MSPS Digitizer

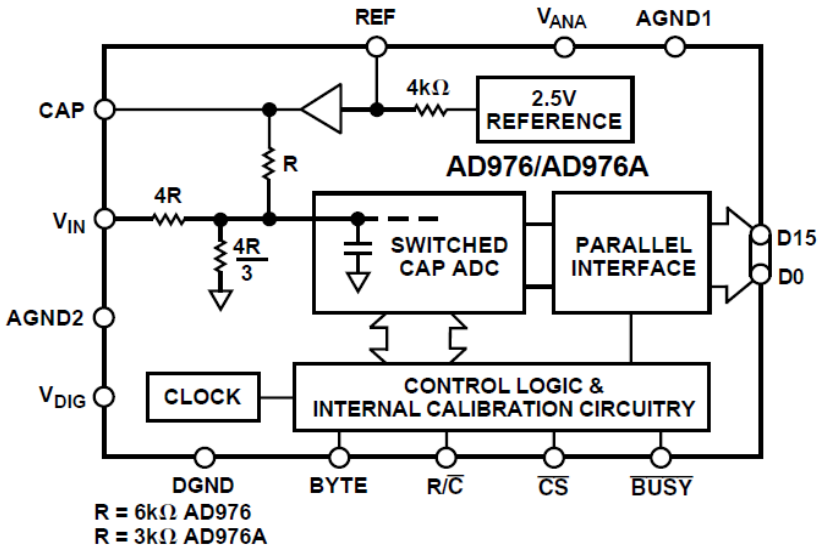
Trig condition: for 1MHz digital sinewave, 400 points are converted by the ADC digitizer

$$|\text{output at clock-400} - \text{output at clock}| > EB$$

Again, when 1 event is trigged, 4096 are recorded



AD976A



16-Bit, 200 kSPS, BiCMOS A/D

Vdig=5V, Vana=3V3, Vinmax=+/-5V

Internal reference, 2,2µF between REF and AGND

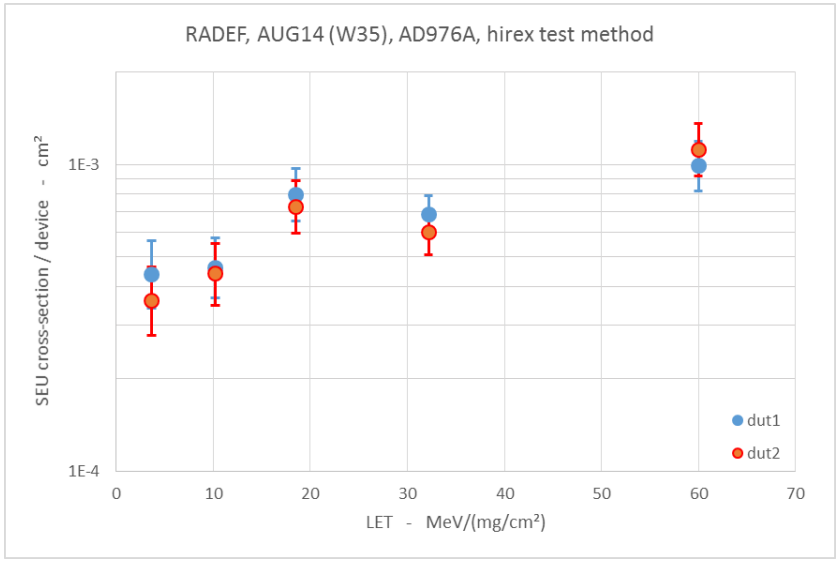
Conversion frequency=200 000 Hz

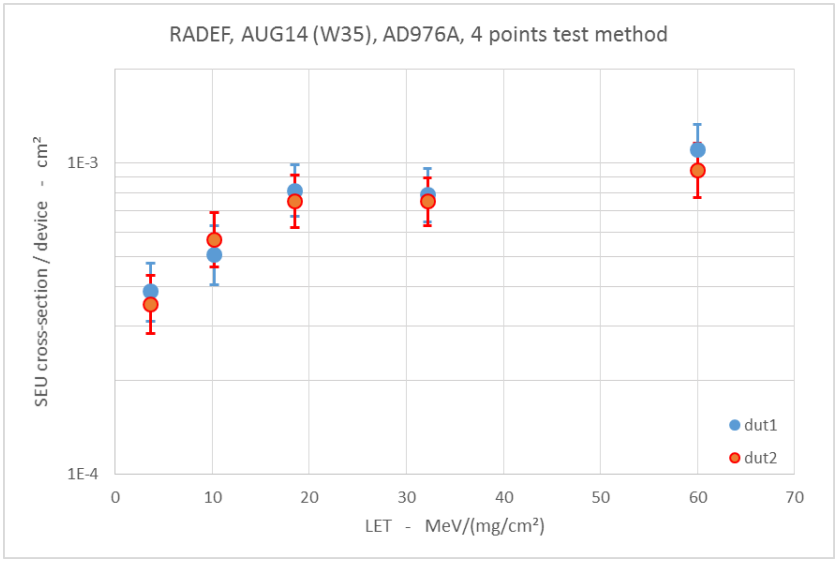
Input sine wave frequency

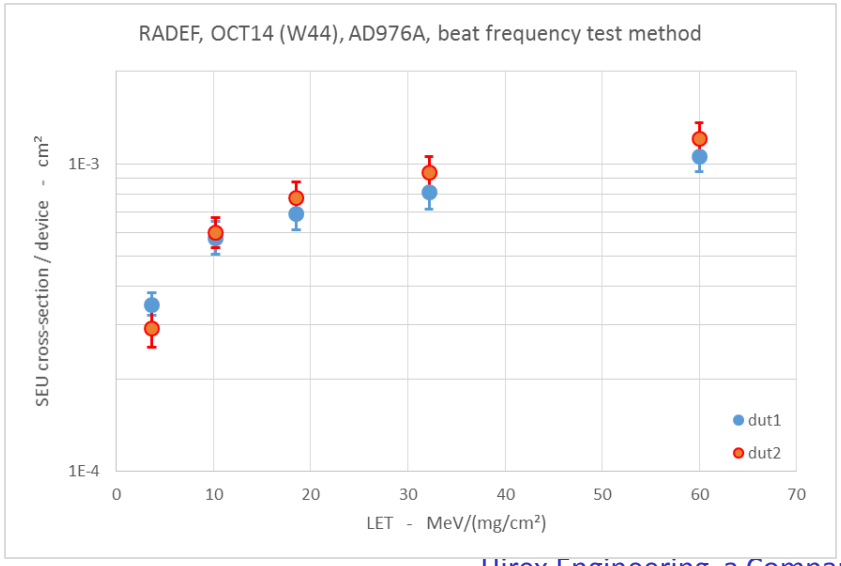
4P method	50 000 Hz
Beat frequency	199 999.03 Hz
Hirex	1 560 Hz (128 points/period)

- No latchup has been detected for any run with LETs up to 60MeV/(mg/cm²)
- No signal flattening nor SEFI
- Single conversion error for the 3 test methods (only 3 SETs with 2 successive conversion errors)
- Internal reference, but no large transients, can be explained by the 2.2µF capacitor at Vref pin with the 4k Ohms internal resistor at 2.5V reference block output.
- 2 false clock pulses in total for all the runs
- The three test methods allow for similar SET events cross-section plots.

AD976A

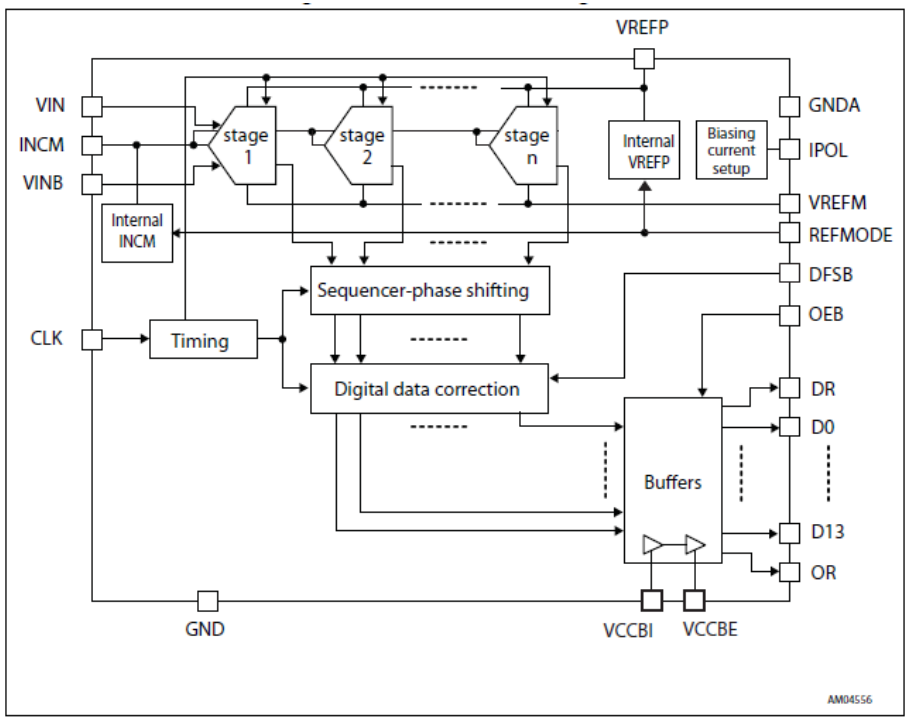






EB= 70 LSBs for the three methods

RHF1401



Rad-hard 14-bit 20 Msps A/D

DVCC=2.5V, AVCC=2.5V, VCCB=3.3V, VCCBI=2.5V

Internal reference

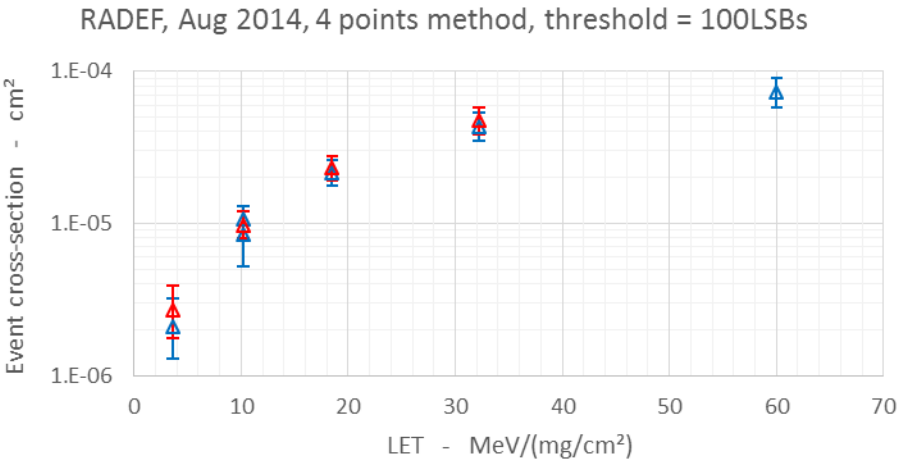
Conversion frequency=15 000 000 Hz

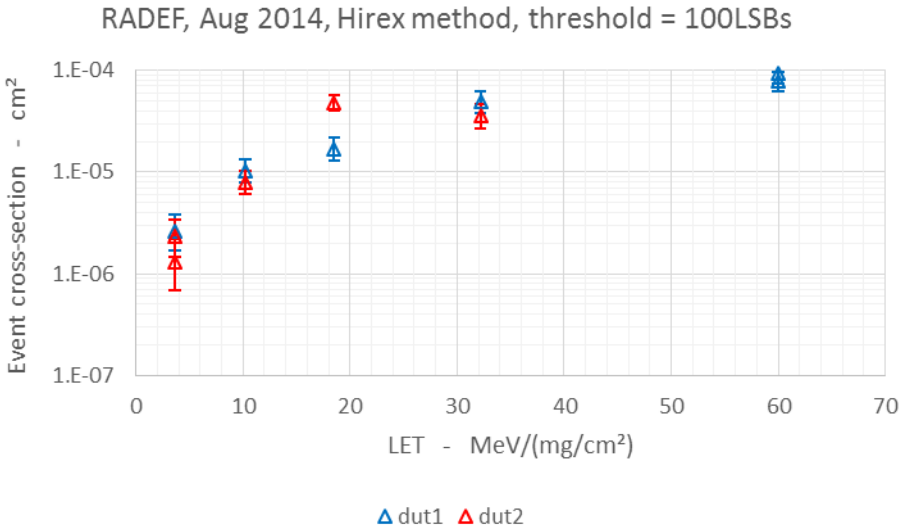
Input sine wave frequency

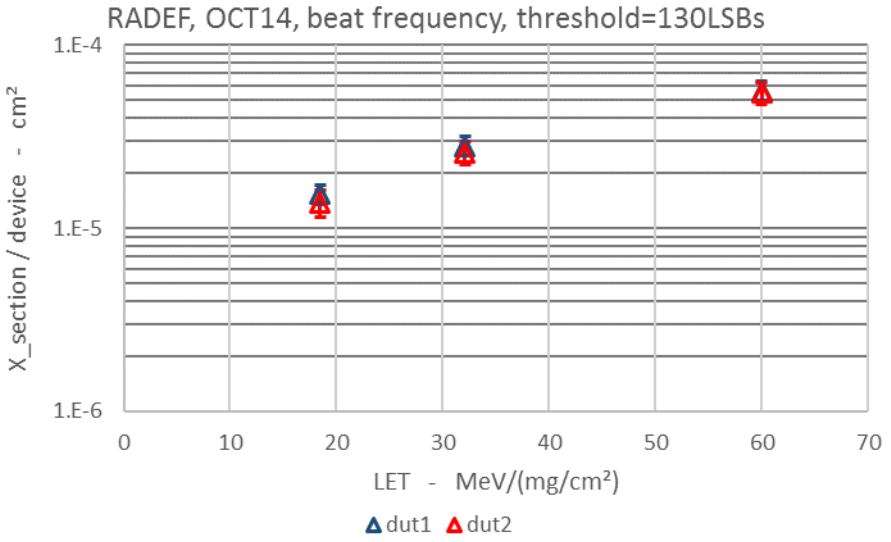
4P method	3 750 000 Hz
Beat frequency	~15 000 000 Hz
Hirex	15 000 Hz (1000 points/period)

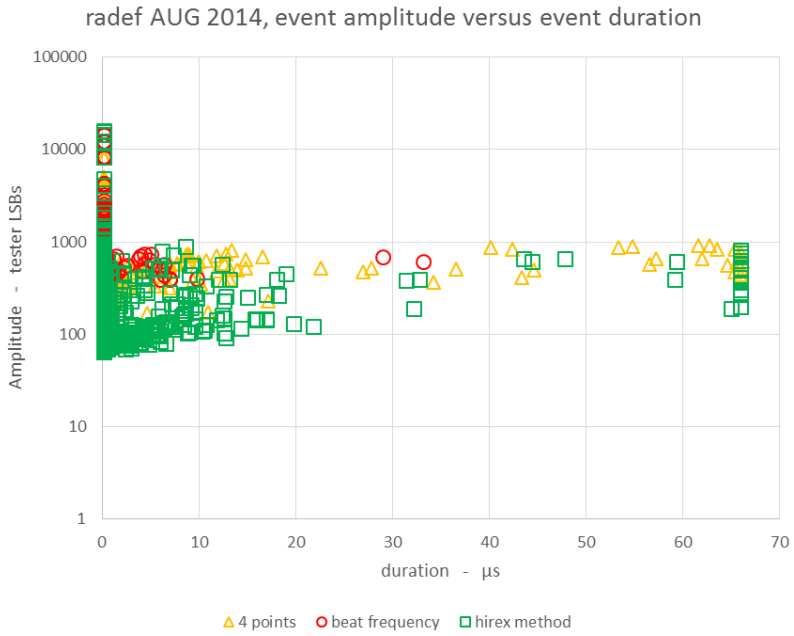
- No latchup has been detected for any run with LETs up to 60MeV/(mg/cm²)
- No flattening nor SEFI
- Single conversion error for the 3 test methods
- Burst events that can be attributed to DUT analog block (internal reference)
- Few false clock pulses in total for all the runs
- The three test methods allow for similar SET events cross-section plots.

RHF1401







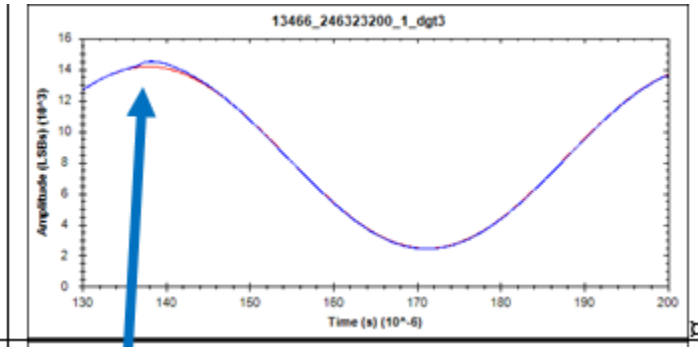


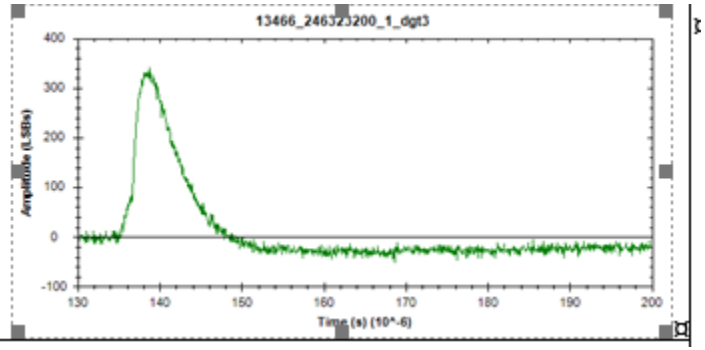
EB=100 LSBs for 4P and Hirex methods

130 LSBs for beat frequency

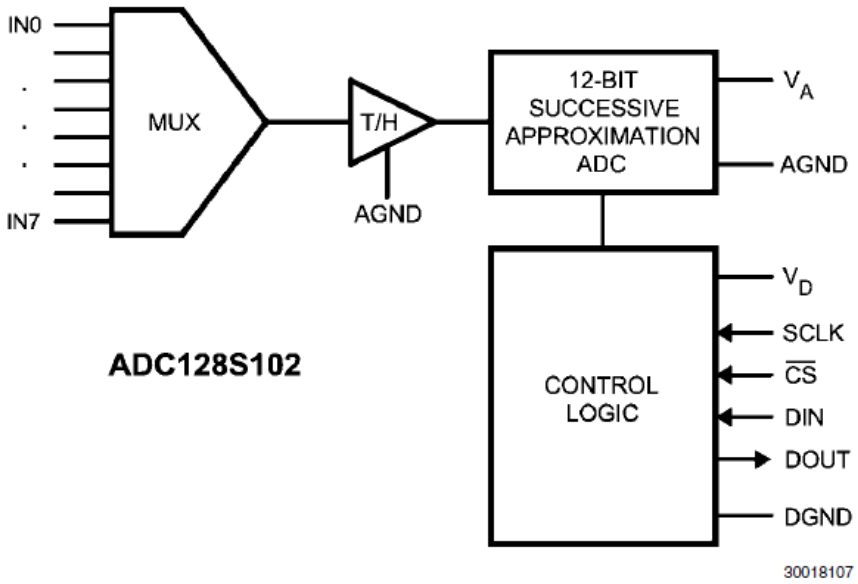
RHF1401

#8¶
RUN004-datestamp:-
13466.246323200¶
Hirex-method¶
→ Xenon¶
Amplitude:-390-tester-LSBs¶
Duration:-32.8-µs¶
¤





ADC128S102



ADC128S102

8-Channel, 50 kSPS to 1 MSPS, 12-Bit A/D

VD=5V, VA=5V, VINmax= +5V

External reference

Conversion frequency= 711 111 Hz

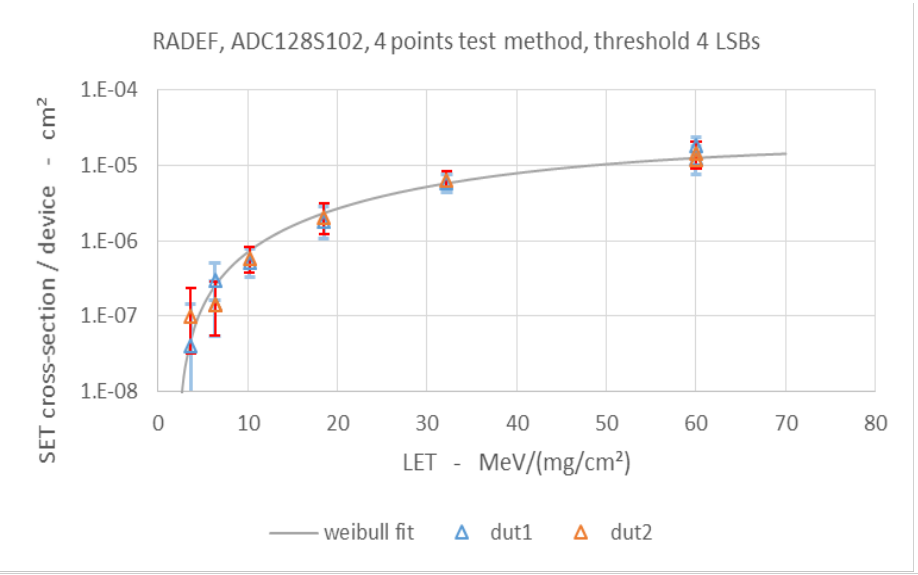
Input sine wave frequency

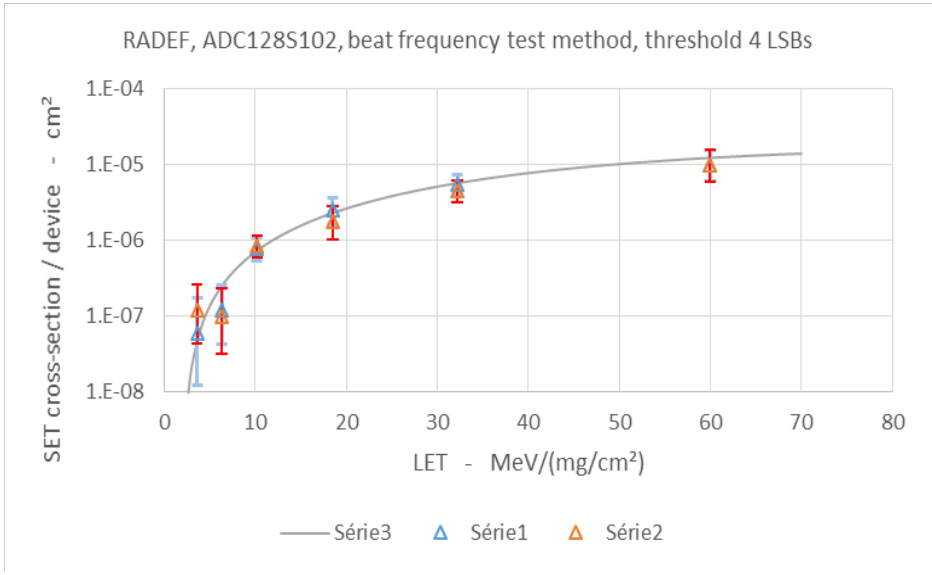
4P method	177 778 Hz
Beat frequency	711 055Hz
Hirex	711,1 Hz (1000points/period)

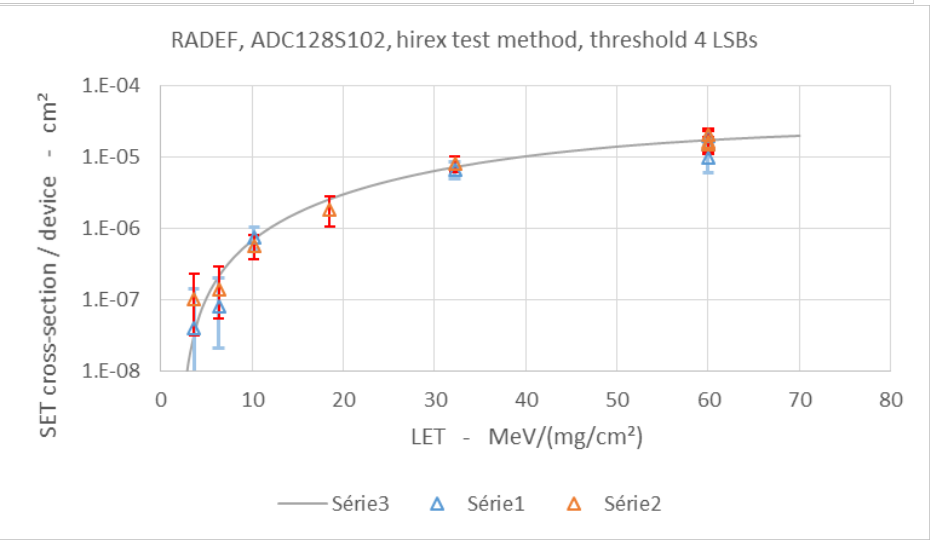
Only 1 channel is considered

- No latchup has been detected for any run with LETs up to 60MeV/(mg/cm²)
- No flattening nor SEFI
- Single conversion error for the 3 test methods
- No burst event (expected as external reference)
- No clock issue as expected
- The three test methods allow for similar SET events cross-section plots.

ADC128S102

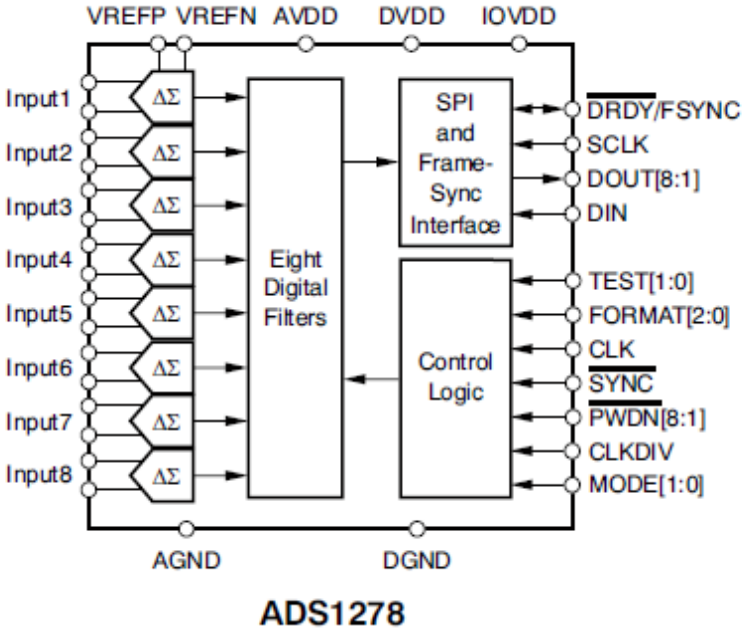






EB=4 LSBs for the 3 methods

ADS1278



ADS1278

Octal, Simultaneous Sampling, 24-Bit A/D
Tested as 16 bit ADC

DVDD=1.8V, AVDD=5V, IOVDDO=3.3V
VREFN= Ground, VREFP =2.048V

External reference

Conversion frequency= 144 000 Hz

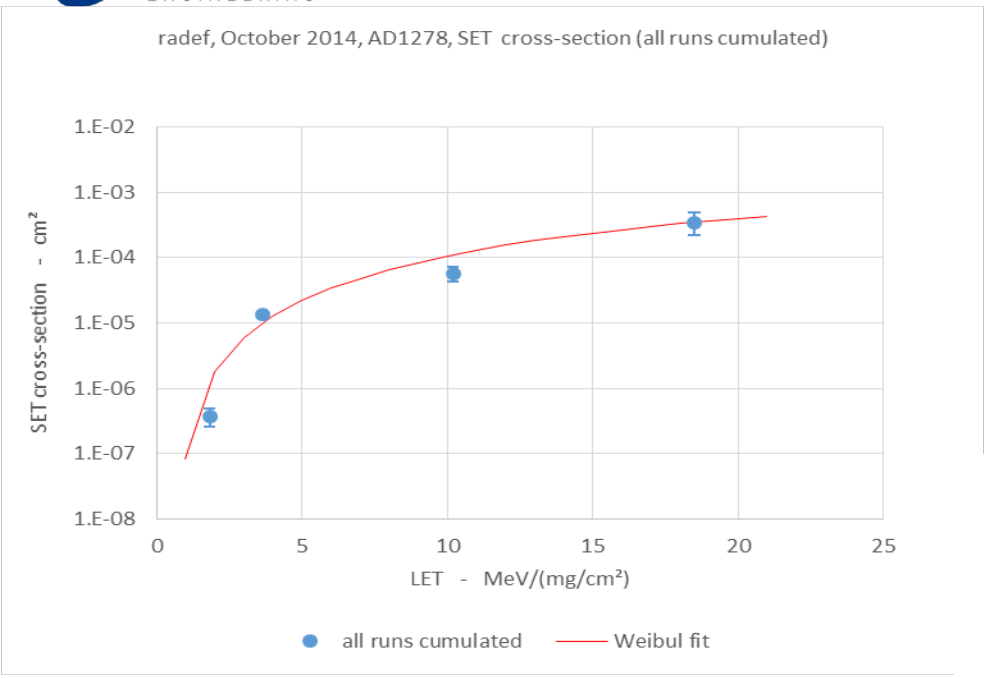
Input sine wave frequency

4P method	36 000 Hz
Beat frequency	143 998 Hz
Hirex	720 Hz (200 points / period)

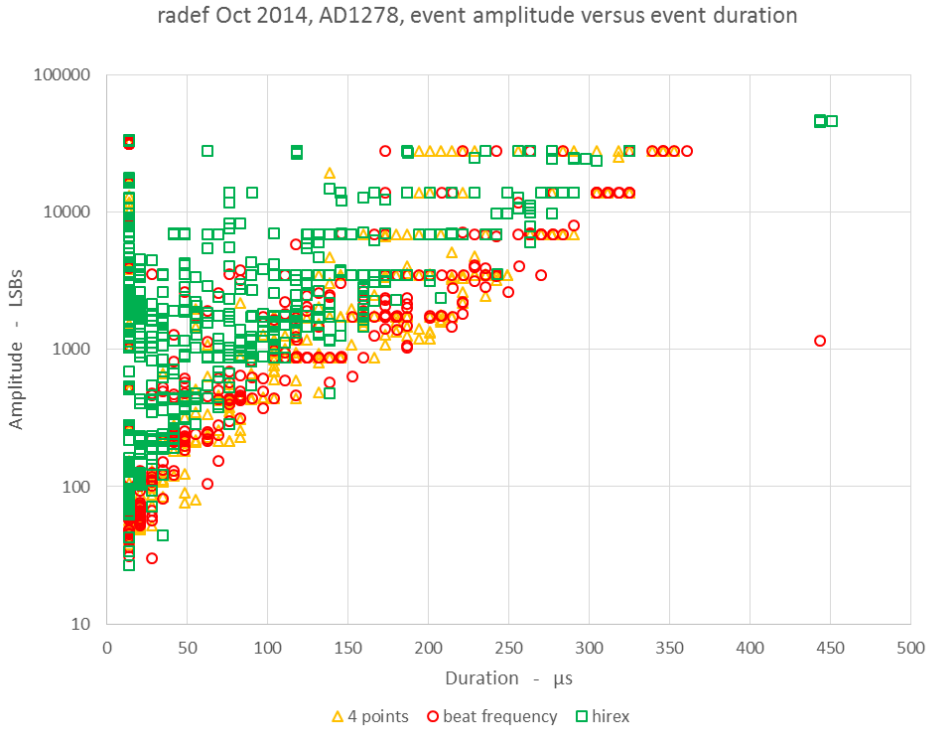
ONLY 1 A/D monitored

- SEL events have been observed with Argon (10.2 MeV/mg/cm²) and Iron (18.5 MeV/mg/cm²). Two of these SEL events were destructive.
- Flattening up to 4ms (4 events)
- Single conversion error and burst event for the 3 test methods
- No clock issue as expected
- The three test methods allow for similar SET events cross-section value for a given LET.

ADS1278

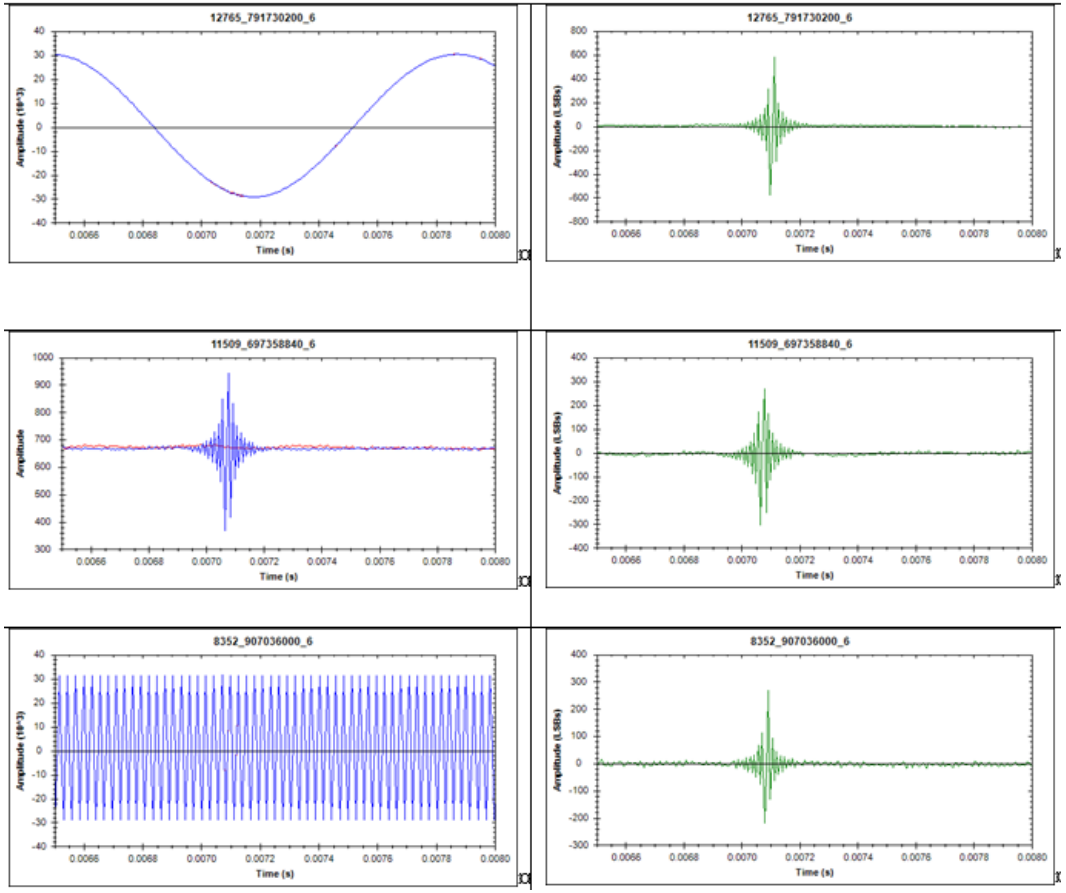


EB=70LSBs (monitored 16 bits)

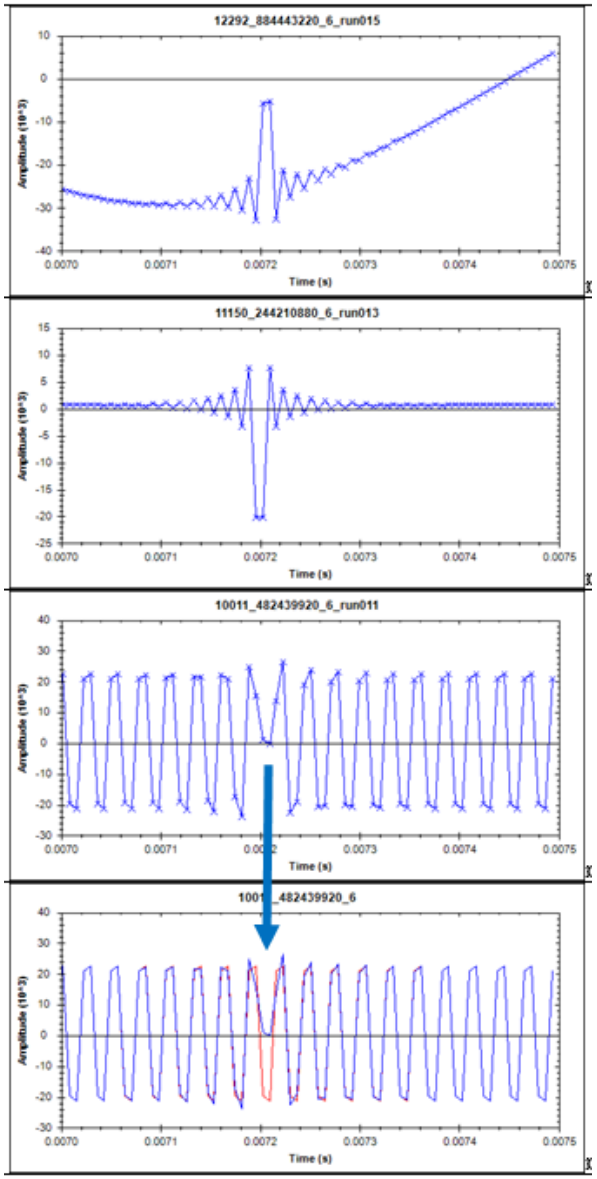


ADS1278

Small bursts



large bursts



Top: hirex
Middle: beat frequency
Bottom: 4P

DAC5675A

CLASS V, 14-BIT, 400-MSPS D/A

DVDD=3.3V, AVDD=3.3V

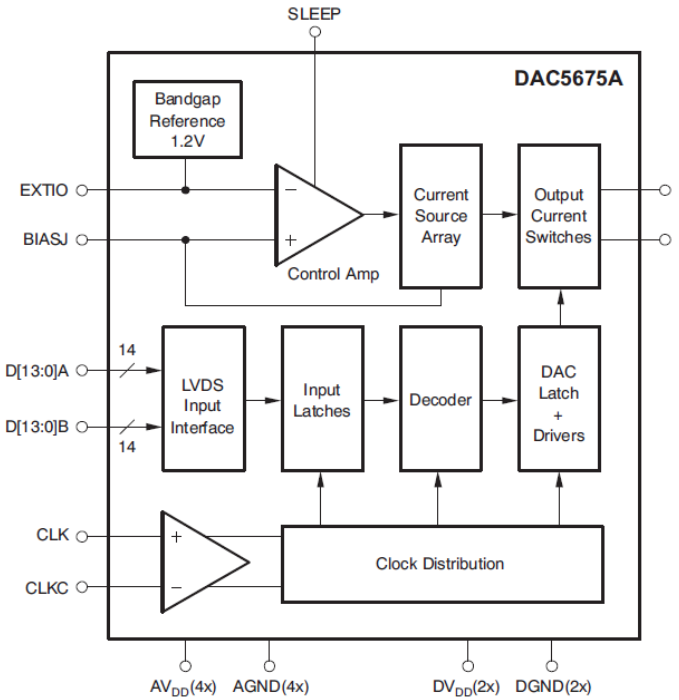
Internal reference

Clock =400 MHz

Digital Input sine wave frequency = 1MHz

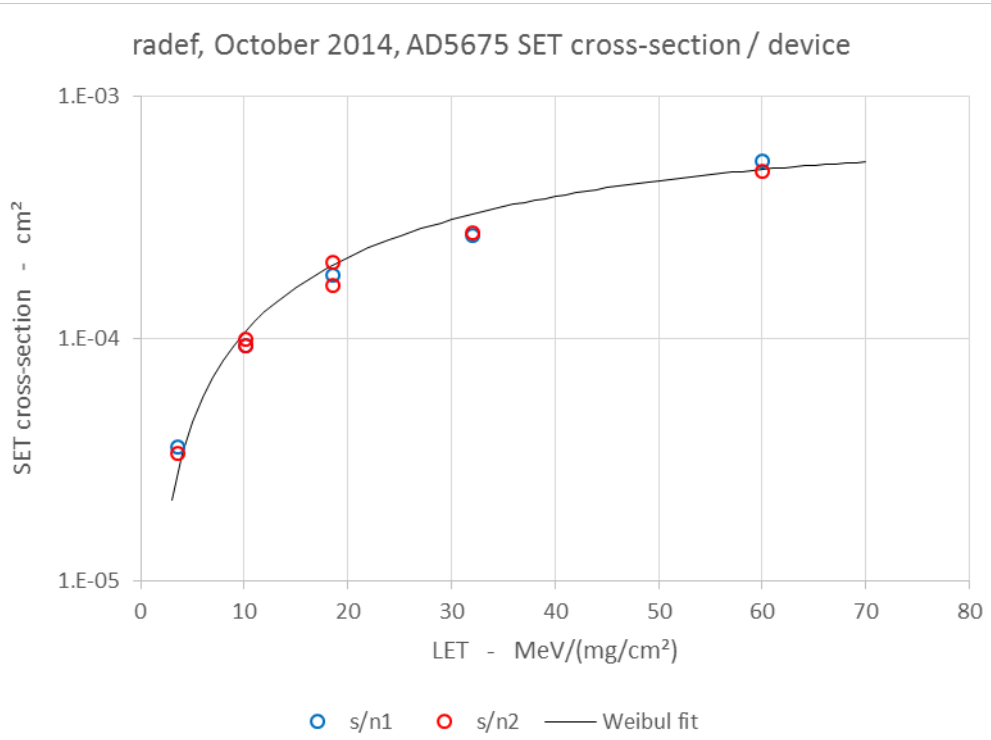
Sampling digitizer frequency = 400MHz

FUNCTIONAL BLOCK DIAGRAM

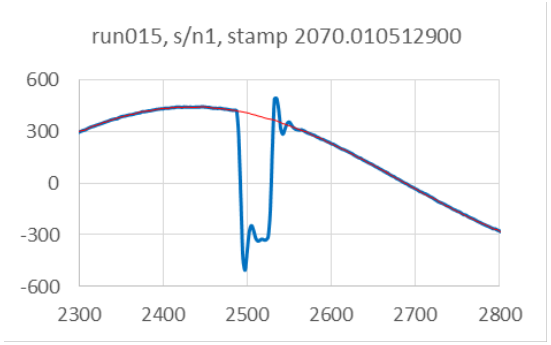


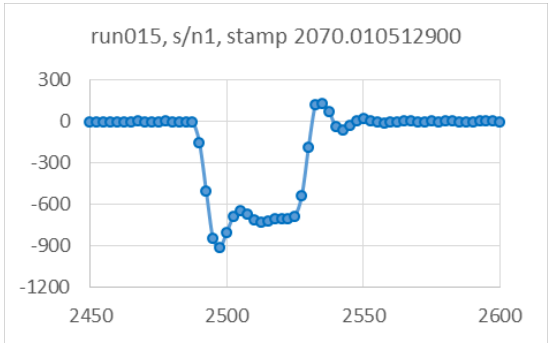
No latchup has been detected for any run with LETs up to 60MeV/(mg/cm²)
No flattening nor SEFI
All the events detected were burst events likely related to the bandgap reference burst events (expected as internal reference)
No single conversion event was detected. One hypothesis might be related to the internal current source array that should contain 2^14 elementary current sources and current switches. If an ion upset 1 or few current switches, the impact would be only few DUT LSBs, well inside the EB window (in tester LSBs) used.
EB= 34 LSBs (10 bit digitizer) corresponding to 612 LSBs 14 bit DUT

DAC5675A



Burst event example





Amplitude=1044LSBs
Duration=57.5ns

Discussion on ADC SEE test methods

SET events cross-sections

- The three methods were found equivalent for providing the event cross-section curve versus LET value.

SEE Test on DUT with Data ready signal

- RHF1401: Very few false pulses upsets have been detected with hirex method and 4 points method
- AD976A: 2 events have been detected with hirex test method.
- Beat frequency or SP methods do not allow for detecting such errors.

Burst events

As soon as 1 conversion error trigs the recording of 4096 points (including the pretrig points), any of the three methods and even SP method were able to record burst events.
When several pretrig periods are recorded within the 4096 points, it is possible to extract the burst shape out of the perturbed output sequence.

Flattening and / or SEFI

Such flattening events have been seen with AD1278 with hirex method and even with beat frequency. Reason is that a first error trigged the record of the 4096 points and then the short SEFI is recorded.

Recommendations

This study has shown that having a system able to record 4096 conversion points (including pre-trig) as soon as 1 point is above the defined EB window is well adapted to the test of A/D or D/A converters.

For beat frequency and 4P methods, the testing system absolutely needs to include a module for the generation of synchronized signals (sine wave input and sampling frequency) with a very good frequency resolution for both.

For hirex method, this module is still preferable to get a more precise error detection (EB reduction), but not strictly necessary.

If a high frequency sine wave input is requested, beat frequency or 4P methods are recommended. If not hirex method is the easiest one to implement.

As already suggested in [1], and as it is easy to select and implement the different methods with the signals generation module, several methods can be used to better characterize a A/D under test (versus input frequency, smaller EB windows, etc.)

(1) : Enhancing Observability of Signal Composition and Error Signatures during SEE Analog to Digital Testing' – M. Berg et Al, IEEE Transactions on Nuclear Science, Volume 57, Issue: 4

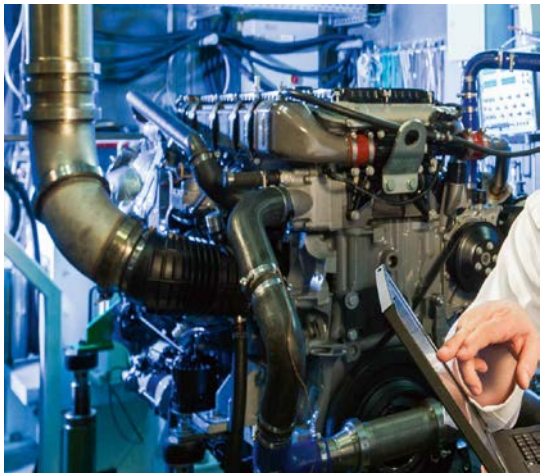
Backup Slides

Company Overview

TÜV NORD Group main areas

ENERGY

IT



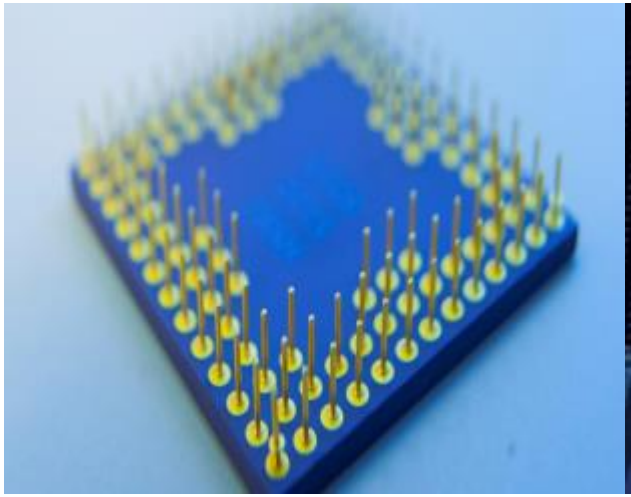
MOBILITY

HEALTH AND NUTRITION

NATURAL RESOURCES

AEROSPACE & ELECTRONIC

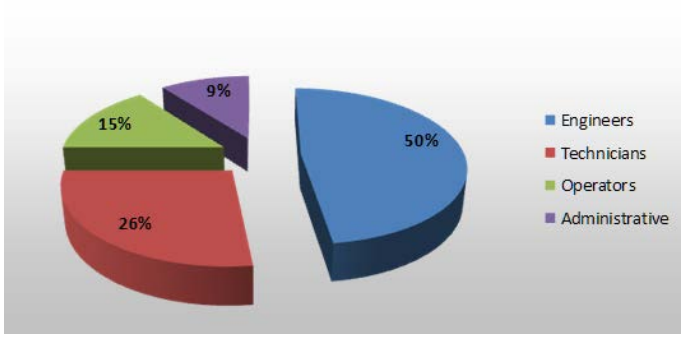
Aerospace & Electronic Business Unit

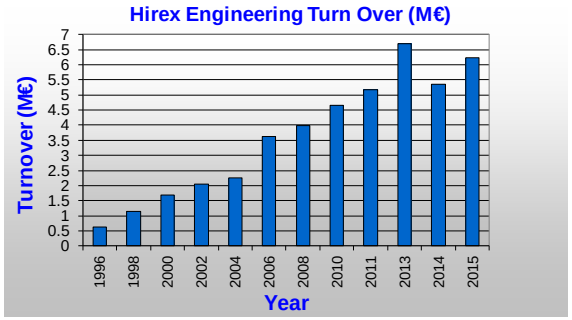


Alter technology group: with **30** years experience in the sector.

Hirex Profile

- Hirex Engineering founded in January 1993.
- Hirex Engineering joined ALTER Technology Group in January 2007.
  - ATN based in Madrid, Seville, Roma, Portsmouth and Shanghai.
  - ATN employees 230 as of today.
  - ATN Turn-over 65 M€.
- 100% Privately owned by TÜV NORD since 29th June 2011.
- Hirex Engineering :
  - Based in Toulouse.
  - 48 employees as of today.
  - 1800 m² Facility.
  - Certified ISO 9001, EN 9100 and ISO 14001.





Expertise & Activities

3 labs for a focused organization:

- SEE: Radiation lab.
- LAT: Semiconductor Technology lab.
- LTE: Electrical & environmental test lab