A Fully-Physical Simulation Framework of Single-Event Effects

Cogenda Pte Ltd
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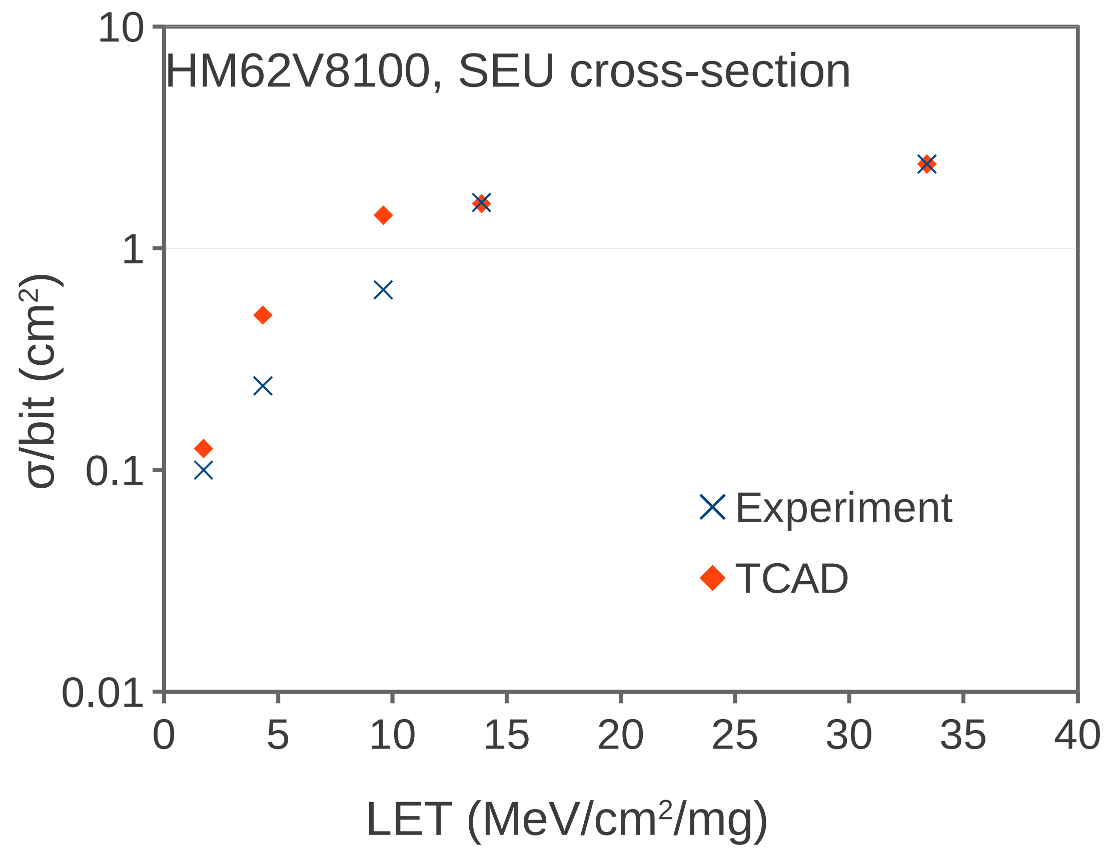
Summary

- Build 3D model for a commercial SRAM chip
- Fully-physical simulation
  - Particle simulation (Geant4)
  - TCAD simulation (TCAD)
- Compare the simulated SEU cross-section against experimental data
- Validated the viability and correctness of the fully-physical approach



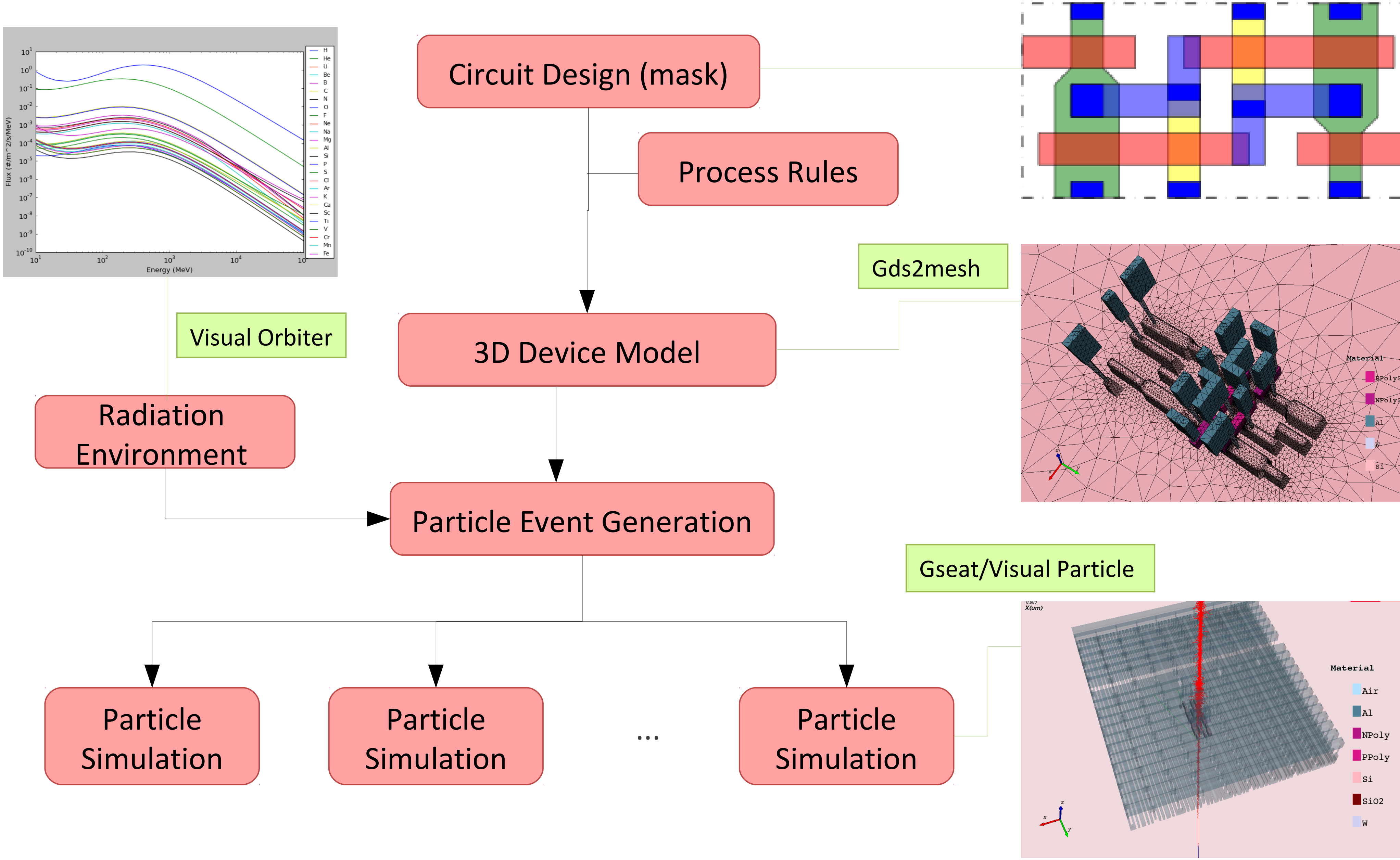
Ion	Energy (MeV)	LET (MeV/cm²/mg)
$^{12}C^{6+}$	80	1.73
$^{19}F^{8+}$	104	4.33
$^{28}Si^{10+}$	126	9.6
$^{35}Cl^{11+}$	138	13.6
$^{63}Cu^{13+}$	161	33.4

H.X. Guo et al, Atomic energy science and technology, v44, pp. 1498-1504, 2010.

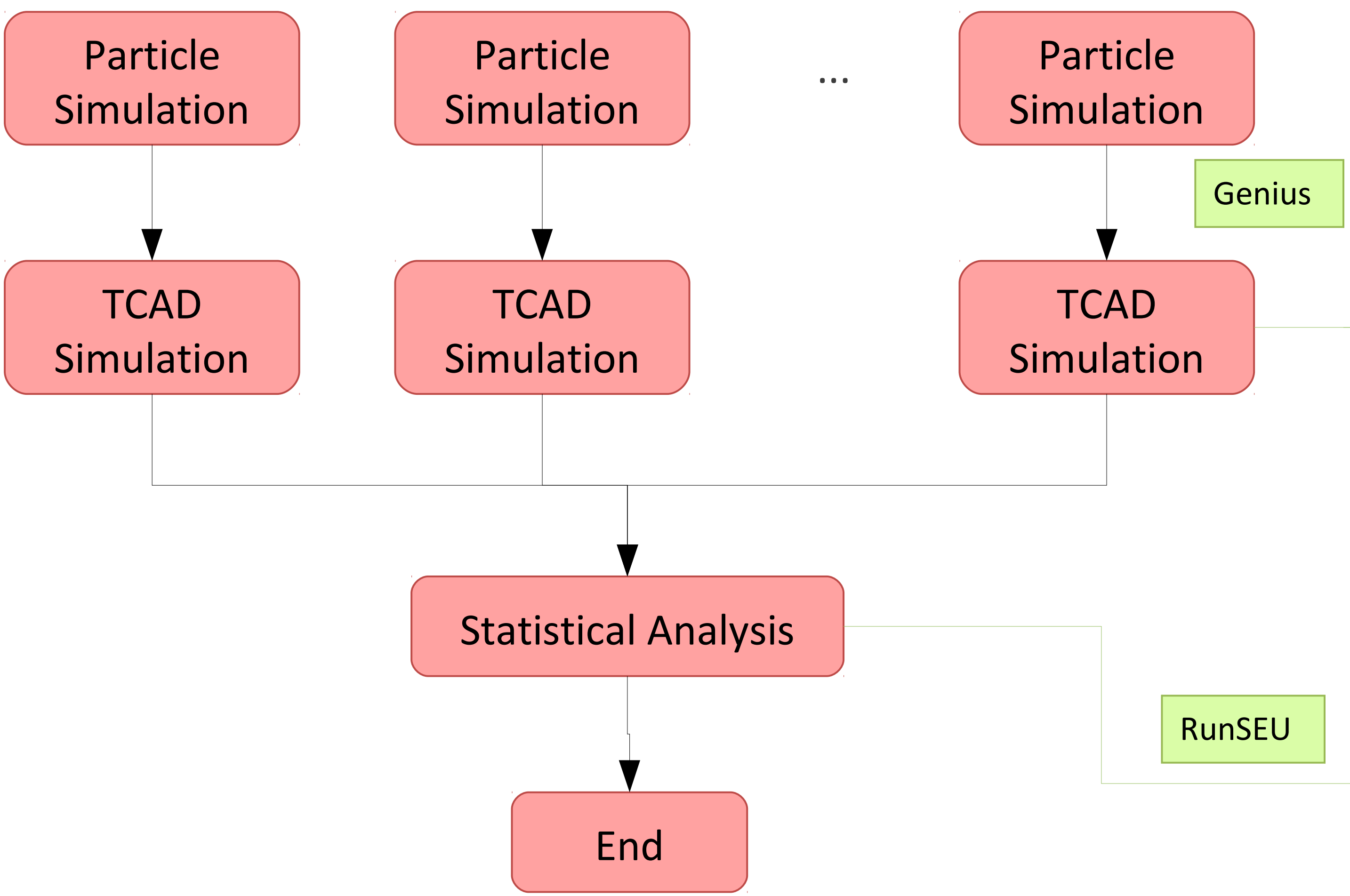
Outline

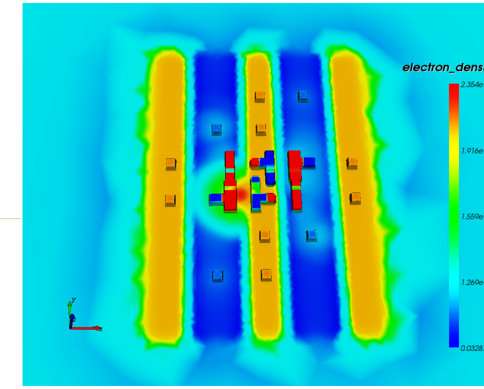
- Components in the framework
  - 3D modeling: Gds2mesh
  - Geant4-based particle simulator: GSeat
  - TCAD device simulator: Genius
  - Statistical sampling: runSEU
- Applications
  - SEU Cross-section of a 0.18um SRAM: HM62V8100
  - Single-event block upset in 90nm SRAM: CV62126EV
  - Extension to Multiple-Composite-Sensitive-Volume model

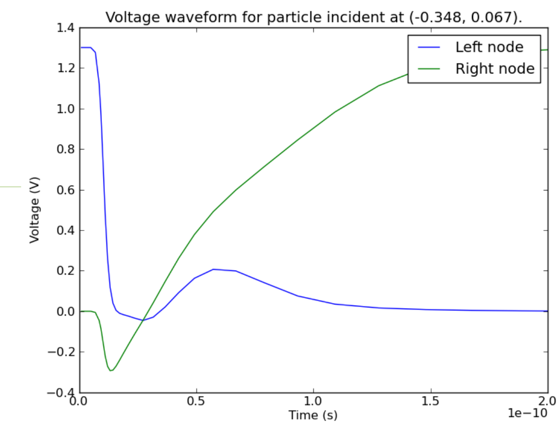
Components in the Framework

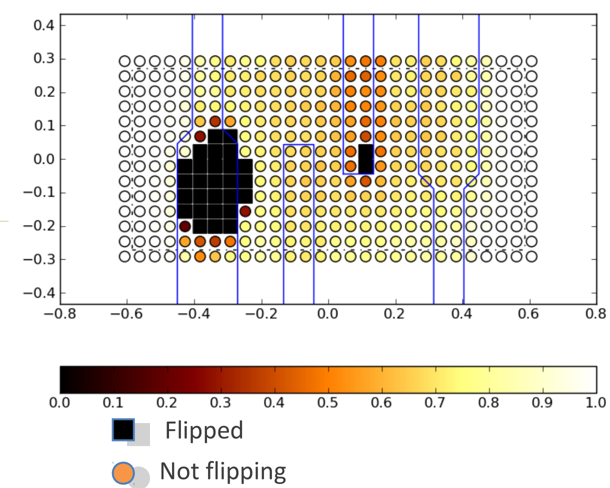


Components in the Framework

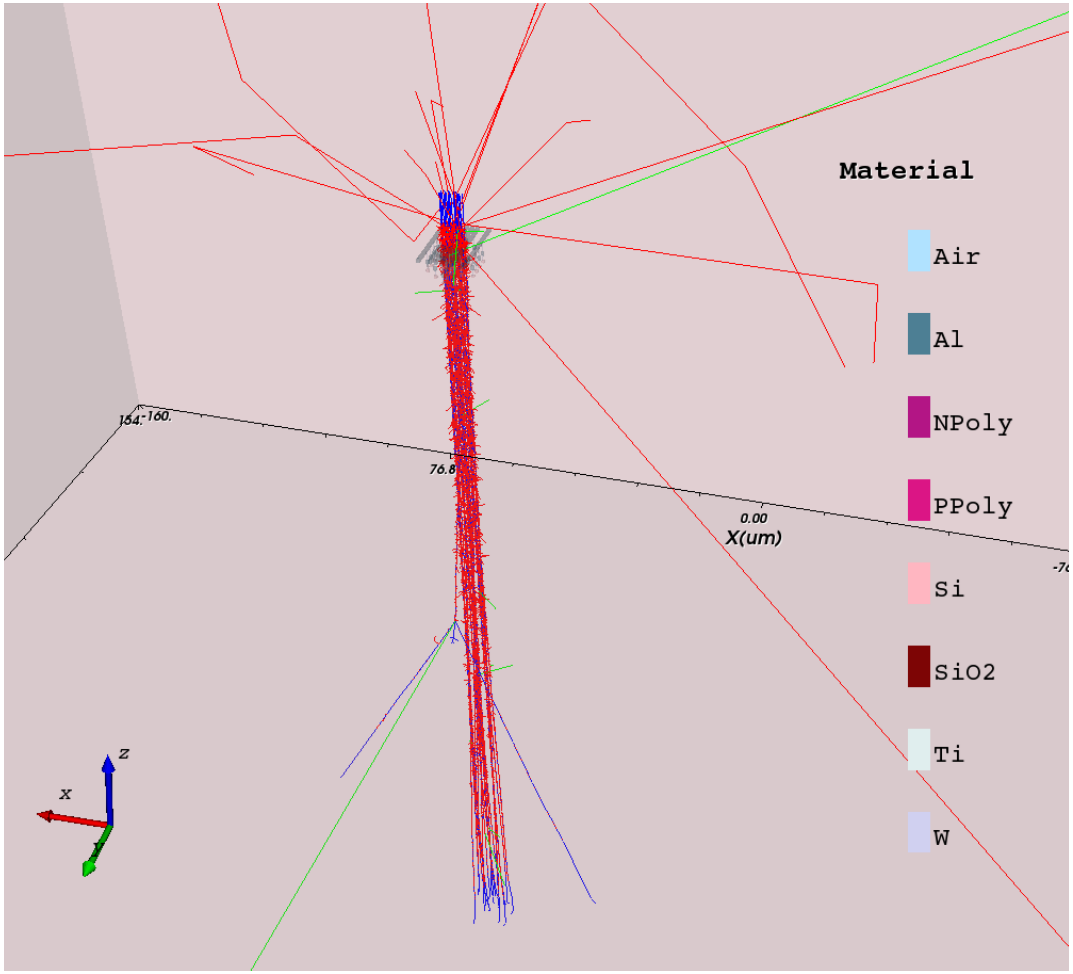








Particle Simulation



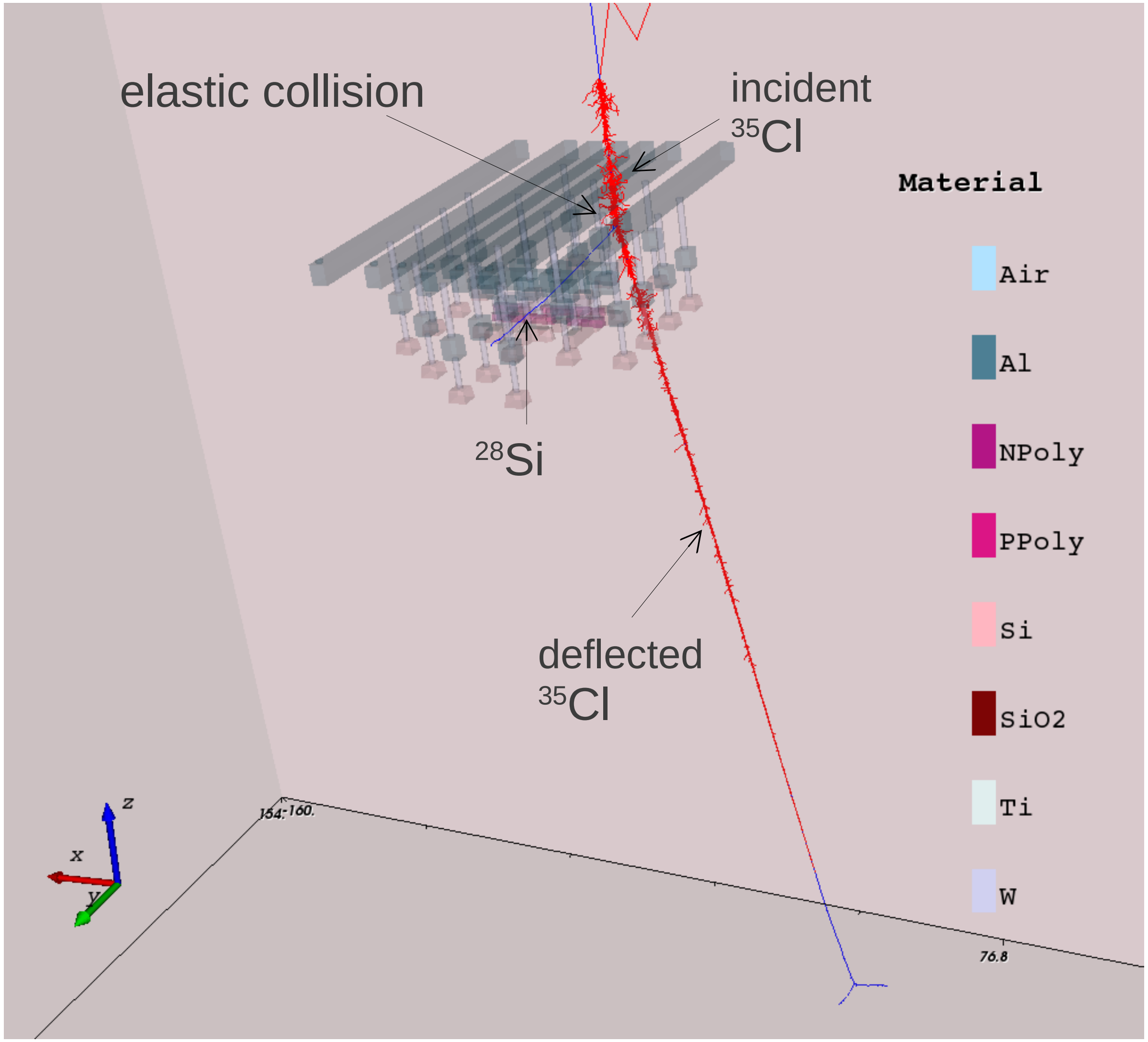
20x C^+ 80MeV

- Physics list from SLAC with updates
- E.g. Physics models for heavy ions:
  - Electromagnetic interactions
    - Multiple scattering
    - Screened Coulomb scattering
  - Hadronic
    - Inelastic collision

Blue: positively charged particles
Red: negatively charged particles
Green: neutral particles

Particle Simulation: Nucleus Recoils

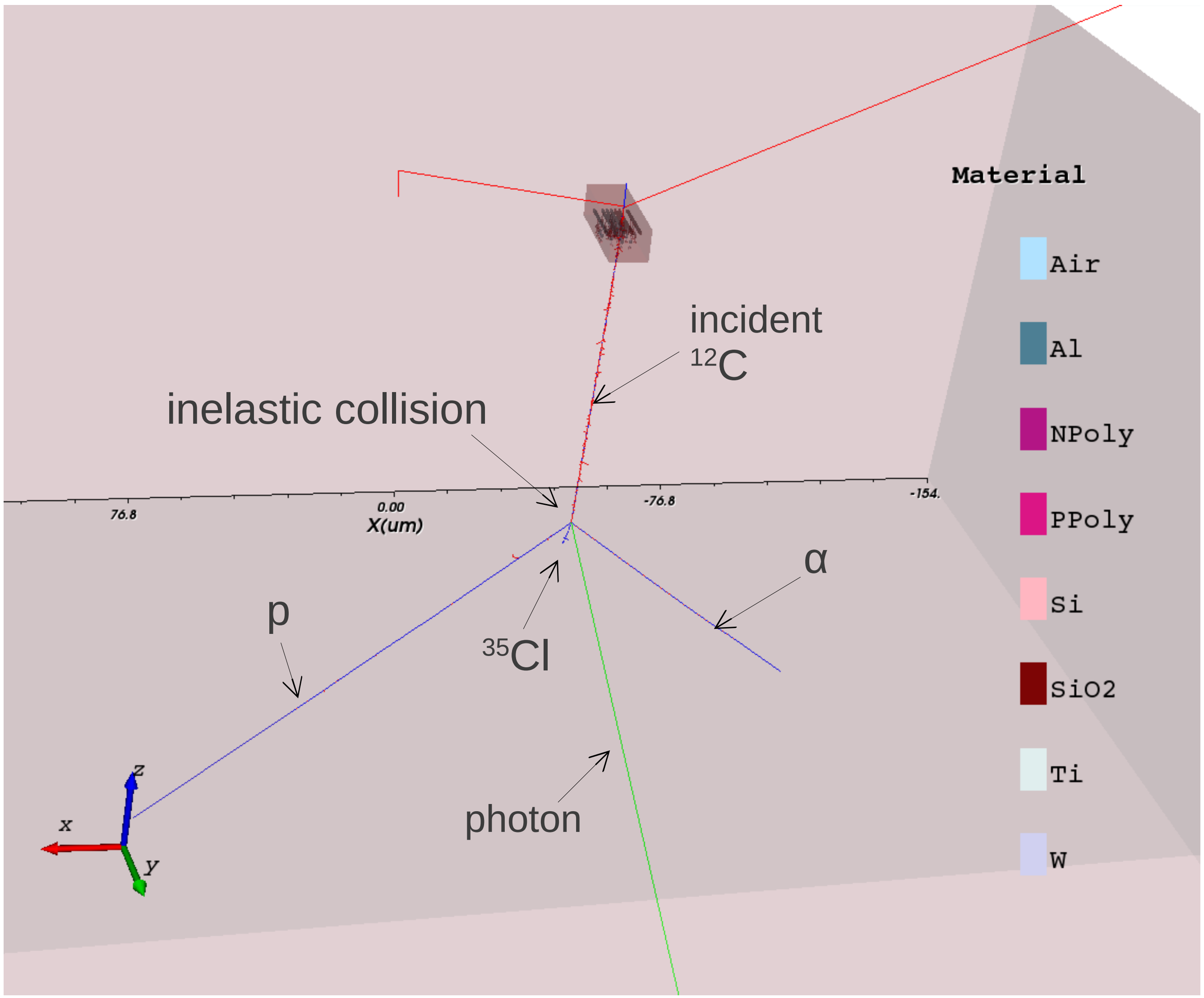
$^{35}Cl^{+}$ 138 MeV



- G4ScreenedNuclearRecoil
- Produces a recoil ion, may increase energy deposited in sensitive volume
- Large scattering angle is possible
  - Can we bias this process?
- Recently become important
  - SEU cross-section seen by a customer can only be explained by NR

Particle Simulation: Inelastic Nuclear Collision

$^{12}C^{+}$ 80MeV



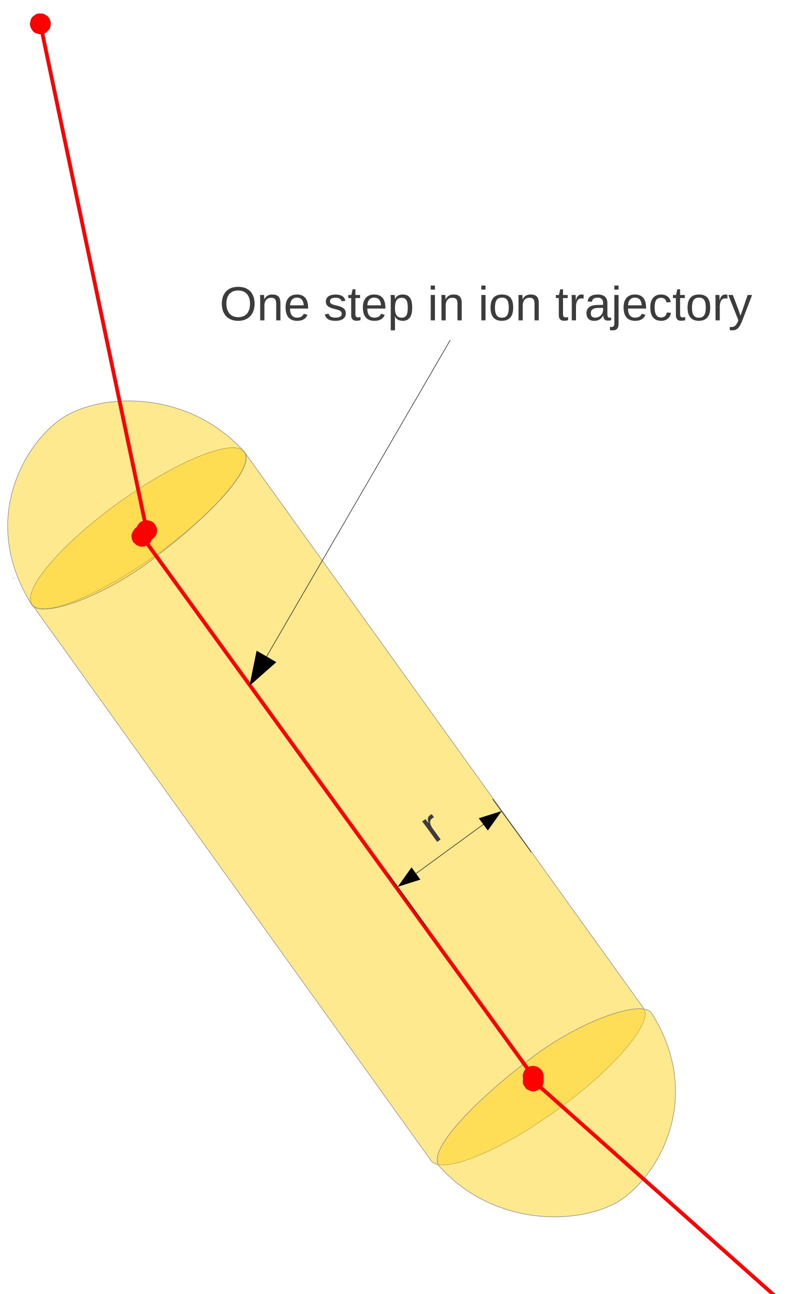
- Enabled models:
  - G4QDM
  - Binary Cascade (light ions)
  - EM-dissociation
- Produces several secondaries, may affect several sensitive volumes.
- We haven't seen any ground test data that invokes inelastic collision model.
- Needed when extrapolating to SEU rate in space environment.

Interface of Geant4 to TCAD

- Conversion
  - From Geant4: trajectory and energy deposition
  - To TCAD: e-h pair generation rate
  - Exchange rate: 3.6eV → e-h pair
- Spatial Structure of Ion Trajectory
  - Energy deposition of each step
  - Distributed in a capsule-shaped region, according to

$$f(r) = \frac{E_{dep}}{\Omega} \exp\left(-\frac{r^2}{L_{\mathrm{ROC}}^2}\right)$$

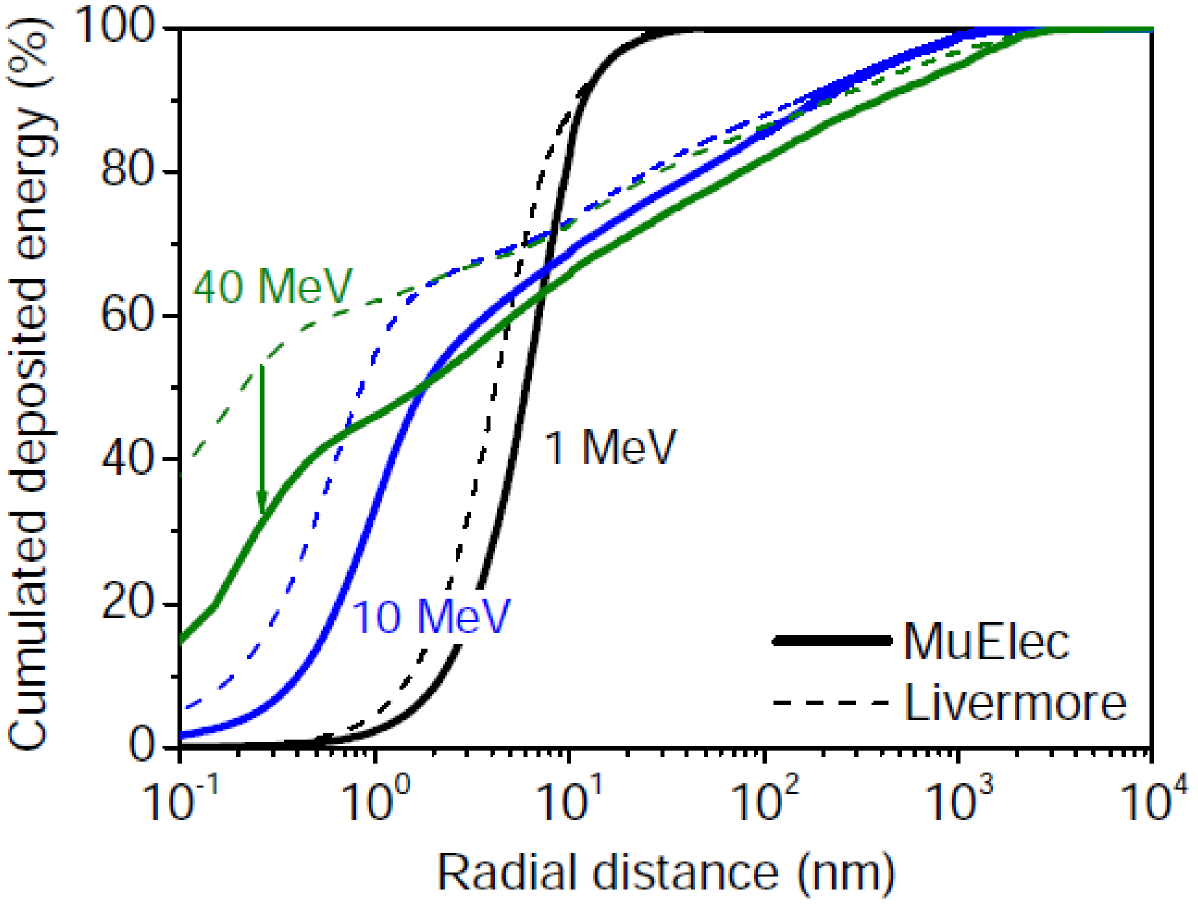
  - Known to be incorrect.



Structure of Track

Detailed simulation shows that radial distribution of deposited energy

- dependent on energy,
- has complex function form.



- Too expensive to be used on regular basis
  - Too slow
  - Takes too much disk space
- Need an analytic model for radial distribution
  - e.g. A. Akkerman NIM 2005.

M. Raine et al, NSREC 2012

Structure of Track (in development)

- Radial structure of track consists of two components
  - Core
    - Many low-energy electrons
    - Low fluctuation from particle to particle
    - Analytic model
  - Tail
    - Dominated by fewer number of high-energy electrons
    - Large fluctuation from particle to particle
    - Track individual high-energy electron in Geant4

- To merge the two components
  - What's the appropriate cut-off range?
    - particle/energy dependent?
  - Truncation of the analytic model?

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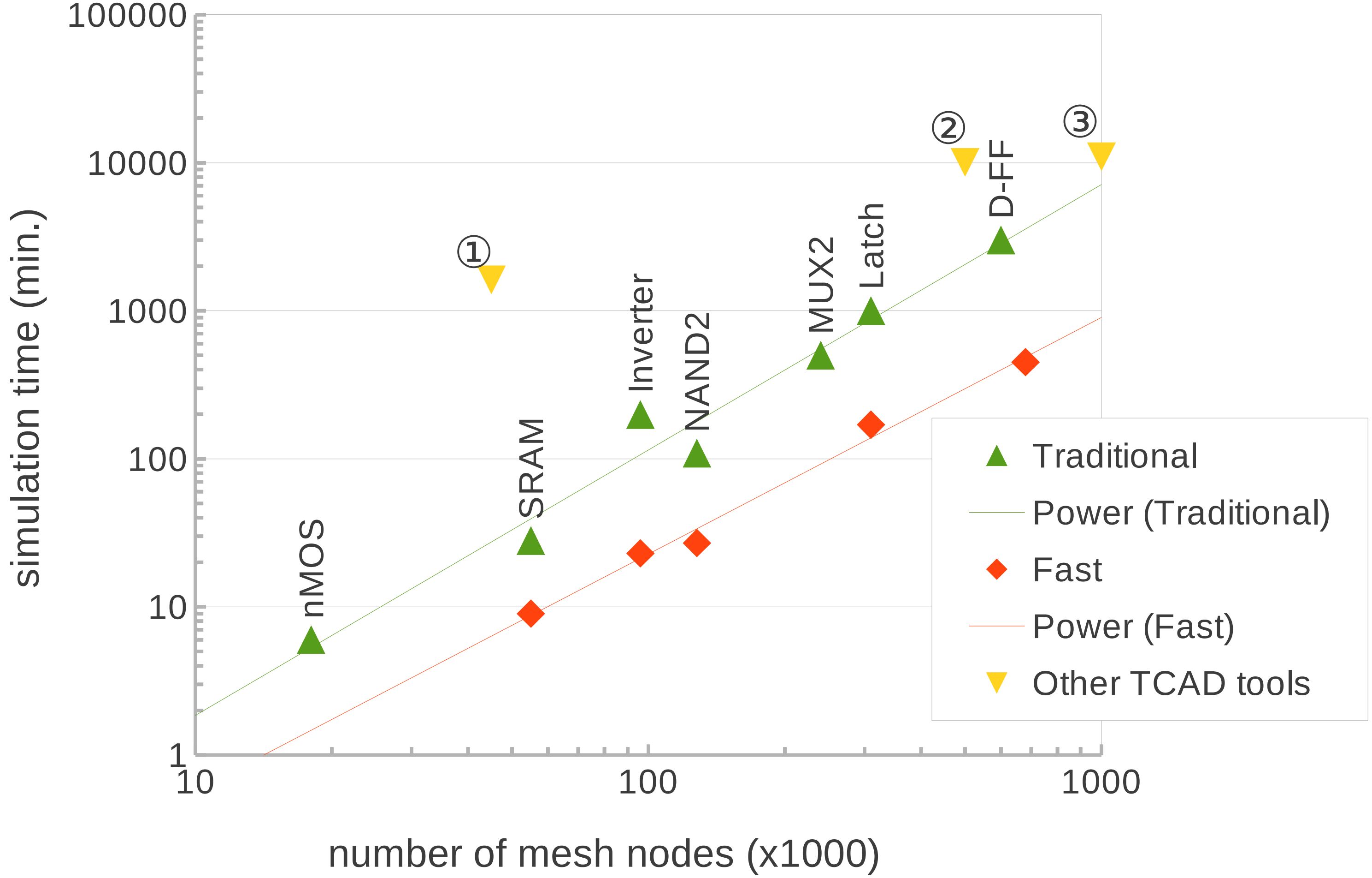
Fast Solver: Overview

- Fast Solver
  - 5x to 10x speed in transient and operation point analyses
  - No change in device equations: Same physics
  - Half-implicit algorithm to solve equations
  - Suitable for CMOS circuits with 2-30 transistors (30k – 5m mesh nodes).
- Status
  - Started in 2010, Stable since Sep 2011
  - Tested extensively with selected customers
  - Presented at SISPAD2012
  - China/US Patents being filed

Fast Solver: Simulation Speed



Cogenda data points:

Transient of two switches (rise/fall), 2 CPUs (Xeon 5620)

Other TCAD data points:

1: 6T SRAM, 45K mesh nodes, transient 4 CPUs yr2008 (old)

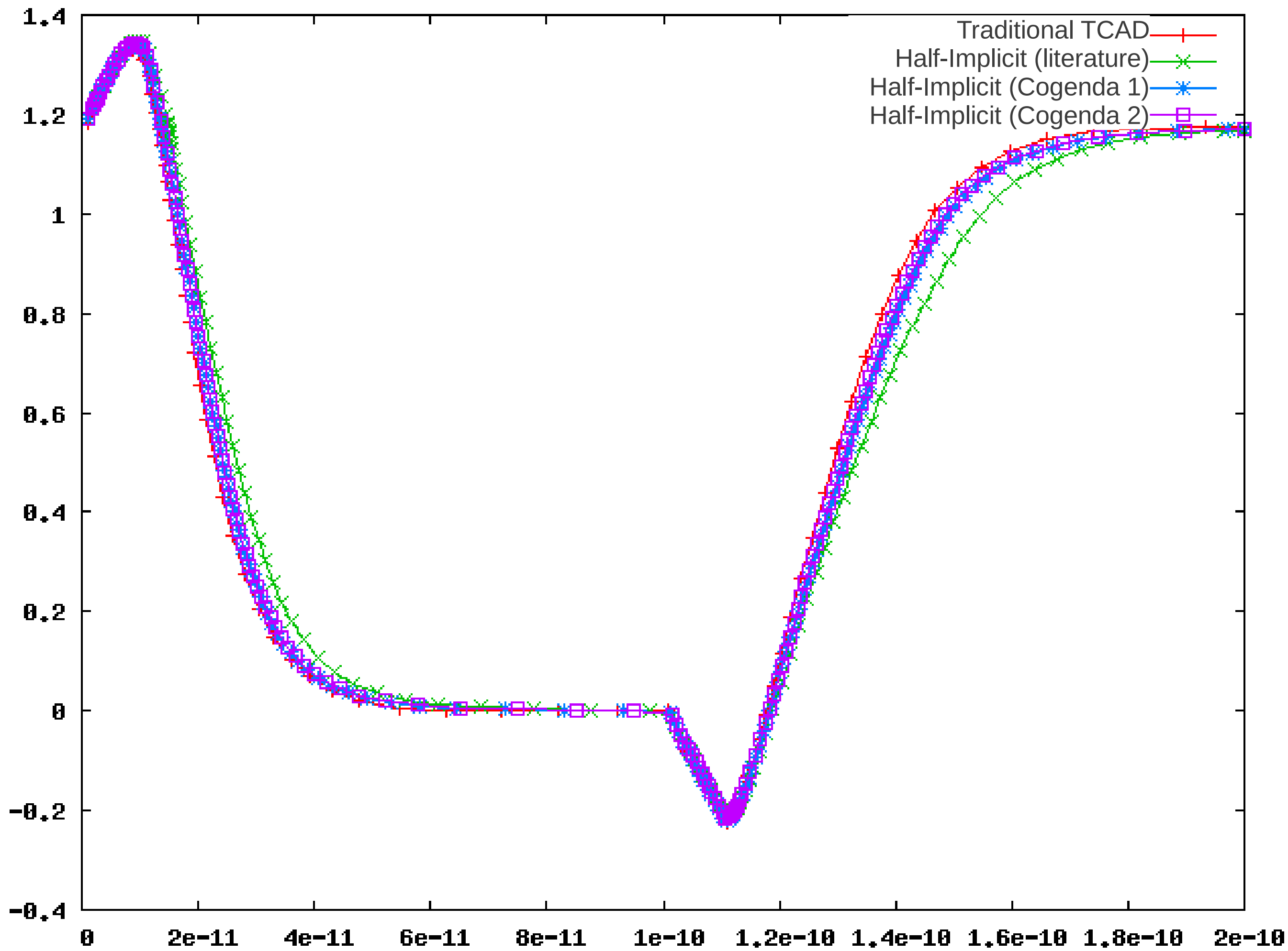
2: power device , 500K mesh nodes, steady-state ? CPUs

3: 6T SRAM, 1million mesh nodes, steady-state 4 CPUs yr2011 (latest)

Trad.: Fully-implicit method
Fast: Half-implicit method

Fast Solver: Simulation Accuracy

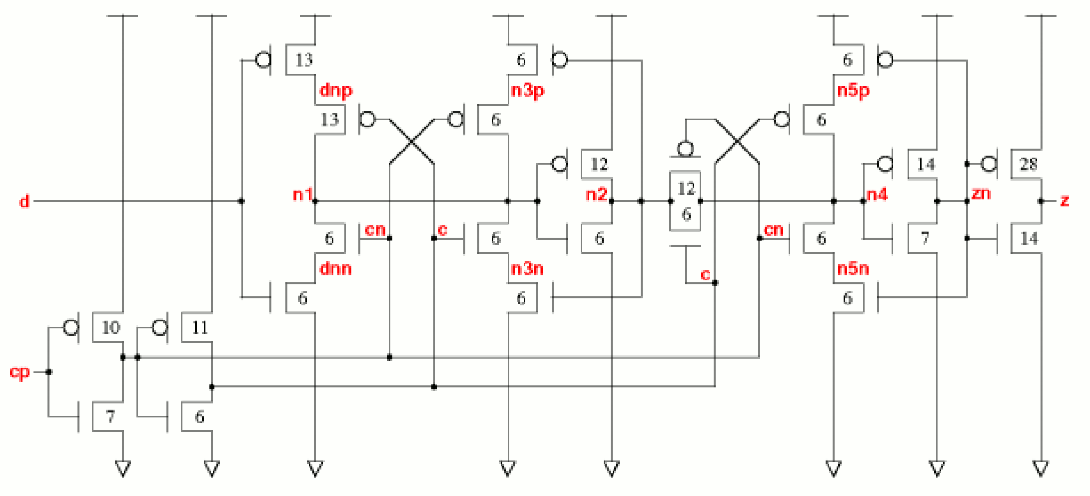
Error in inverter rise/fall time < 5%.



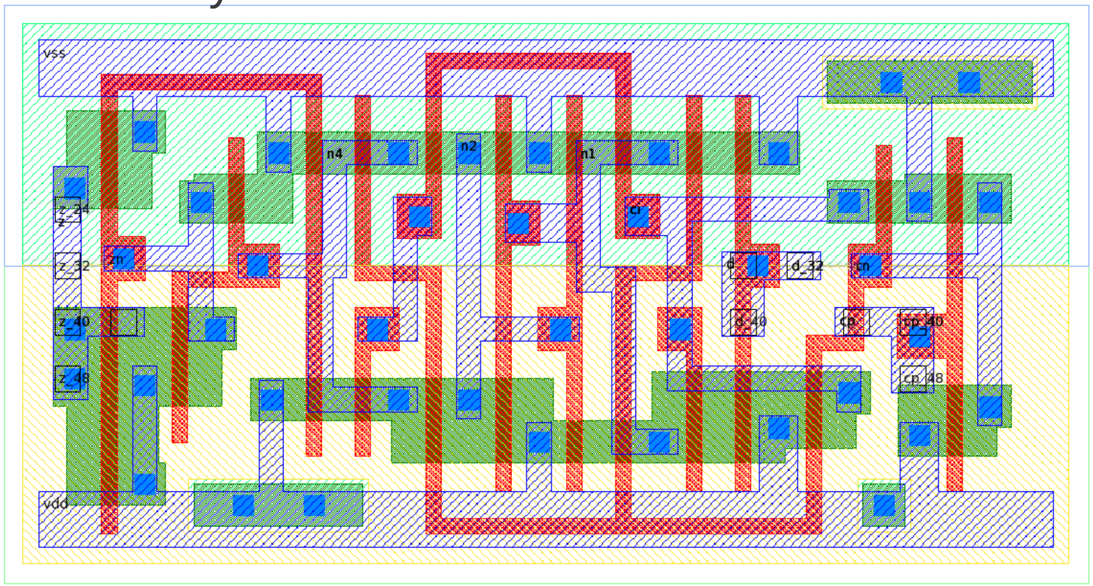
Inverter circuit, 110k mesh nodes

World's Largest TCAD Simulation

Schematic



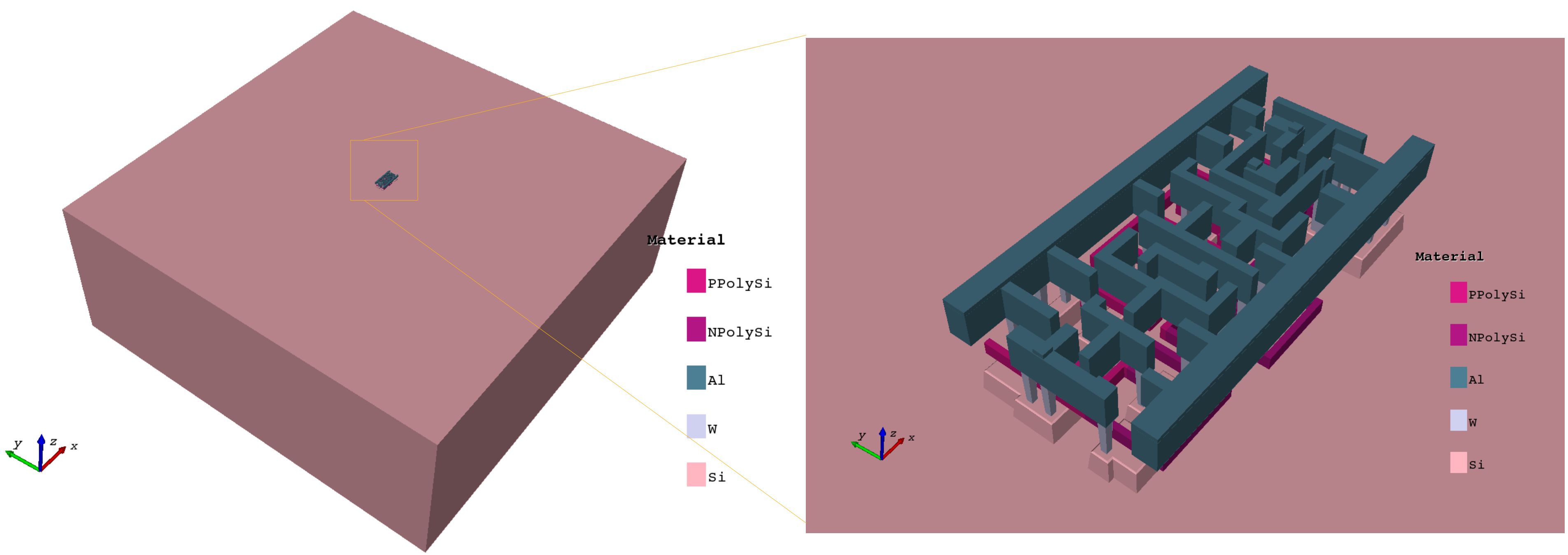
Mask layout



- D-Flipflop circuit
- 24 transistors
- 90nm CMOS design
- Largest circuit block in a standard library
- Presented at SISPAD2012

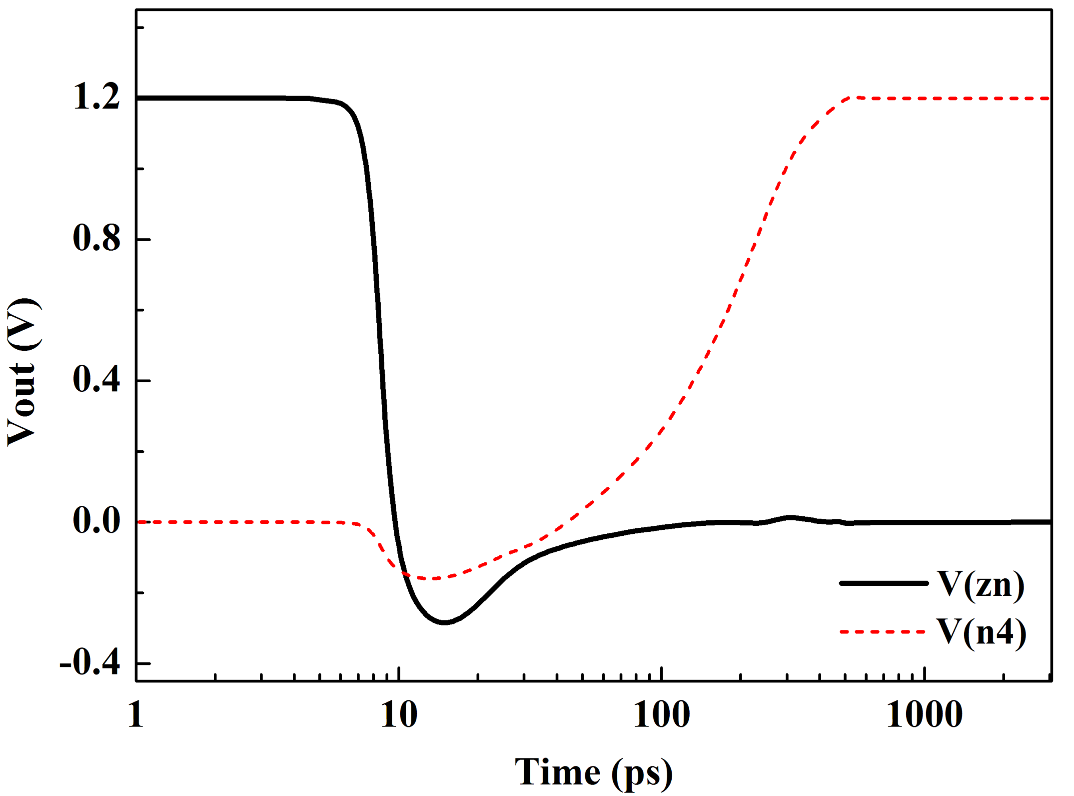
World's Largest TCAD Simulation

- Realistic 3D model
- 1,673,519 mesh nodes
- Simulation: 95 MeV Cl^+ ion strikes on the device



World's Largest TCAD Simulation

- Data flipped
- Simulate 3 ns in 252 time steps
- Completed in 268 minutes, with 48 cores.



4 nodes, dual Xeon X5670 CPUs
48 cores in total

In comparison, simulate a SRAM device (960,000 nodes) with Synopsys tool takes ~1 week.

Fast Solver for SEU

Simulation time for SEU simulation on some circuits (field data).

CMOS Circuit	Technology node	Mesh nodes (x1000)	Simulation Time (CPU E5-2650 core-hours)	Memory (GB)
6T SRAM	90nm	80	4	3
6T SRAM Hitachi HM62V8100	0.18um	310	24	10
12T RadHard SRAM	0.18um	720	70	30
12T RadHard SRAM	0.25um	600	60	24
24T D Flip-Flop	90nm	1,670	220	190

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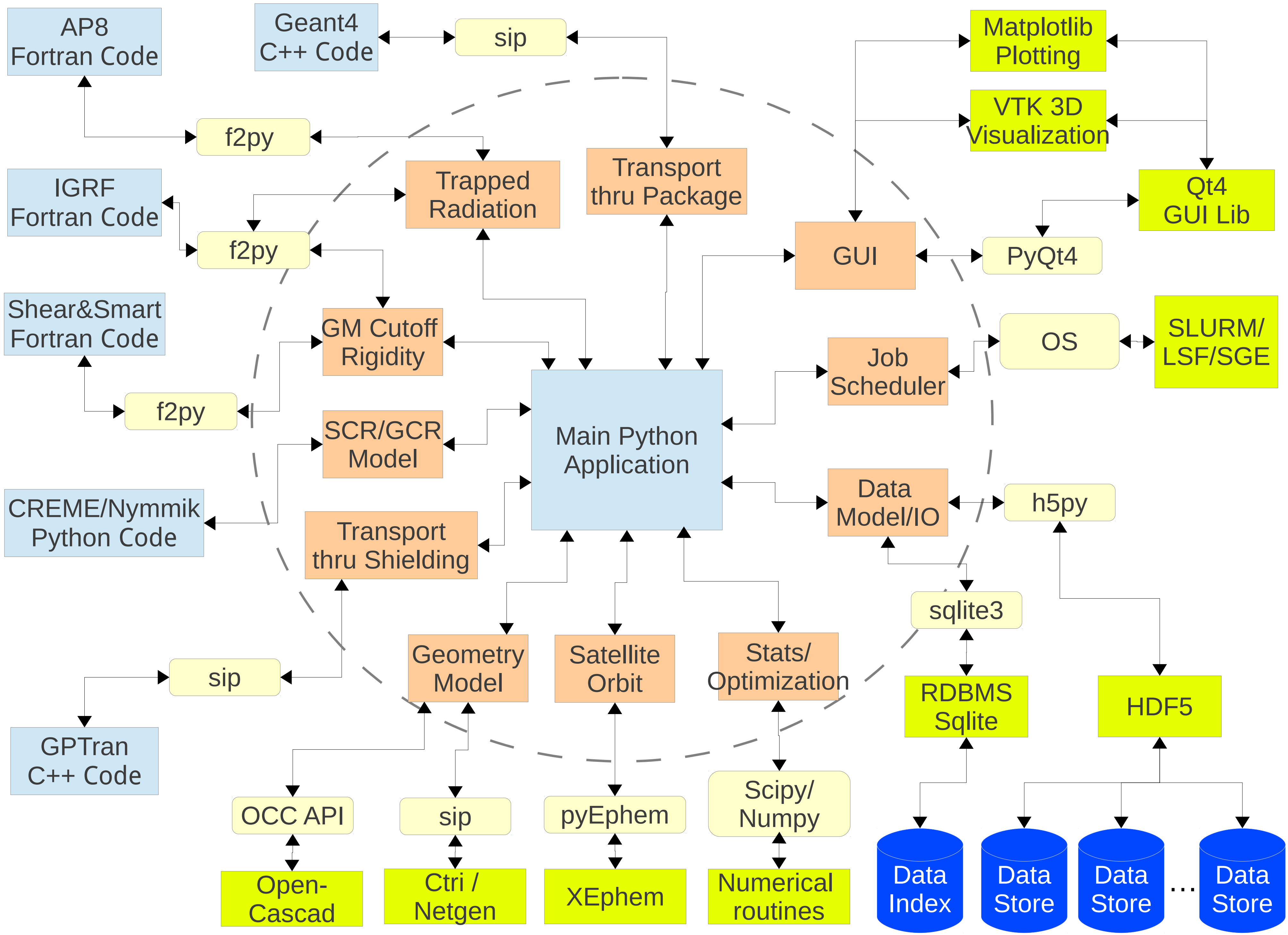
Statistical Sampling

- Performance bottleneck
  - TCAD >10,000× slower than G4 simulation
  - Reduce # of TCAD simulation aggressively
  - Ensure statistically unbiased
    - Outright reject a particle as non-SEU: incorrect
    - Assign a low SEU probability to a particle: correct in Bayesian sense
- runSEU
  - Importance sampling with Subset Simulation
  - Scheduling computation “targets” and “tasks”
  - Data management

Software Architecture

- Integrating > 10 Programs
  - Python as driver/glue language
    - Call external simulators (for long simulation)
    - Legacy C/Fortran module integrated into python
  - HDF5 for bulk data storage
  - Job Scheduler (internal and external)
  - GUI, Graphing, Visualization


AP8
Fortran Code
Geant4
C++ Code
sip
Matplotlib
Plotting
VTK 3D
Visualization
f2py
Trapped
Radiation
Transport
thru Package
Qt4
GUI Lib
IGRF
Fortran Code
f2py
GUI
PyQt4
Shear&Smart
Fortran Code
GM Cutoff
Rigidity
OS
SLURM/
LSF/SGE
Job
Scheduler
f2py
SCR/GCR
Model
Main Python
Application
CREME/Nymmik
Python Code
Transport
thru Shielding
Data
Model/IO
h5py
sqlite3
sip
Geometry
Model
Satellite
Orbit
Stats/
Optimization
RDBMS
Sqlite
HDF5
GPTran
C++ Code
OCC API
sip
pyEphem
Scipy/
Numpy
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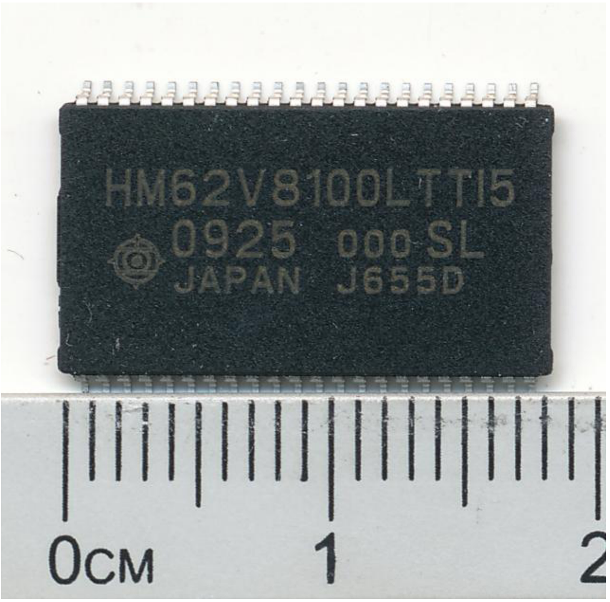
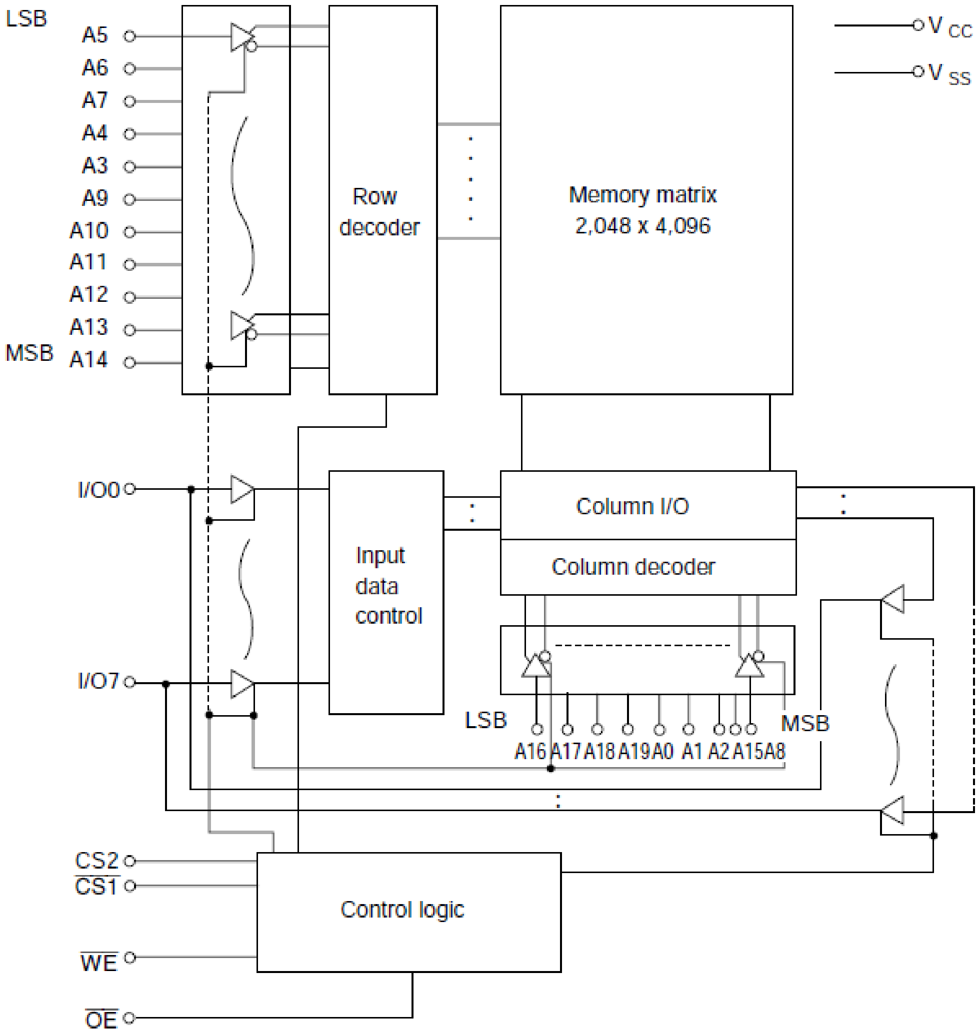
IC Structural Analysis

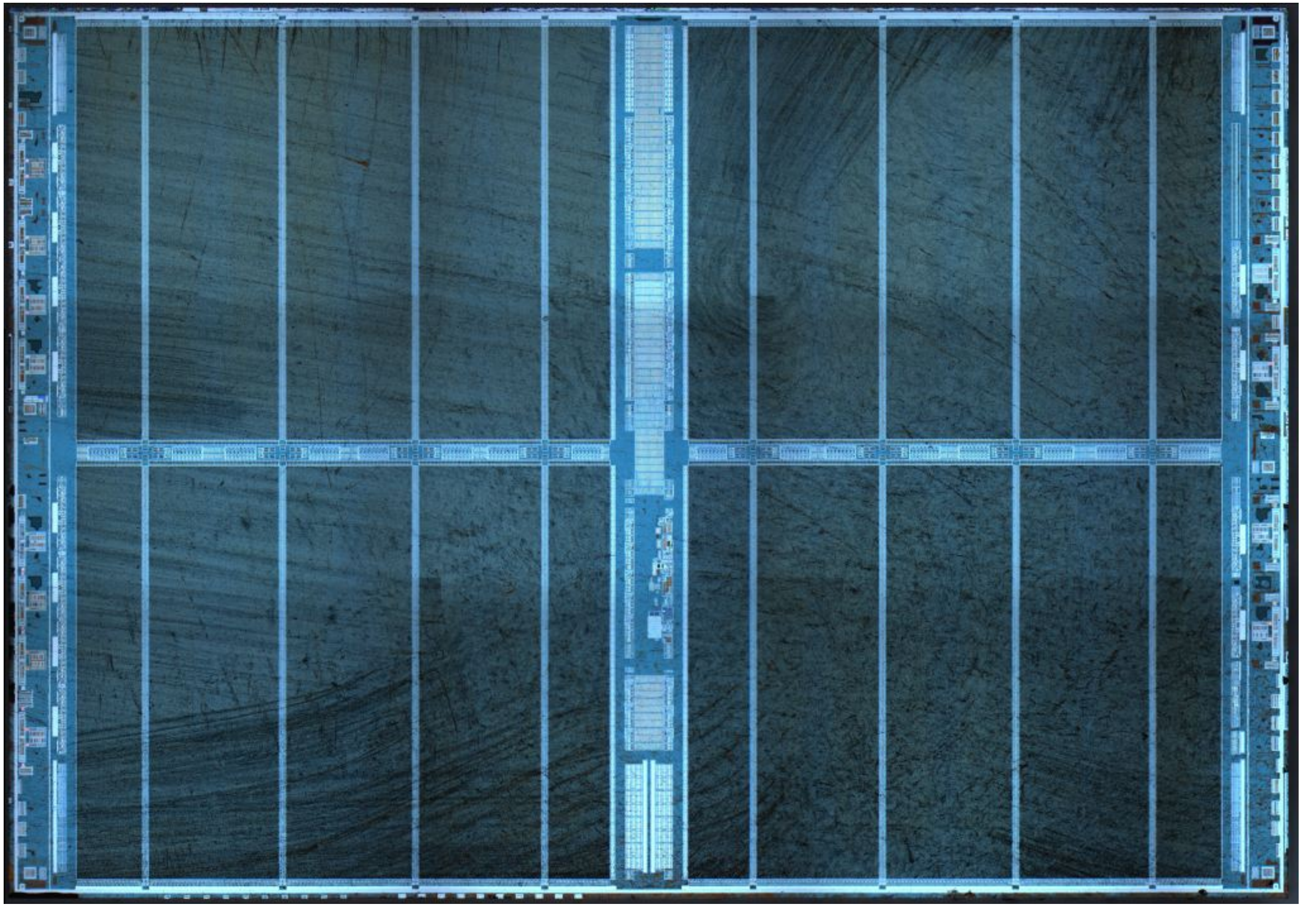
- COTS Low-power SRAM
- HM62V8100 (Hitachi)
- 8Mbit
- 0.18 µm bulk CMOS Process
- TSOP II packaging





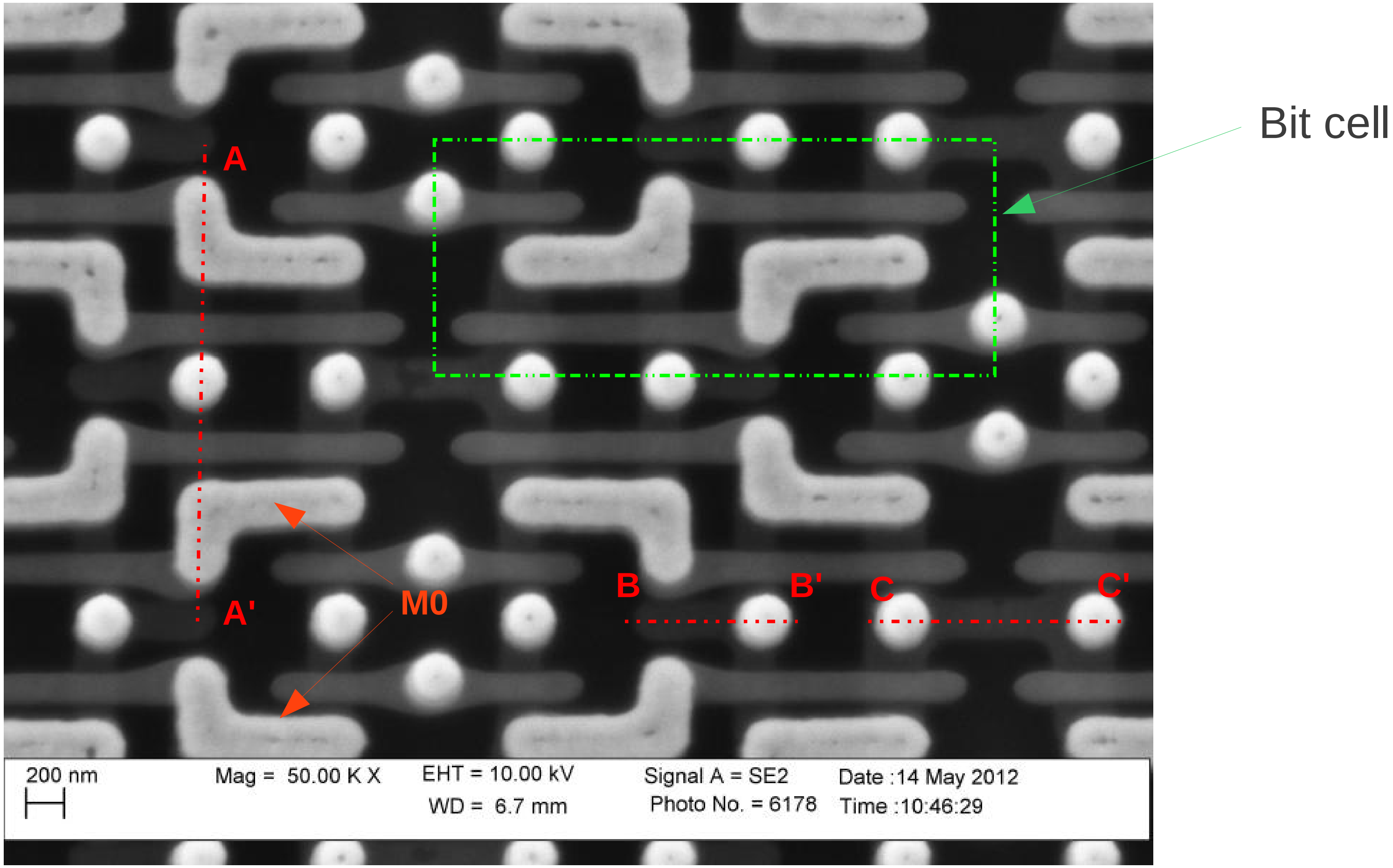
IC Structural Analysis

Optical micrograph of stained active after de-layering
Chip area 8.16mm x 5.68mm



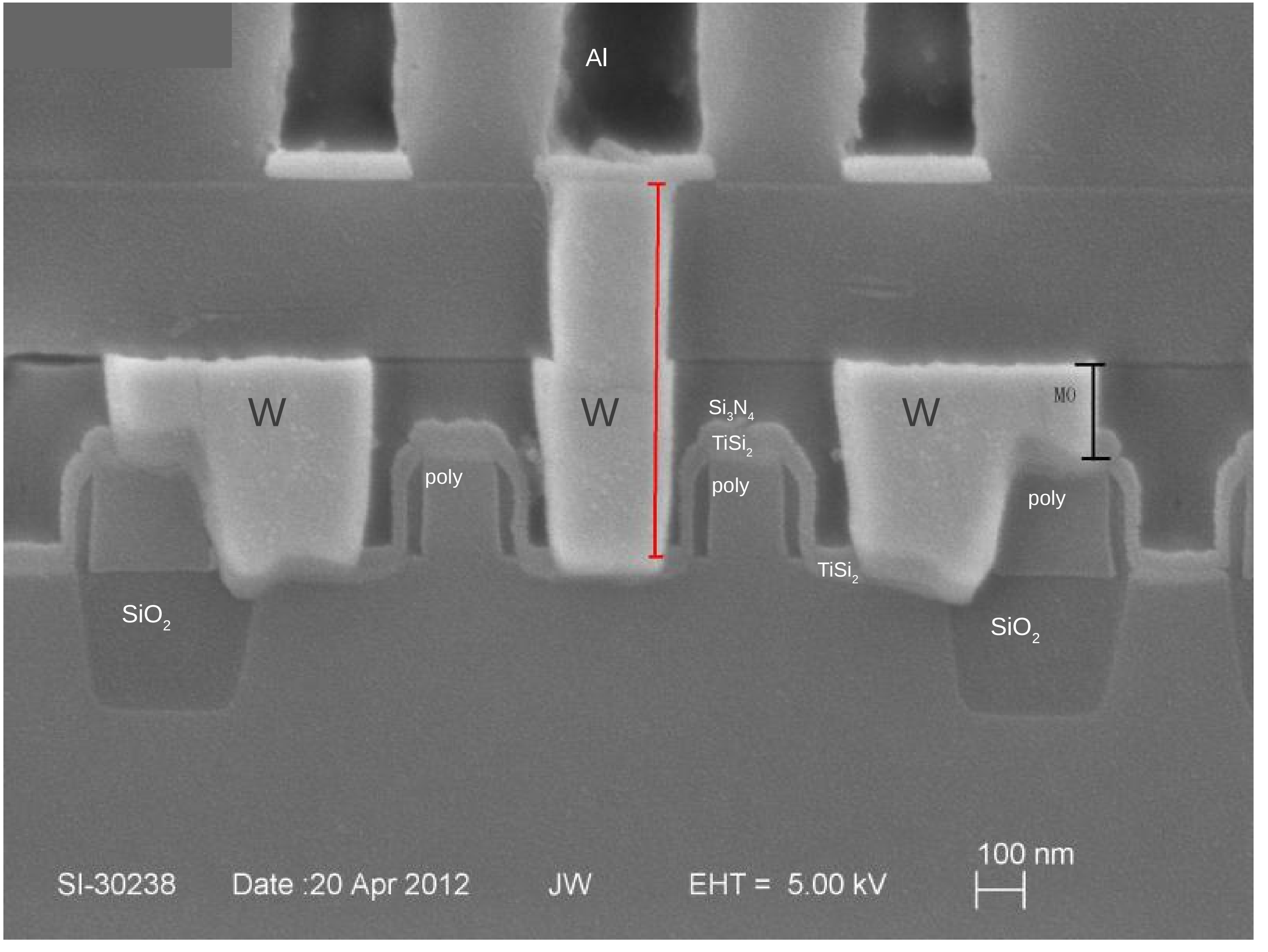
Structural Analysis: Bit Cell

SEM micrograph of the Poly layer in SRAM array
Metal 0 local interconnects are visible
Area of bit cell: 3.02 × 1.28 μm^2。



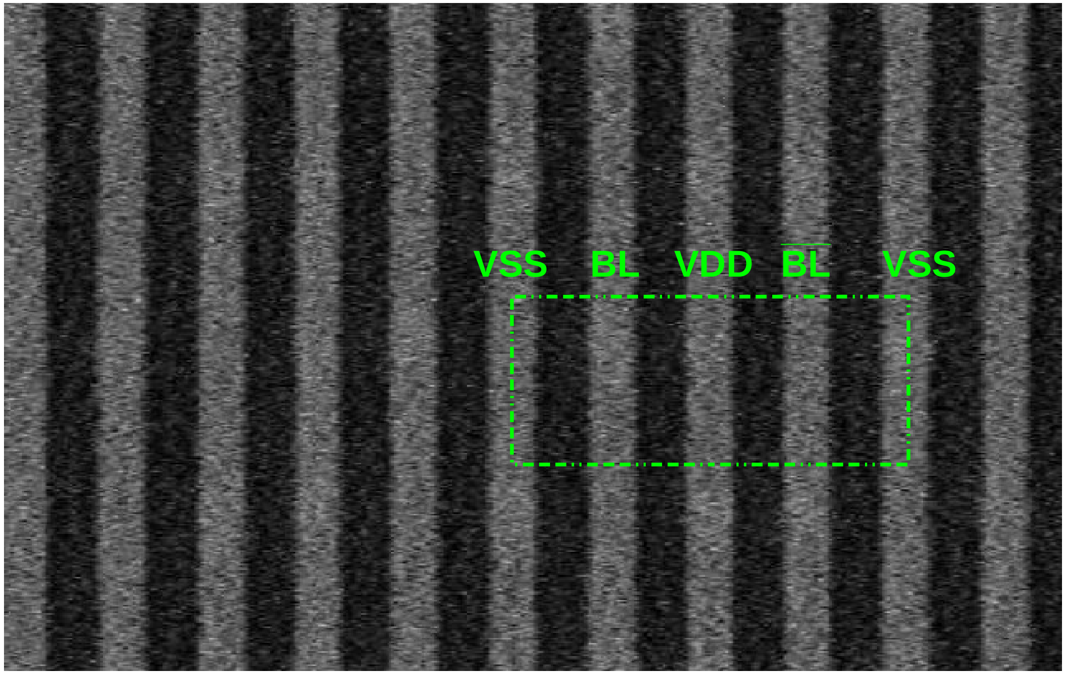
Structural Analysis: Bit Cell

Cross-sectional SEM micrograph along A–A'

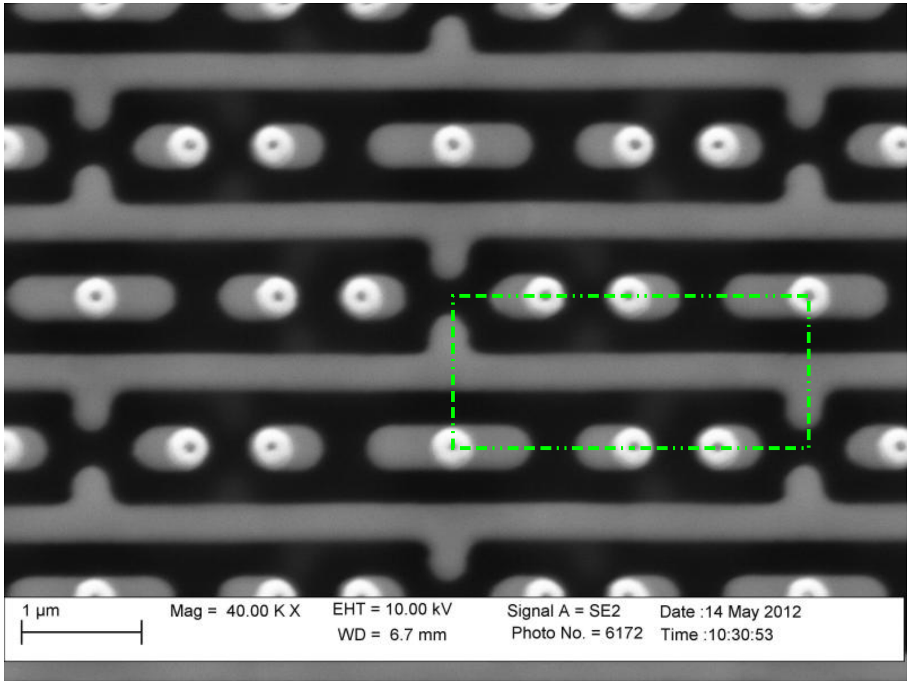


Structural Analysis: Bit-line/Word-line

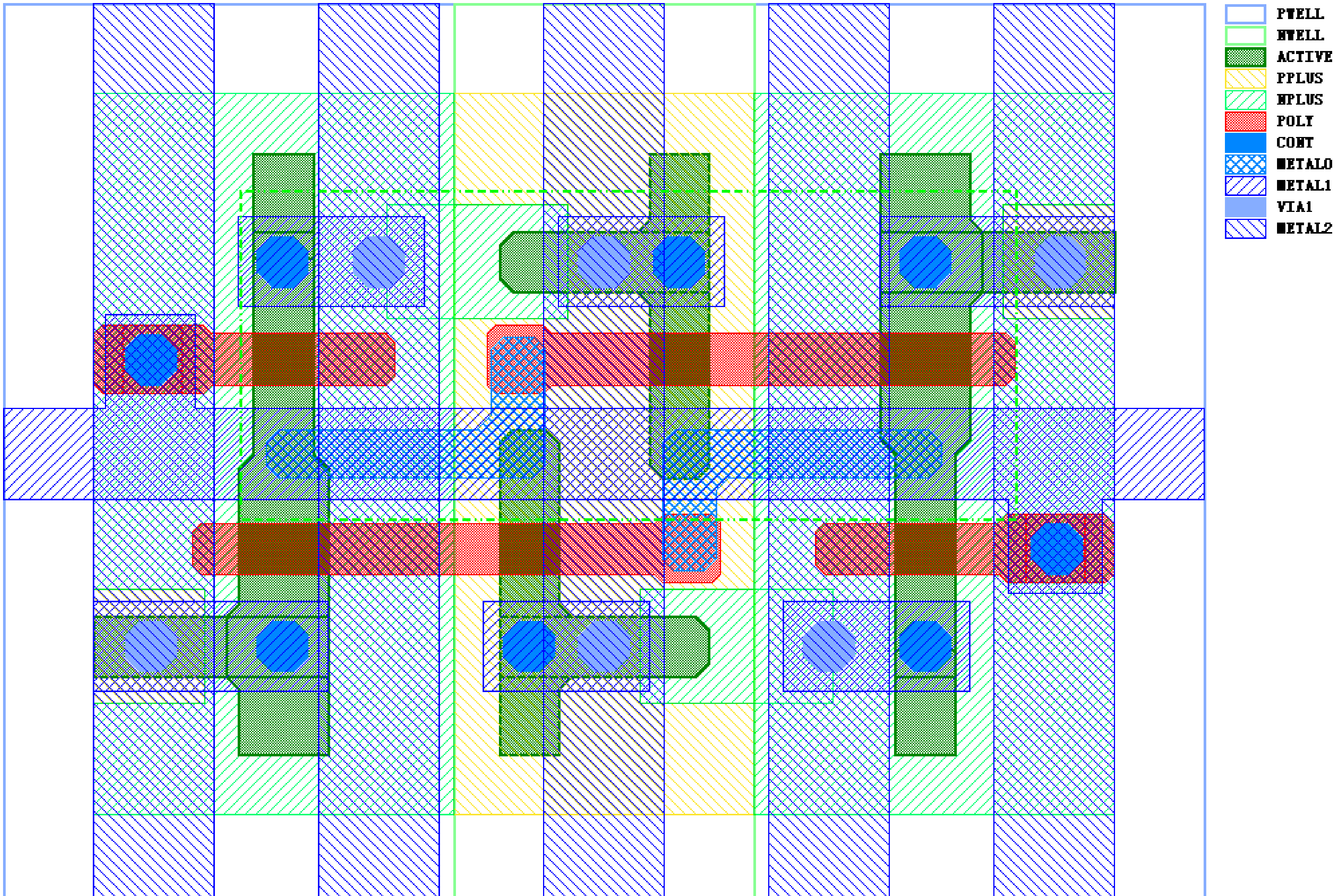
Metal 2: bit line



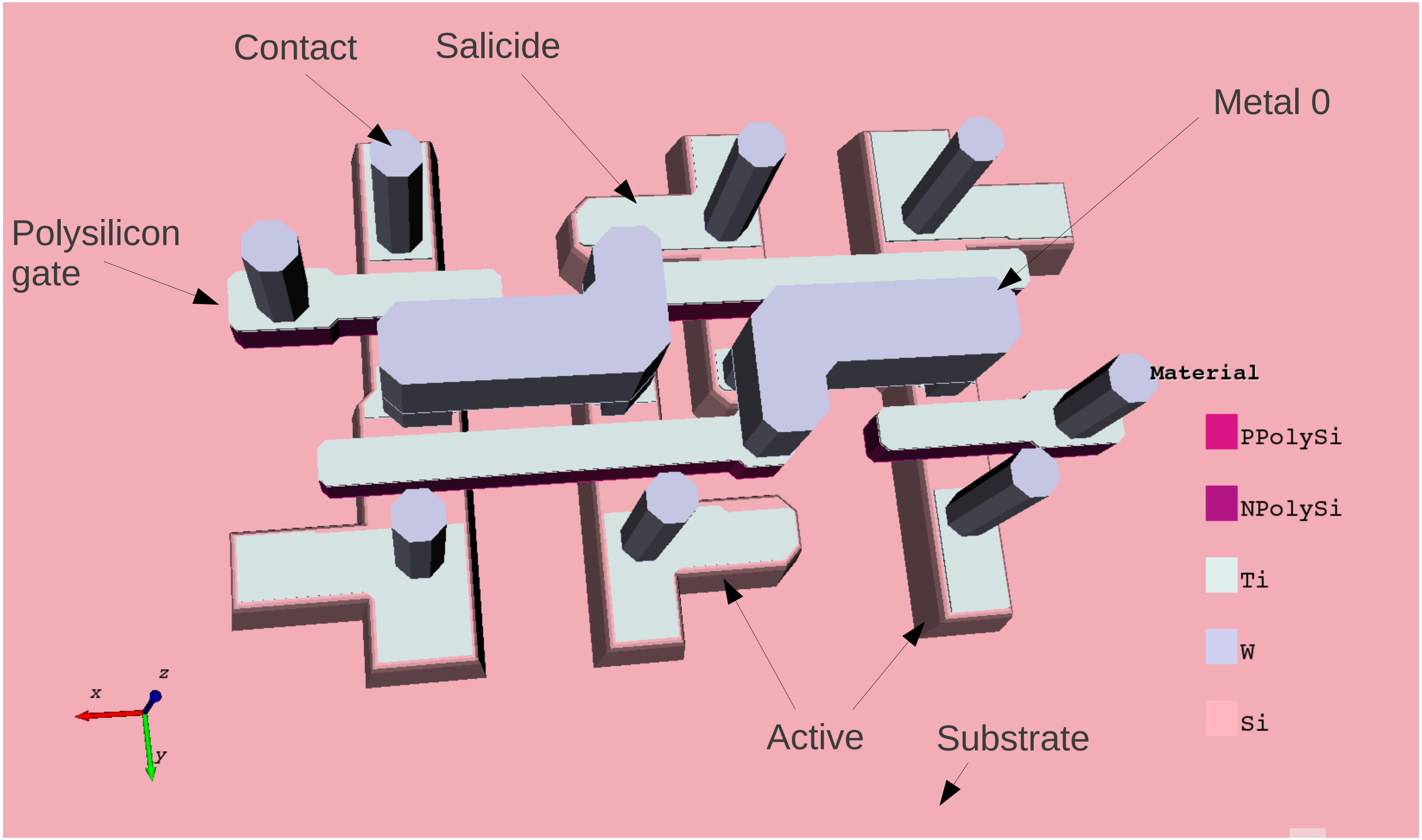
Metal 1: word line



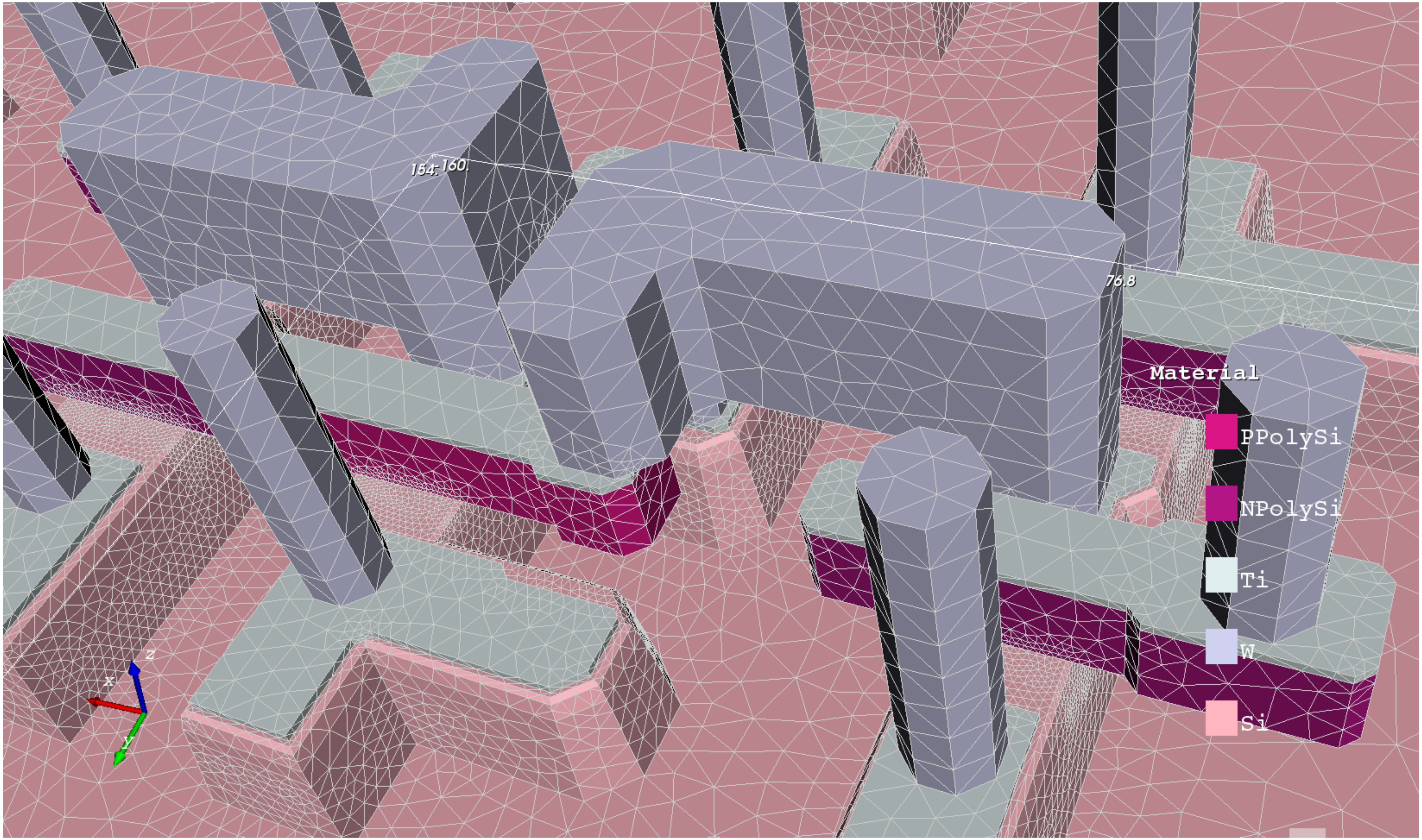
Structural Analysis: Extracted Layout



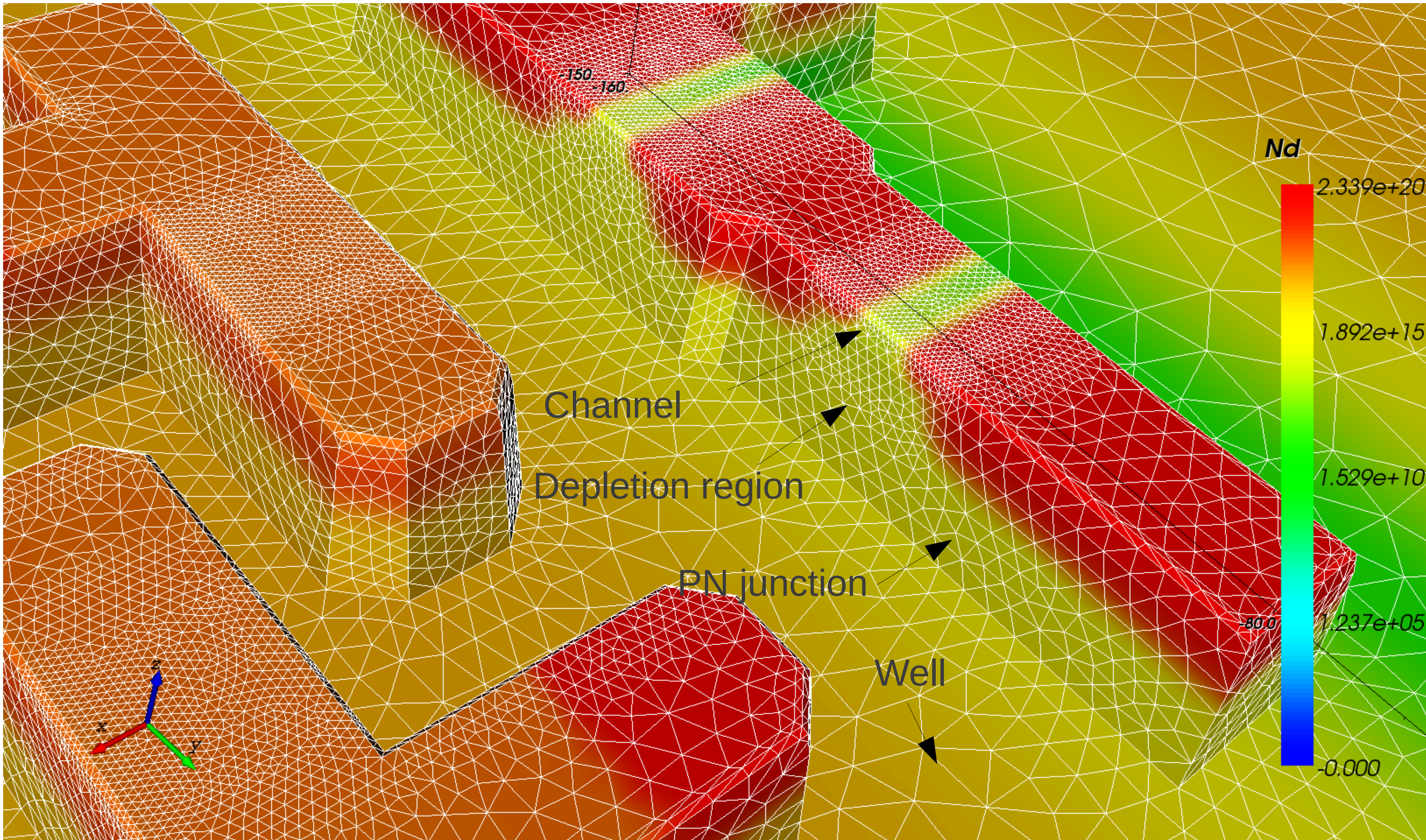
3D Modeling: SRAM cell



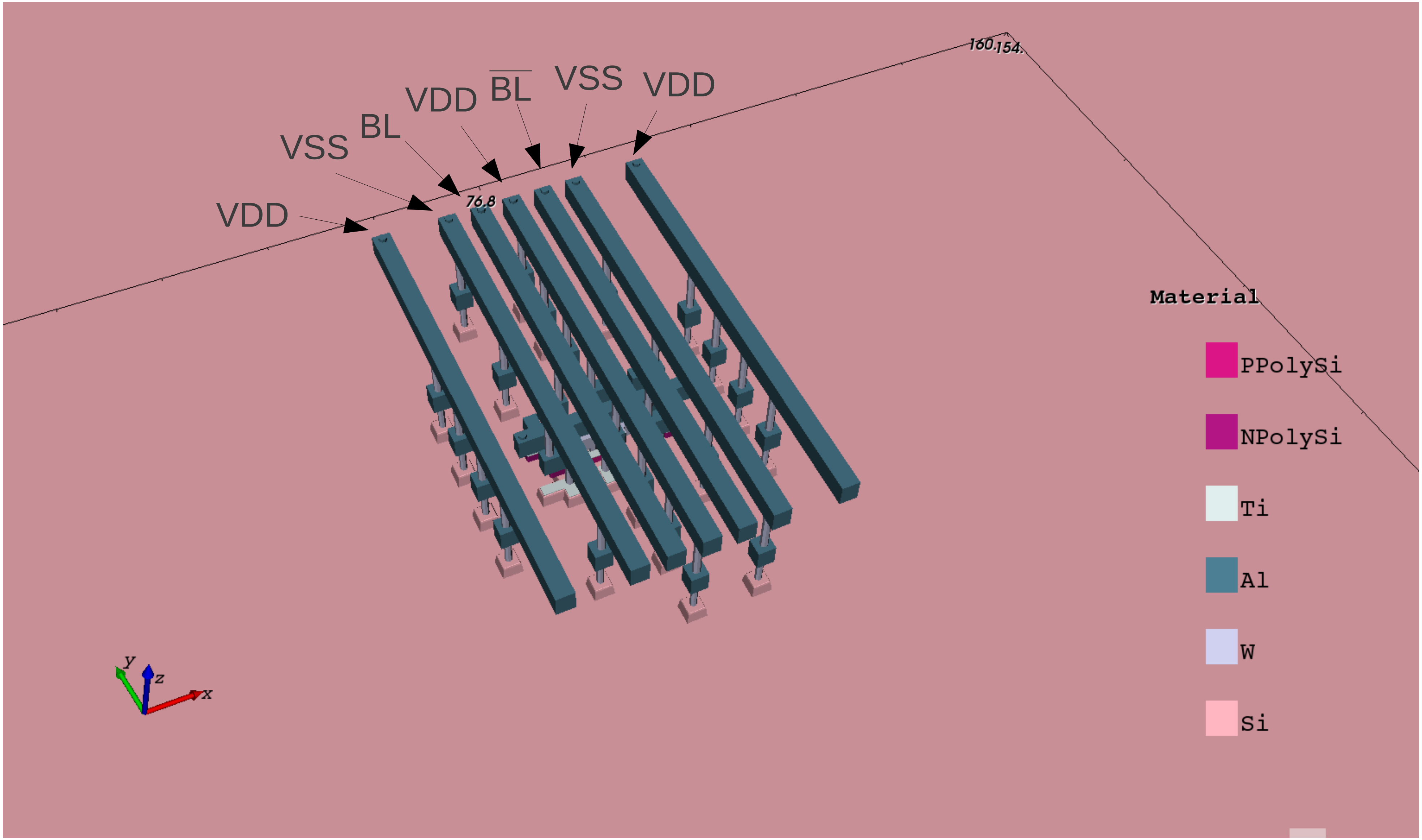
3D Modeling: Structural Details



3D Modeling: Doping Profile/Mesh

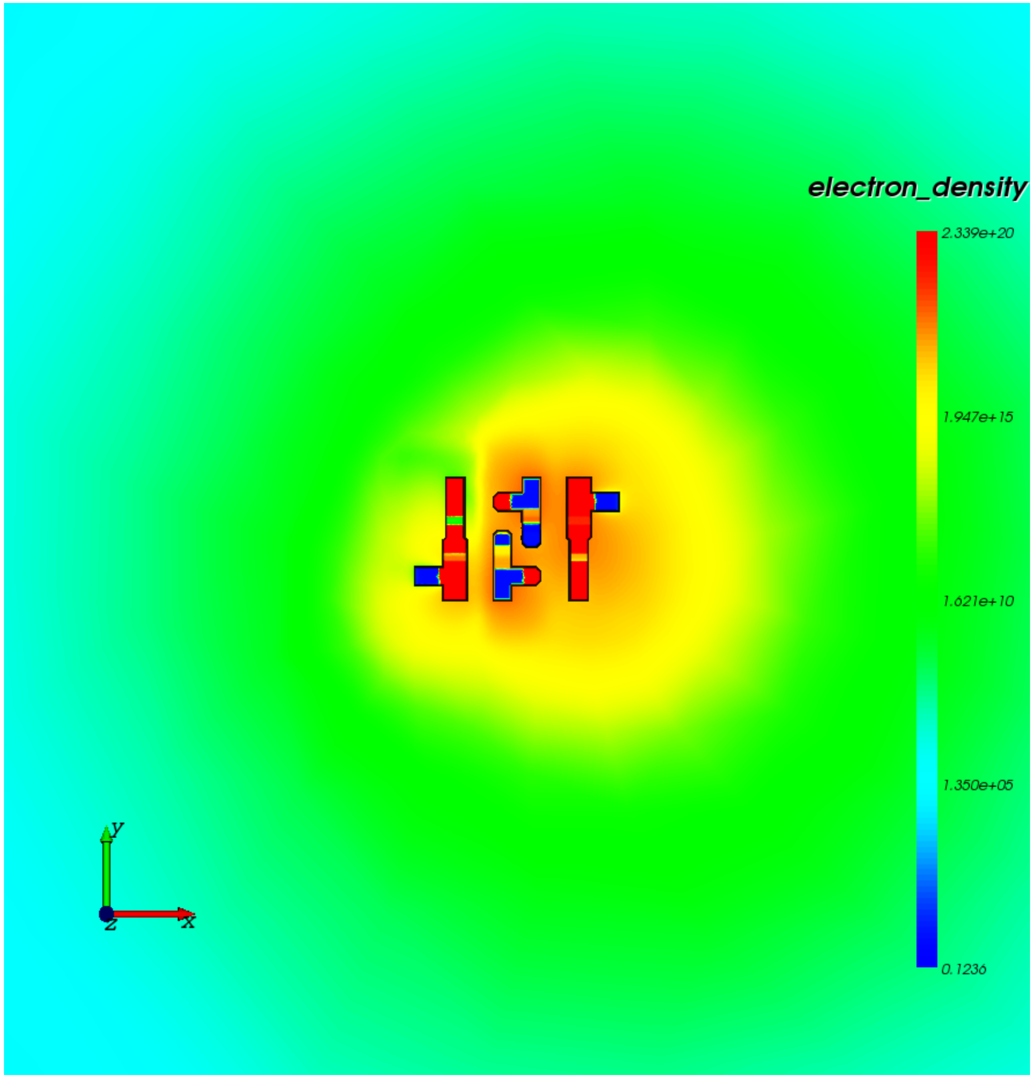


3D Modeling: Interconnects/Well Contacts



3D Modeling: Well and Well contacts

Cu^+ 161MeV, t = 207 ps



Rejected Model 1:

- Totally ignore well contacts outside this cell

Inconsistent with real device:

- Latch-up is seen
- Over-estimated SEU cross-section

Causes of inconsistency

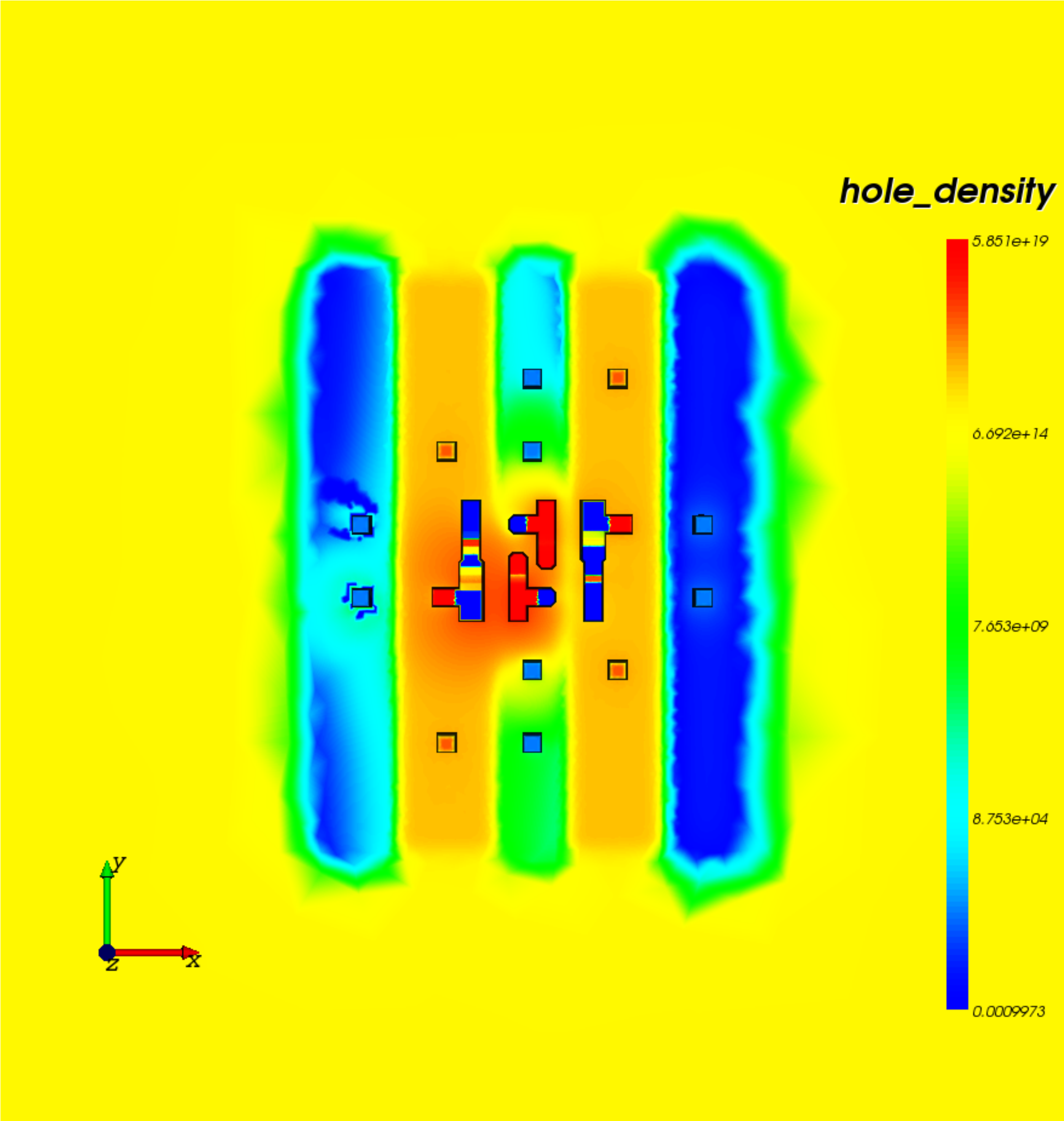
• Large amount of e-h pairs under high LET particle strikes

• Well-contacts within cell not sufficient to remove carriers.

• Well potential collapses, causing latch-up

3D Modeling: Well and Well contacts

Cu⁺ 161MeV, t = 381 ps



Rejected model 2:

- Increased well area
- Several well contacts in adjacent cells
- Latch-up eliminated

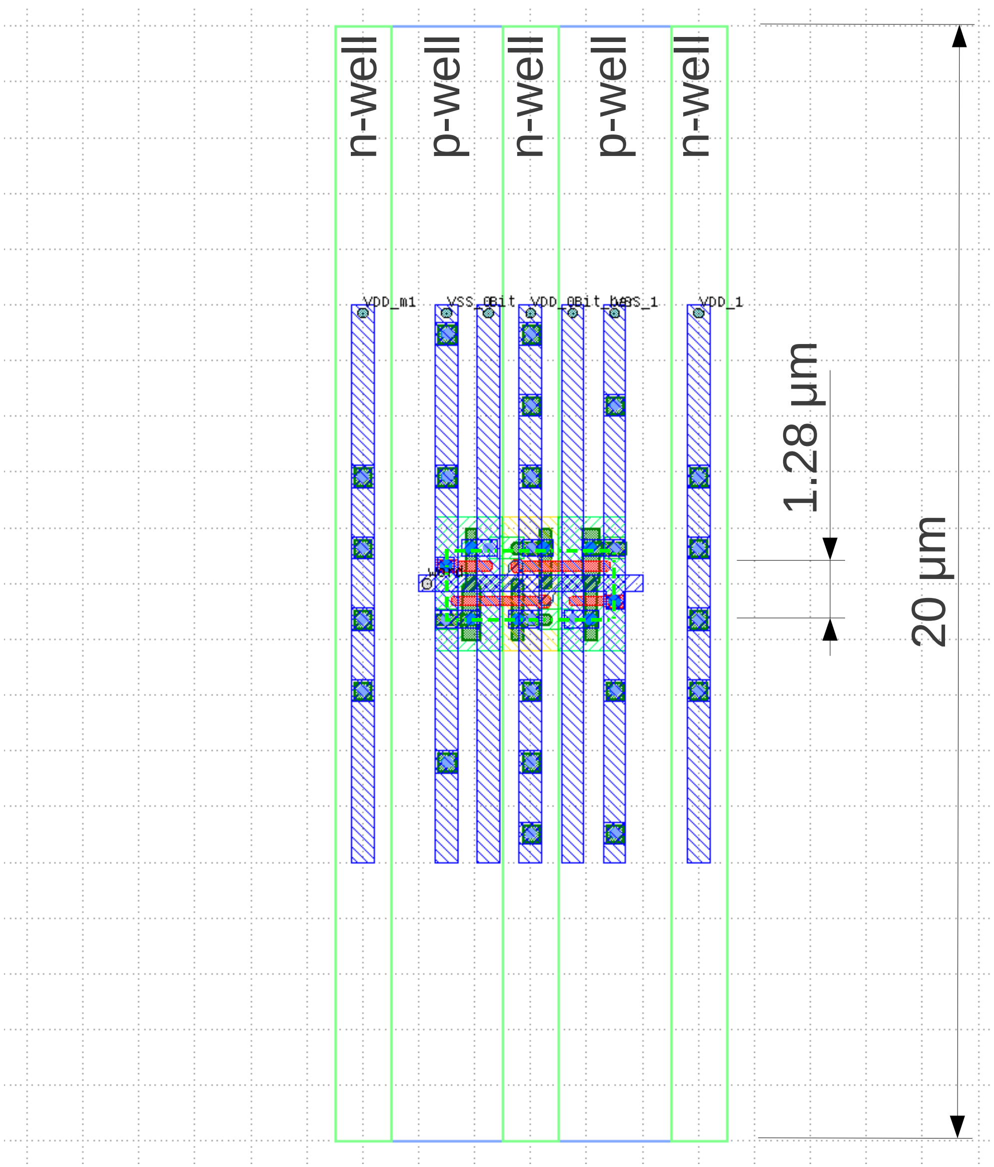
Still inconsistent with real device:

- Over-estimation of SEU cross-section

Causes of inconsistency

- Well area not large enough, carriers fill up the well
- Too few well contacts

3D Modeling: Well and Well contacts

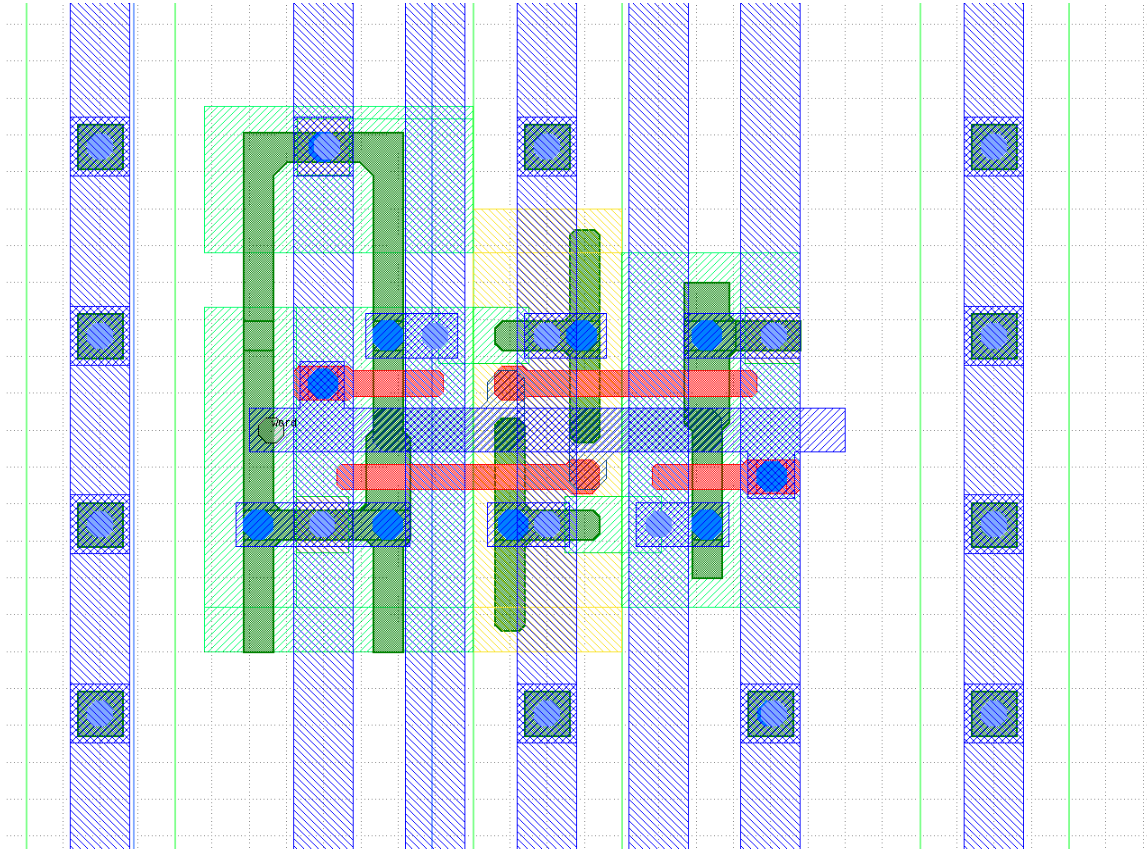


Adopted Model 1:

- 20 μm well
- Extra n-well on the left/right
- Extra well contacts

- Correctly describes the carrier collection by well-contacts

3D Modeling: Well and Well contacts

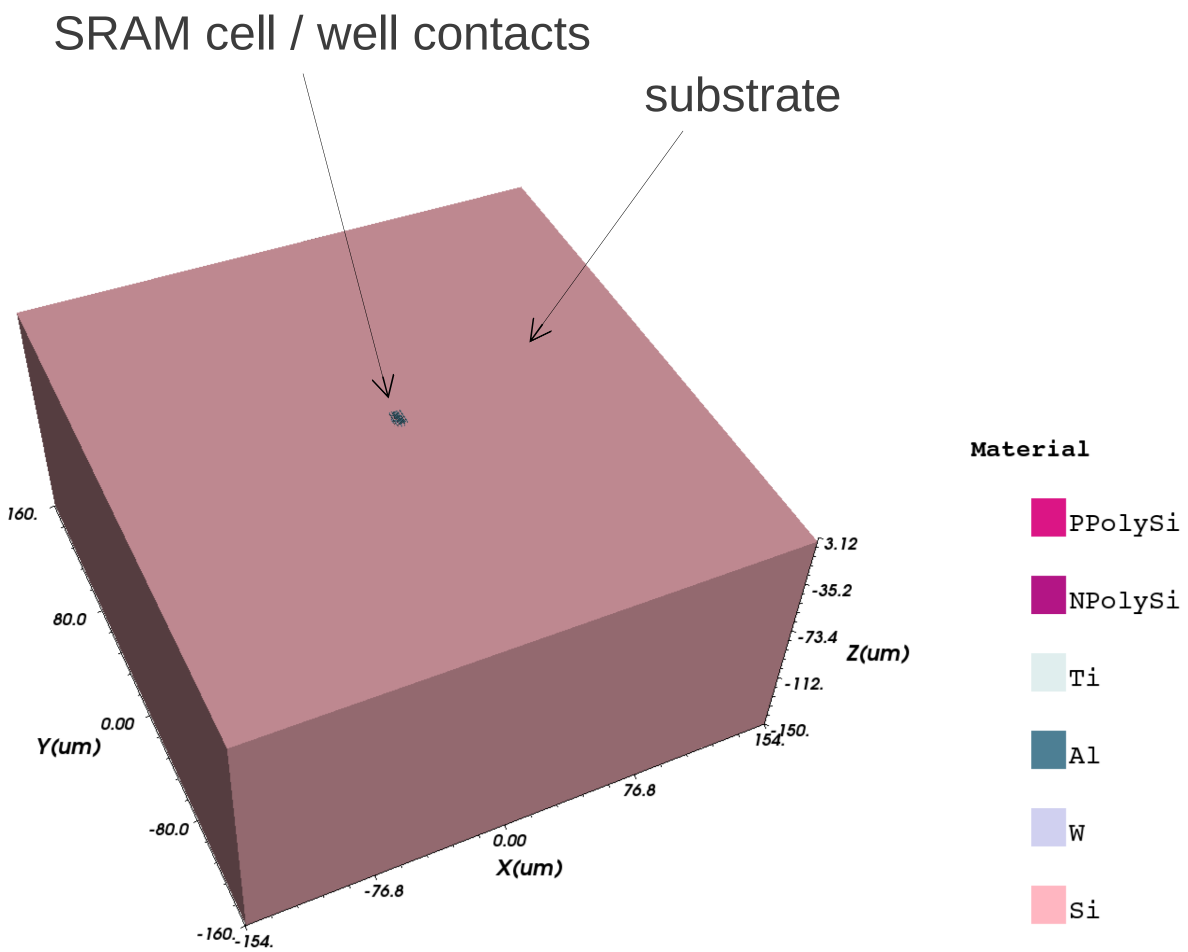


Adopted Model 2:

- For high-LET particles
- Need to consider carrier collection by adjacent active region/circuit nodes
- Extra active region and contacts

- Correctly describes the carrier collection by adjacent actives

3D Modeling: Substrate



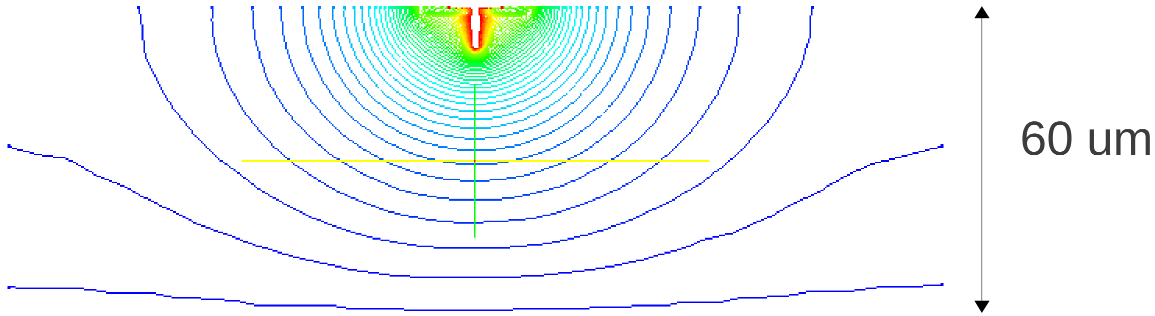
Actual chip size

- 8.2 x 5.7 x 0.25 mm
- TCAD model of this size is impractical

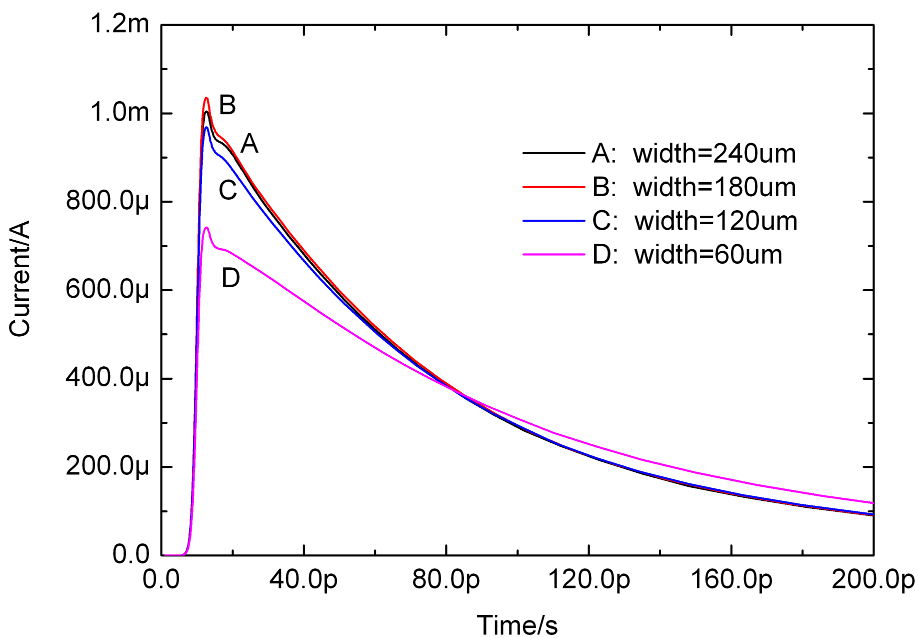
Rules for model sizing:

- Thickness > max. particle range
- Width > 2 x Thickness
- Compensate any reduced thickness with a series resistance

3D Modeling: Substrate

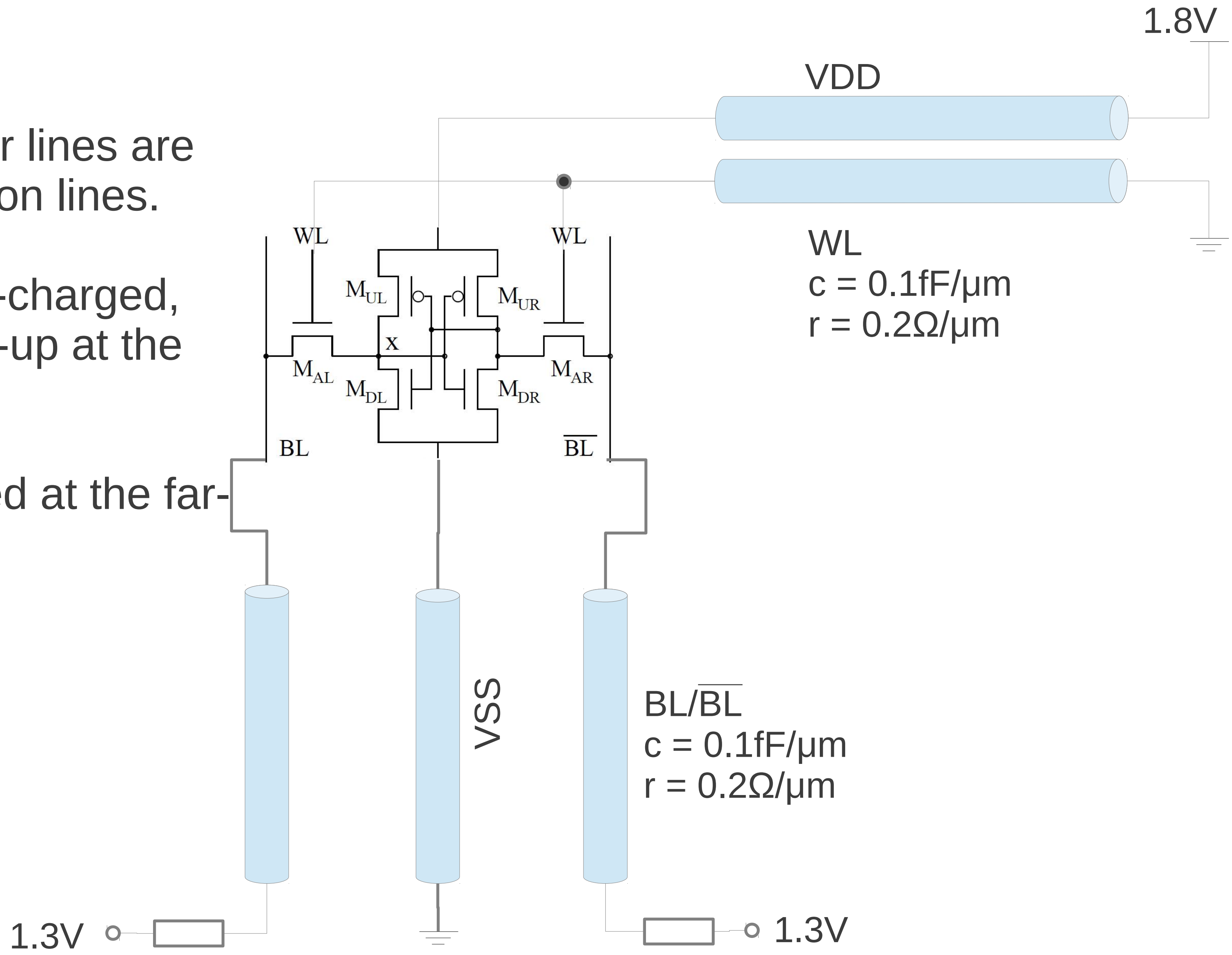


- As current flow into the substrate, it spreads out
- Truncating the width of the substrate causes under estimation of the charge collection.
- Requirement: width > 2 x thickness



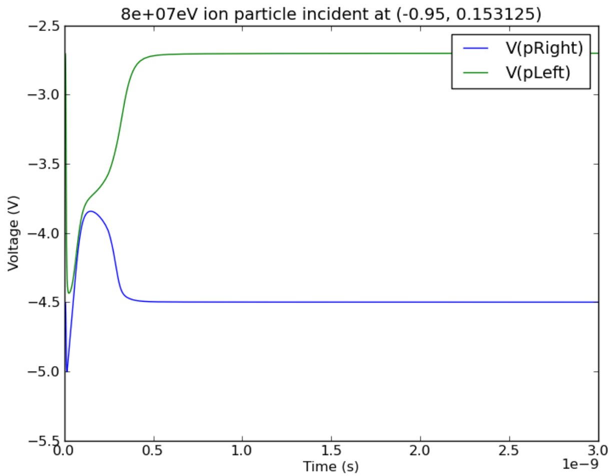
Peripheral Circuit Modeling

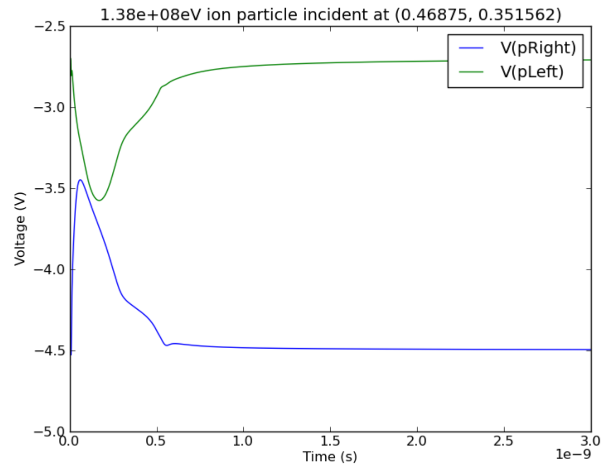
- BL, WL, Power lines are RC transmission lines.
- BL/$\overline{\text{BL}}$ are pre-charged, with weak pull-up at the far-end
- WL is grounded at the far-end

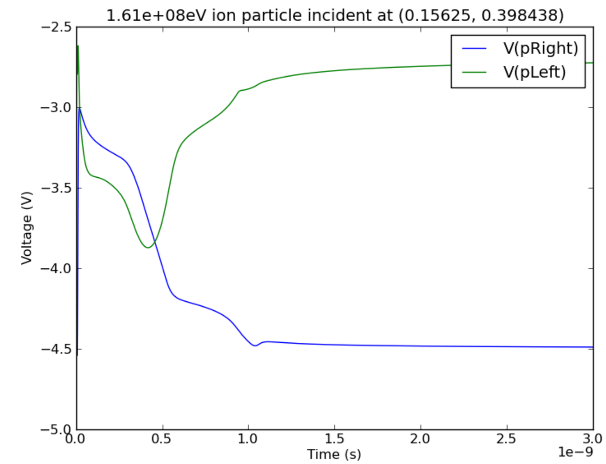


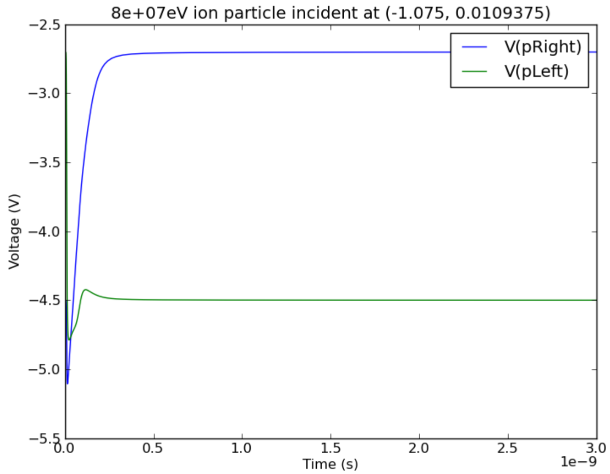
Transient Waveforms: Various Circuit Response Mechanisms

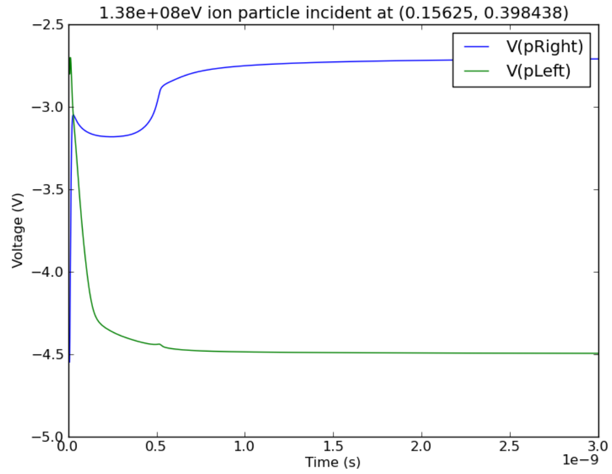
Waveform of left/right circuit nodes

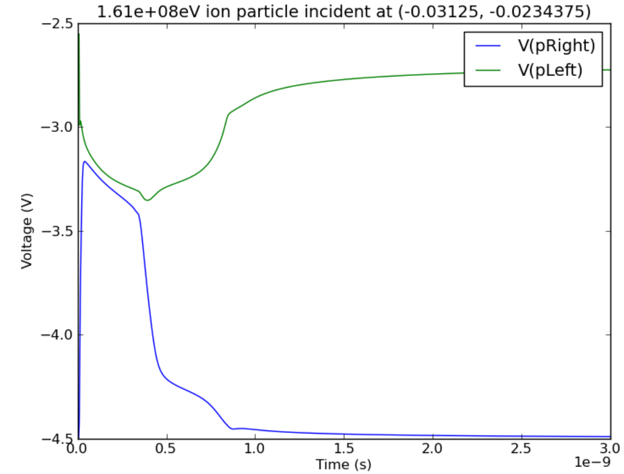






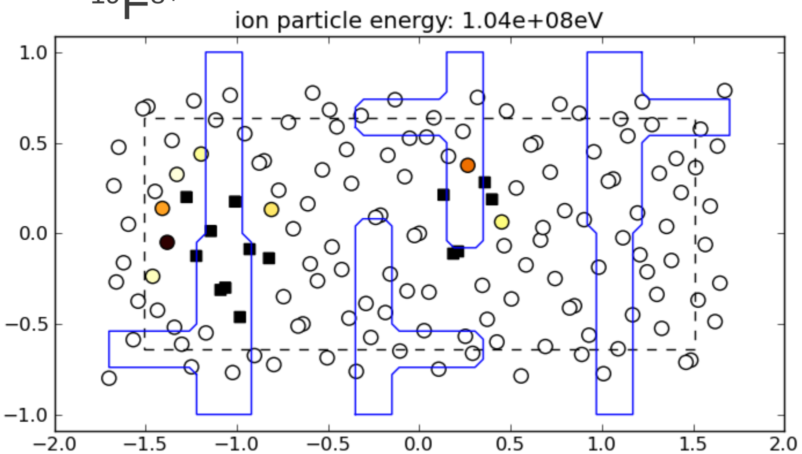




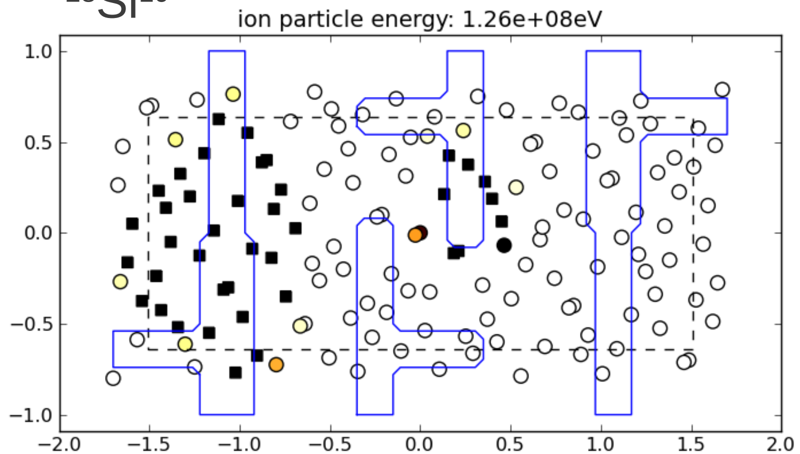


SEU Flip Event Maps

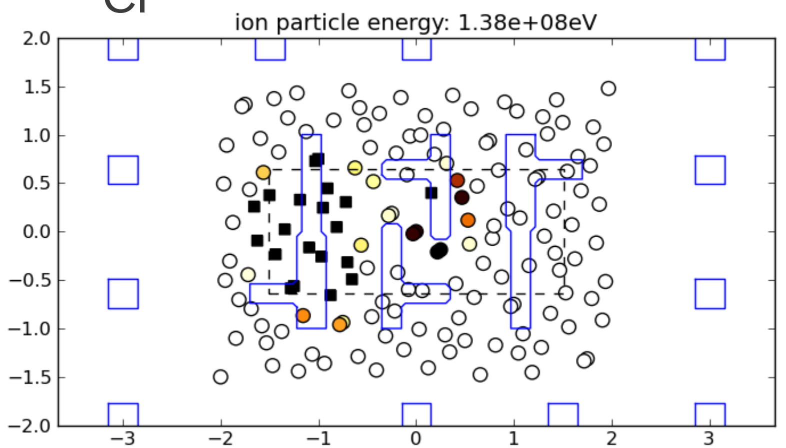
$^{19}F^{8+}$



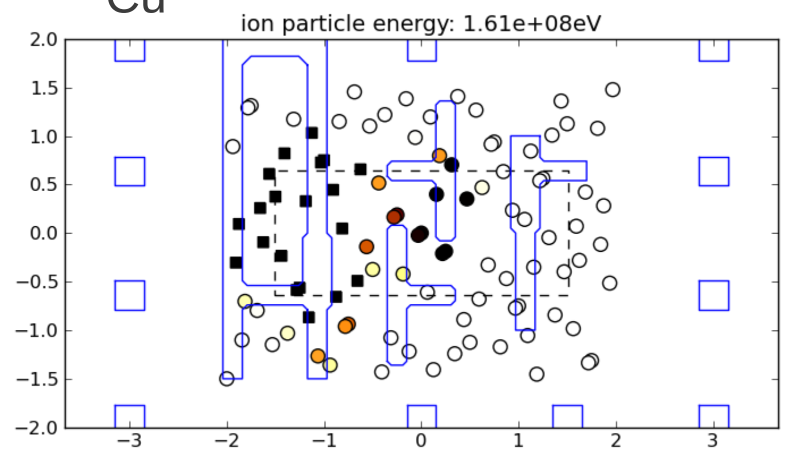
$^{28}Si^{10+}$



$^{35}Cl^{11+}$



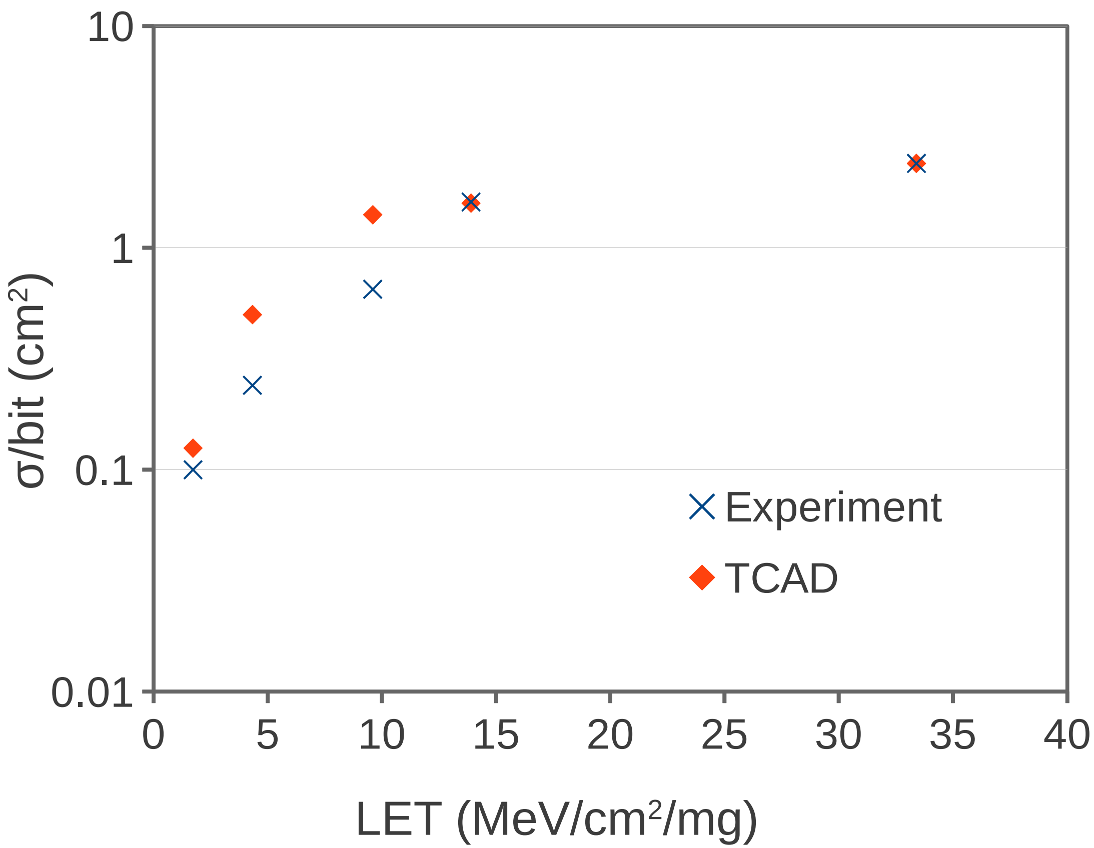
$^{63}Cu^{13+}$



Outline

- Components in the framework
  - 3D modeling: Gds2mesh
  - Geant4-based particle simulator: GSeat
  - TCAD device simulator: Genius
  - Statistical sampling: runSEU
- Applications
  - SEU Cross-section of a 0.18um SRAM: HM62V8100
  - Single-event block upset in 90nm SRAM: CV62126EV
  - Extension to Multiple-Composite-Sensitive-Volume model

SEU Threshold: Small-Probability Events



When simulating small SEU cross-section (near threshold)

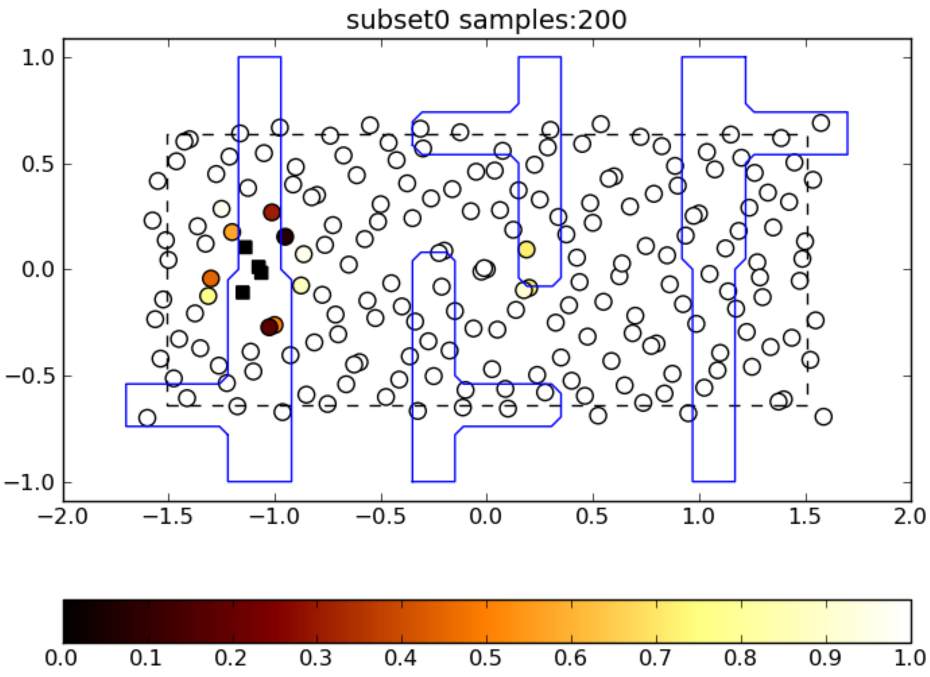
- Few flipping events
- High statistical variance
- Needs a large number of samples

Solution:

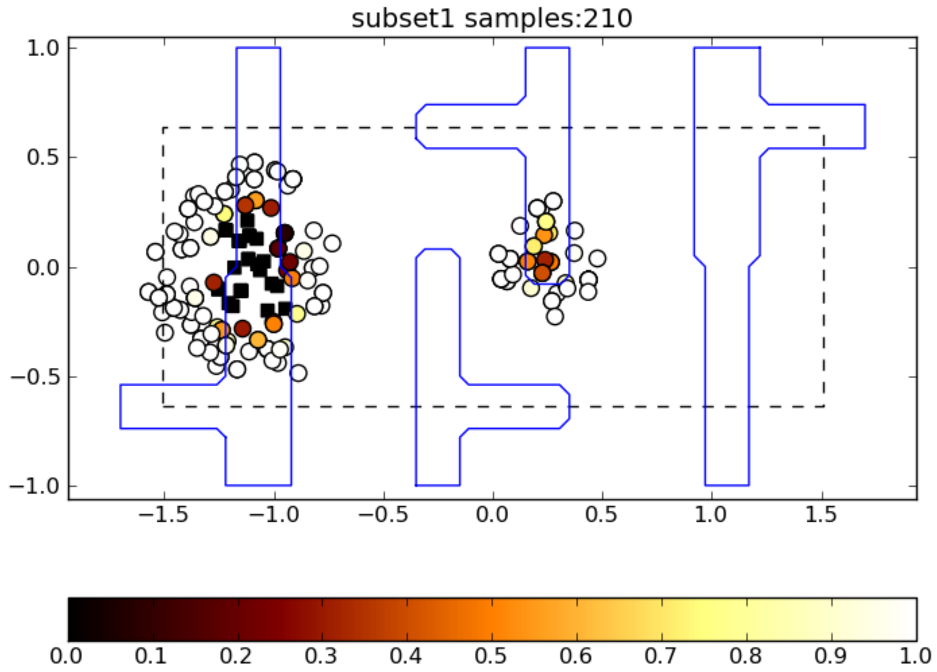
- Importance sampling with Subset Simulation

Subset Sampling

$^{12}C^{6+}$ Subset 0: Simple MC sampling



Subset 1: Importance sampling

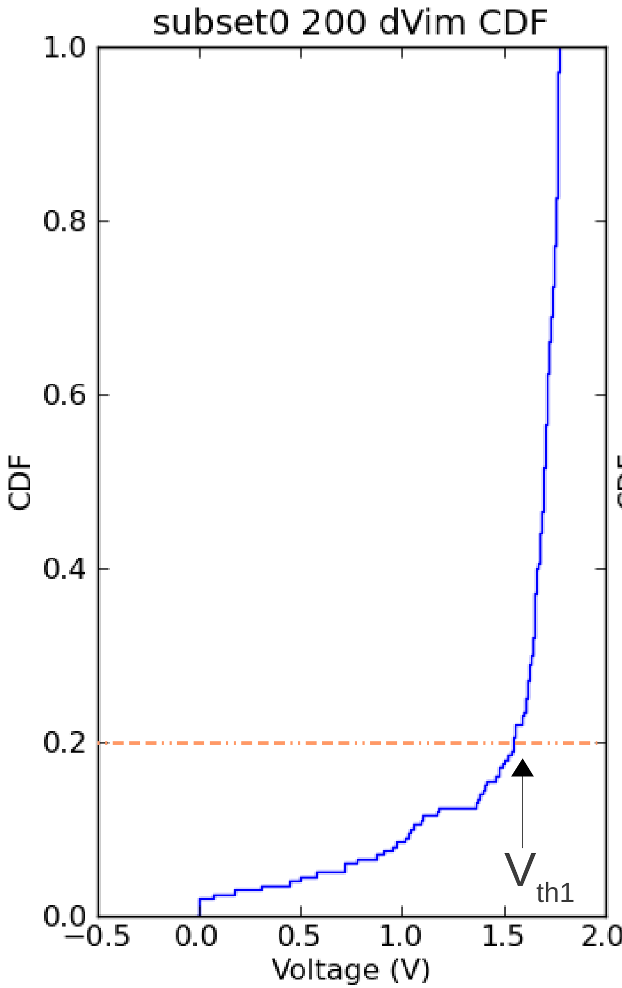


C. Shen et al, RADECS 2012

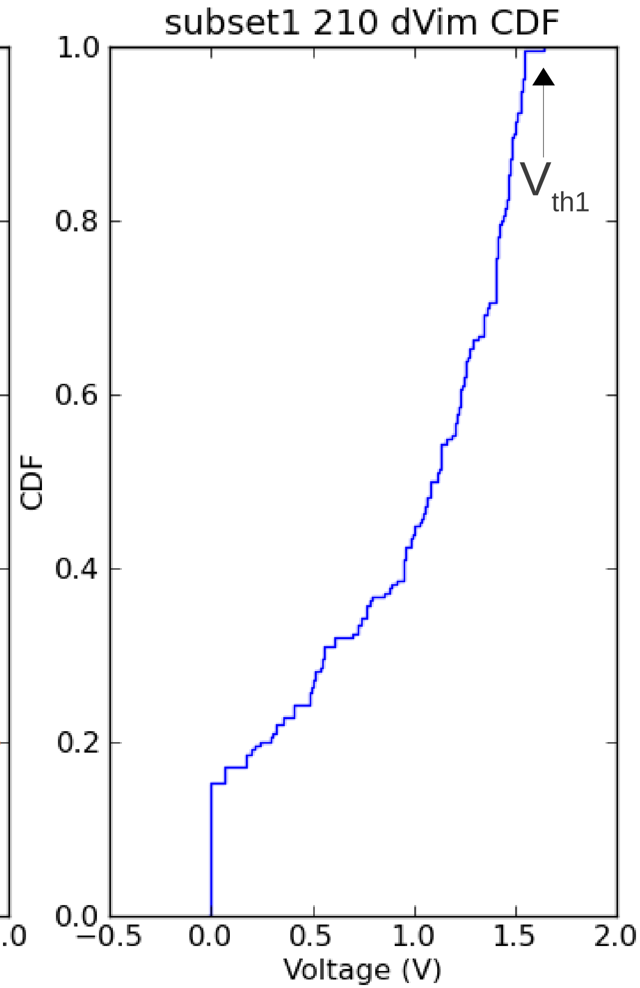
Subset Sampling

CDF of Minimum difference between left/right circuit nodes (ΔV)

Subset 0:
contains all samples



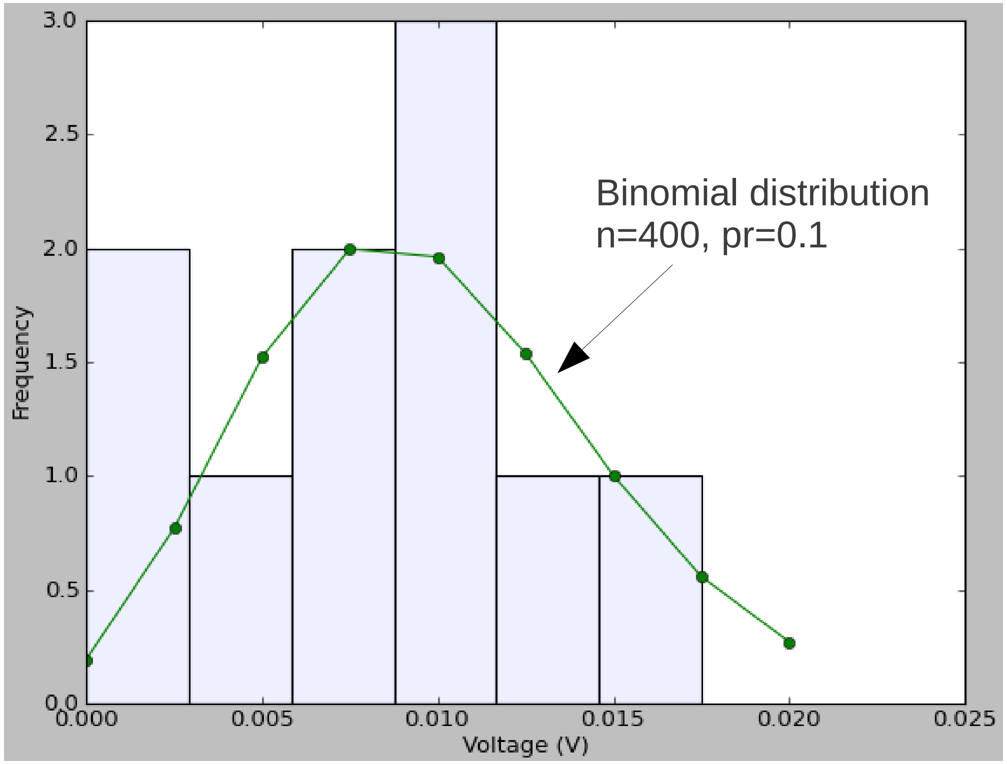
Subset 1:
Contains only samples with ΔV < 1.55 V

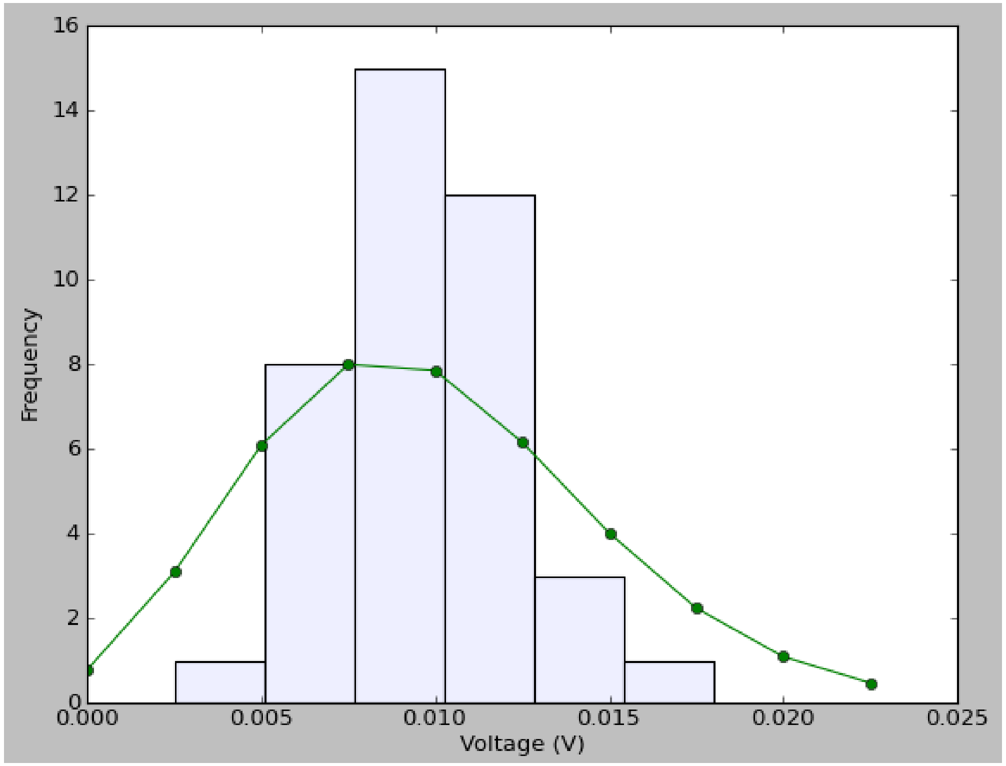


Improved Convergence

10 Plain Monte-Carlo Runs
Sample size: 400
Results show large variance

40 Subset Simulation Runs
TCAD runs: <400
Much less variance





Performance and Cost

- Computing Environment
  - Commercial HPC service
  - Parallel computation on 10 computing nodes
  - All work complete within 1 week
    - Including debugging the mask and 3D model
- Costs

Machine time (core-hour)	16,200
Power consumption (KWh)	1,350
Commercial HPC service charge	~ US$ 1,000

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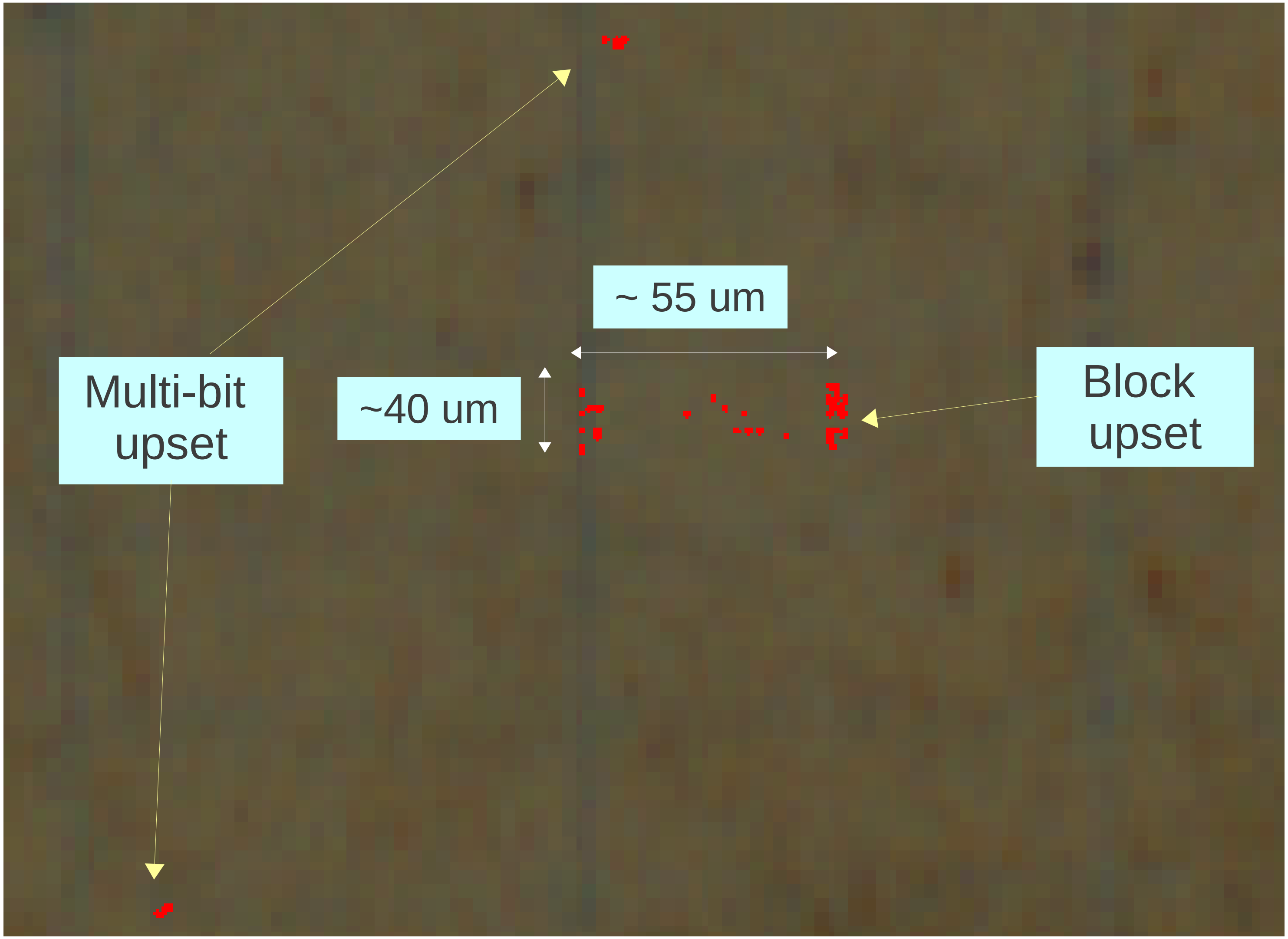
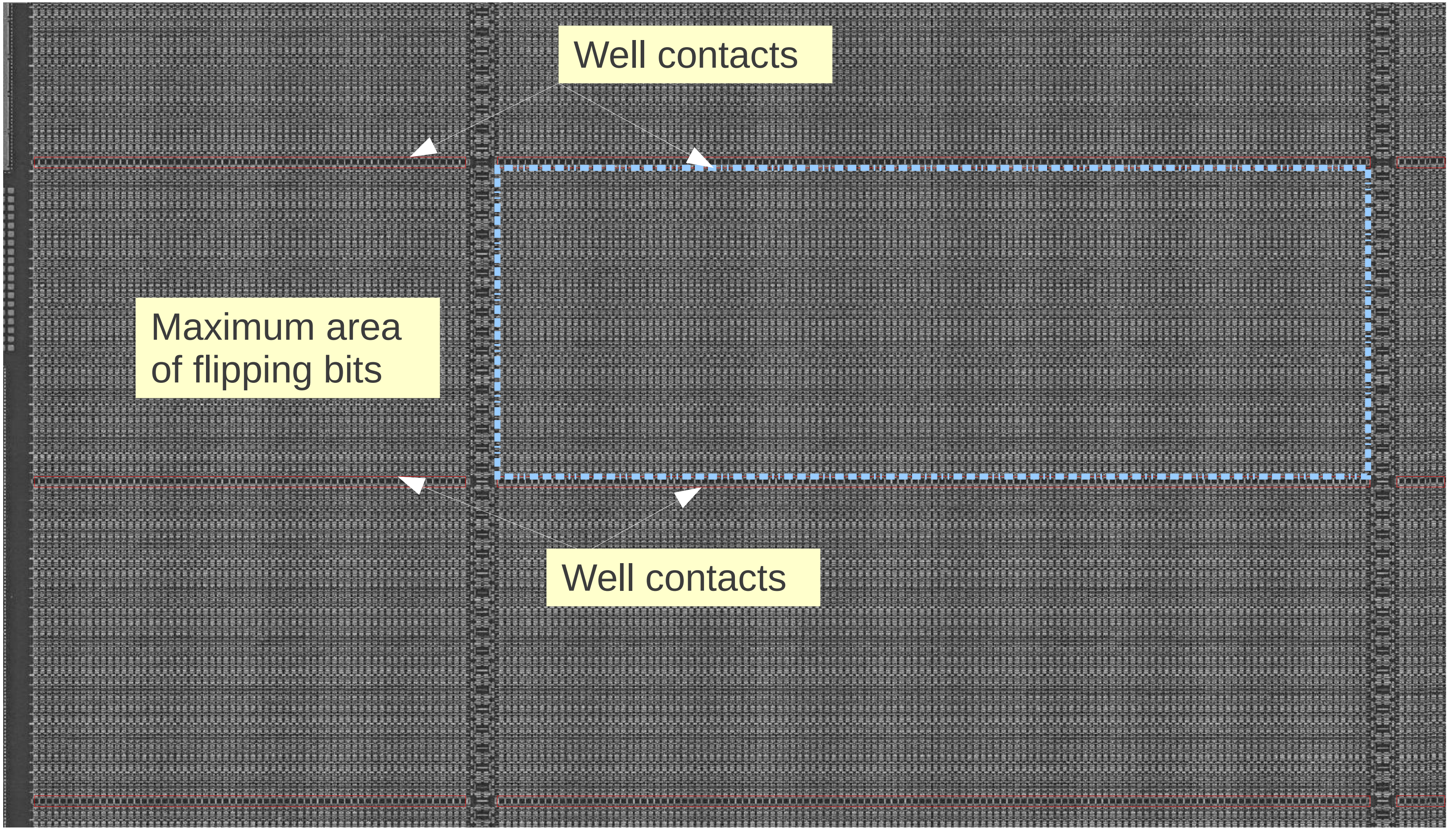
Single Event Block Upset

- Cypress CV62126EV, 90 nm, 1MBit, “SEL immune”
- Mapping logical address of flipped bits to physical location on chip

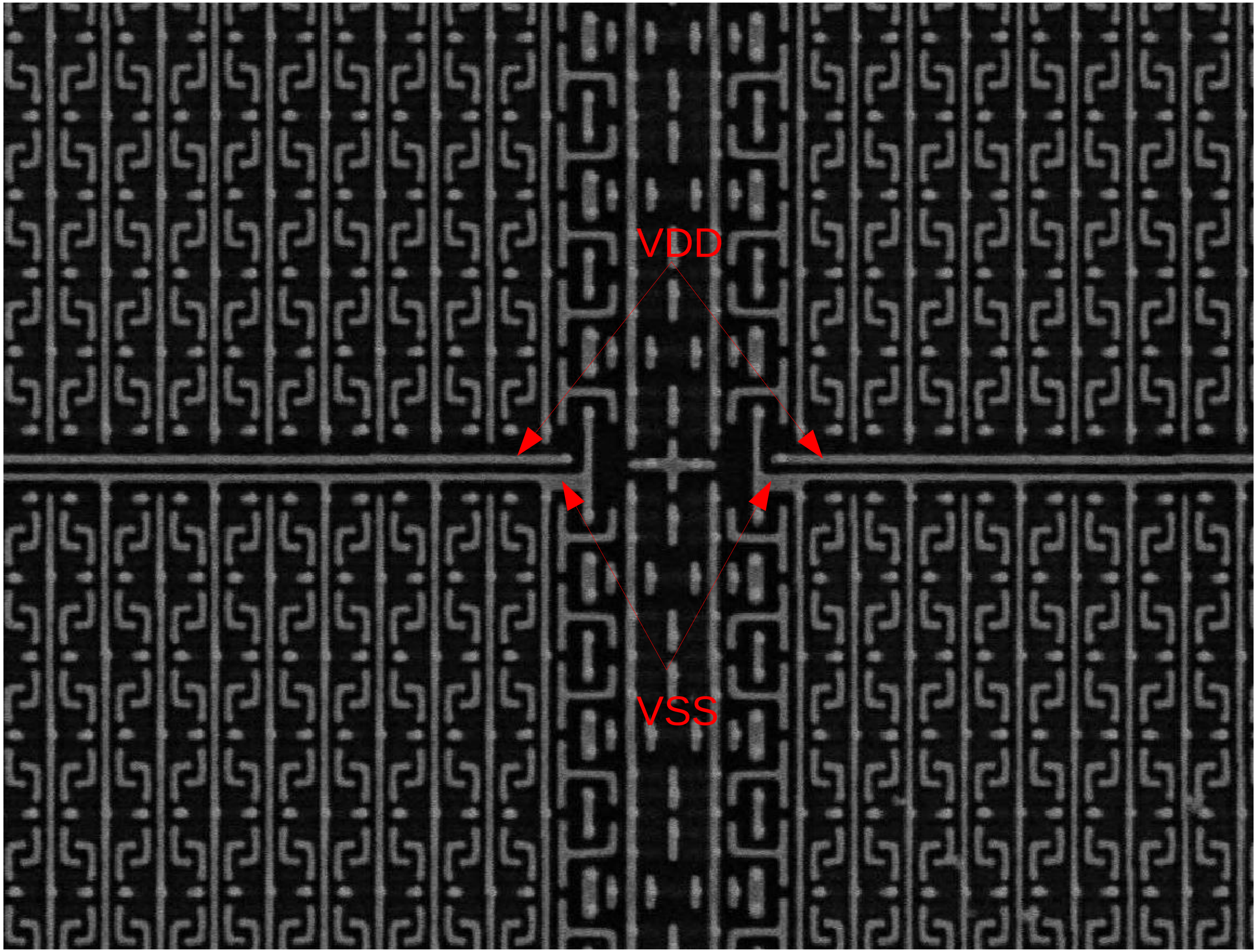


Single Event Block Upset



Suspected Reason

Weak VDD supply to N-Well: 108um, 90 Ohm



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On-Orbit SEU Rate Prediction

- Fully-Physical Simulation too slow
  - A fast SEU assessment tool needed
    - Train once, using ground test results
    - Predict SEU rate in different radiation environment
- IRPP
  - Ground test → fit to Weibull curve (training)
  - Integral LET spectra → SEU rate (predicting)
- Composite Sensitive Volume
  - Ground test → extract sensitive volume / sensitivity (training)
  - MRED → effective collected charge (predicting)
- Can be formulated as a machine learning problem
  - Support Vector Machine is the machine-learning of our choice

SEU Rate Prediction as a Classification Problem