Final Presentation

Network on Chip (NoC) for Many-Core System on Chip in Space Applications

December 13, 2017

COBHAM
Cobham Gaisler AB

RECORE

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NoC round table

- Network-on-Chip (NoC) round table co-organized by ESA and CNES in 2009:
  - future SoC developments for space applications would benefit significantly from the use of NoC technology;
  - no NoC IP was generally available for the space community without entailing specific modifications or adaptations.

Contract details

- ITT No.: AO/1-8166/14/NL/LF
- ESA Contract No.: 4000115252/15/NL/LF

- Prime Contractor: **Recore Systems BV**, The Netherlands
- Sub-Contractor: **Cobham Gaisler AB**, Sweden

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Our objectives

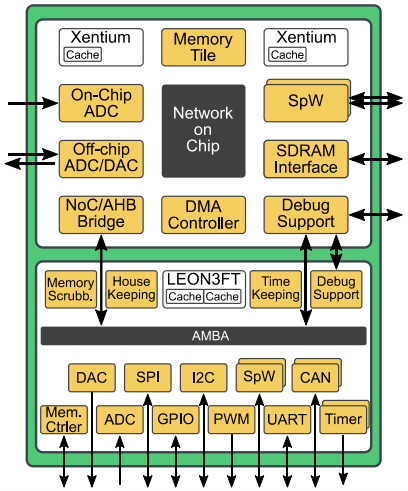
- To propose and define Network-on-Chip technology;
  - To propose hardening of the proposed NoC technology;
  - To implement the NoC IP in VHDL (for SoC design);
  - To implement functional SystemC (for early software development);
- To demonstrate the NoC IP capabilities implementing a reference design (use case);
- To validate the NoC IP using rad-hard CMOS target technology.

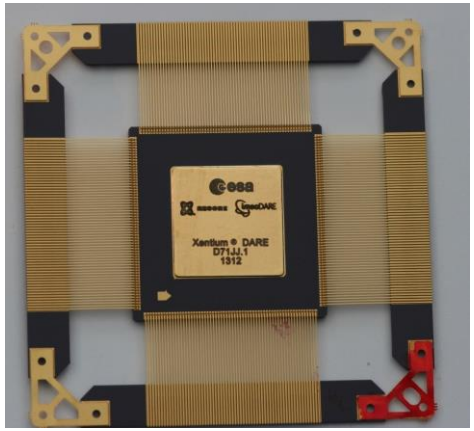
Results

- NoC IP technology for future System-on-Chip (SoC) available in ESA's IP core portfolio for the European space industry; and
- NoC IP validated with state-of-the-art space proven IP components for hardened ASIC process technologies.

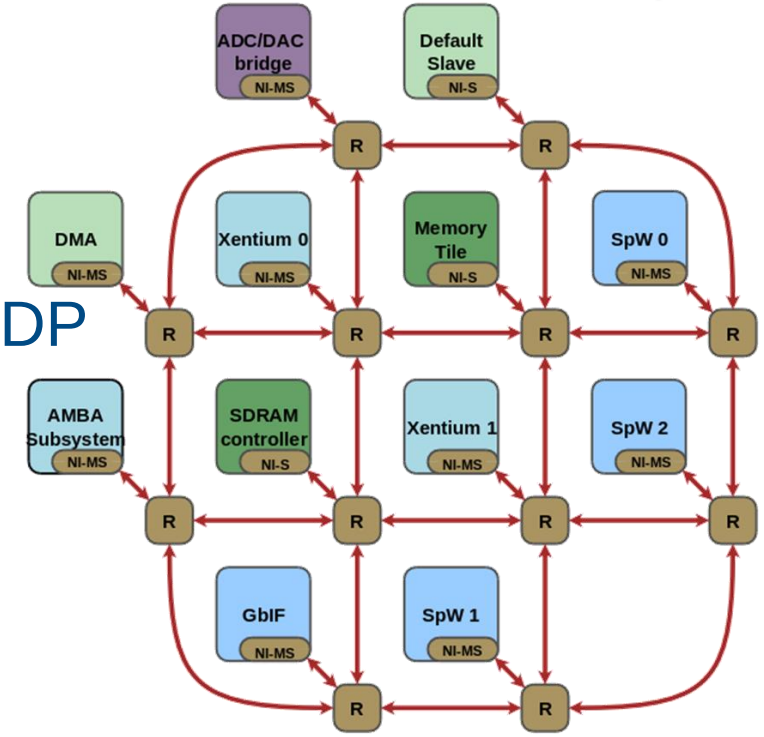
Baseline Network-on-Chip

Recore's NoC already used in MPPB, XentiumDARE and SSDP





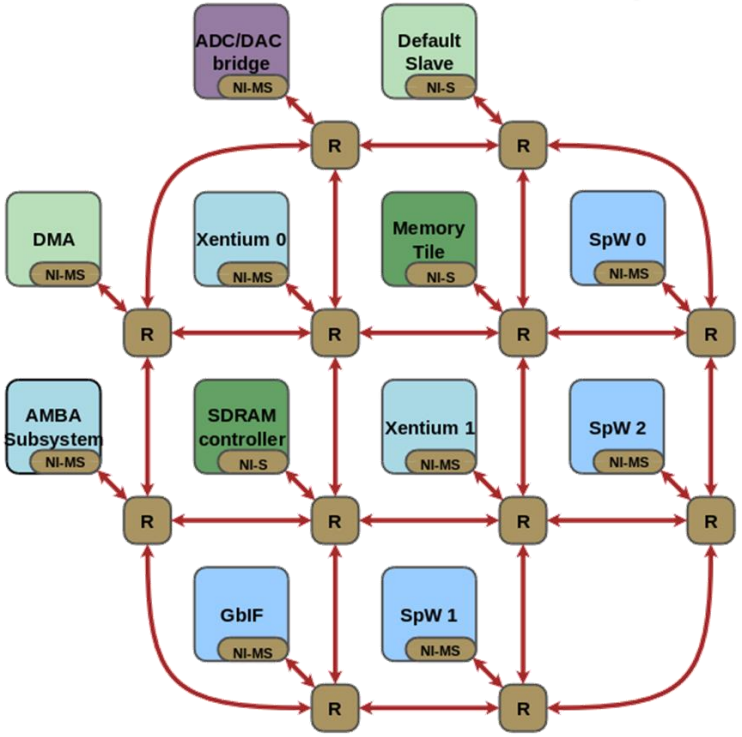
Baseline NoC (1/2)



- Used in MPPB, XentiumDARE, SSDP

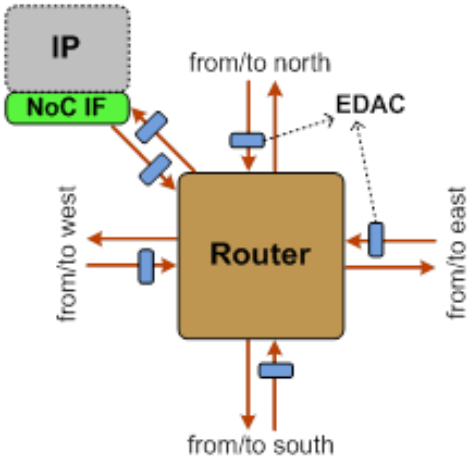
- Packet-switched routing
- 5 port routers
- 4 services, priority based
  - for throughput and latency guarantees
- Memory mapped communication protocol layer
- X-Y routing
  - deadlock free
  - design-time layout of tiles based on estimated traffic load

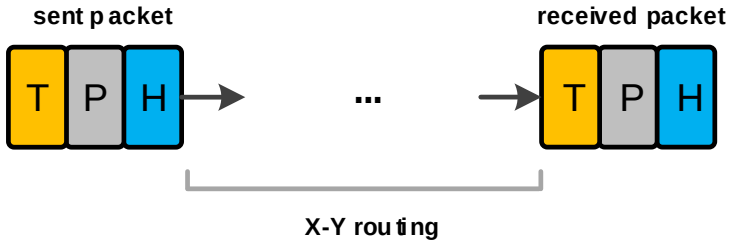
Baseline NoC (2/2)



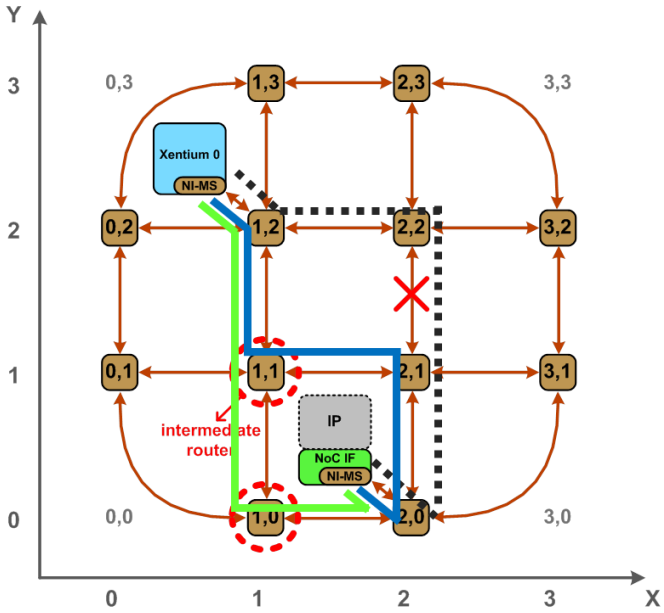
- Before this activity:
  - NoC technology integrated and part of sub-system / SoC design
  - Fault-tolerance not integral part of NoC
- After this activity:
  - NoC IP available as stand-alone IP package
    - Including documentation, stand-alone testbench
  - Fault-tolerance improvements

Baseline NoC extensions

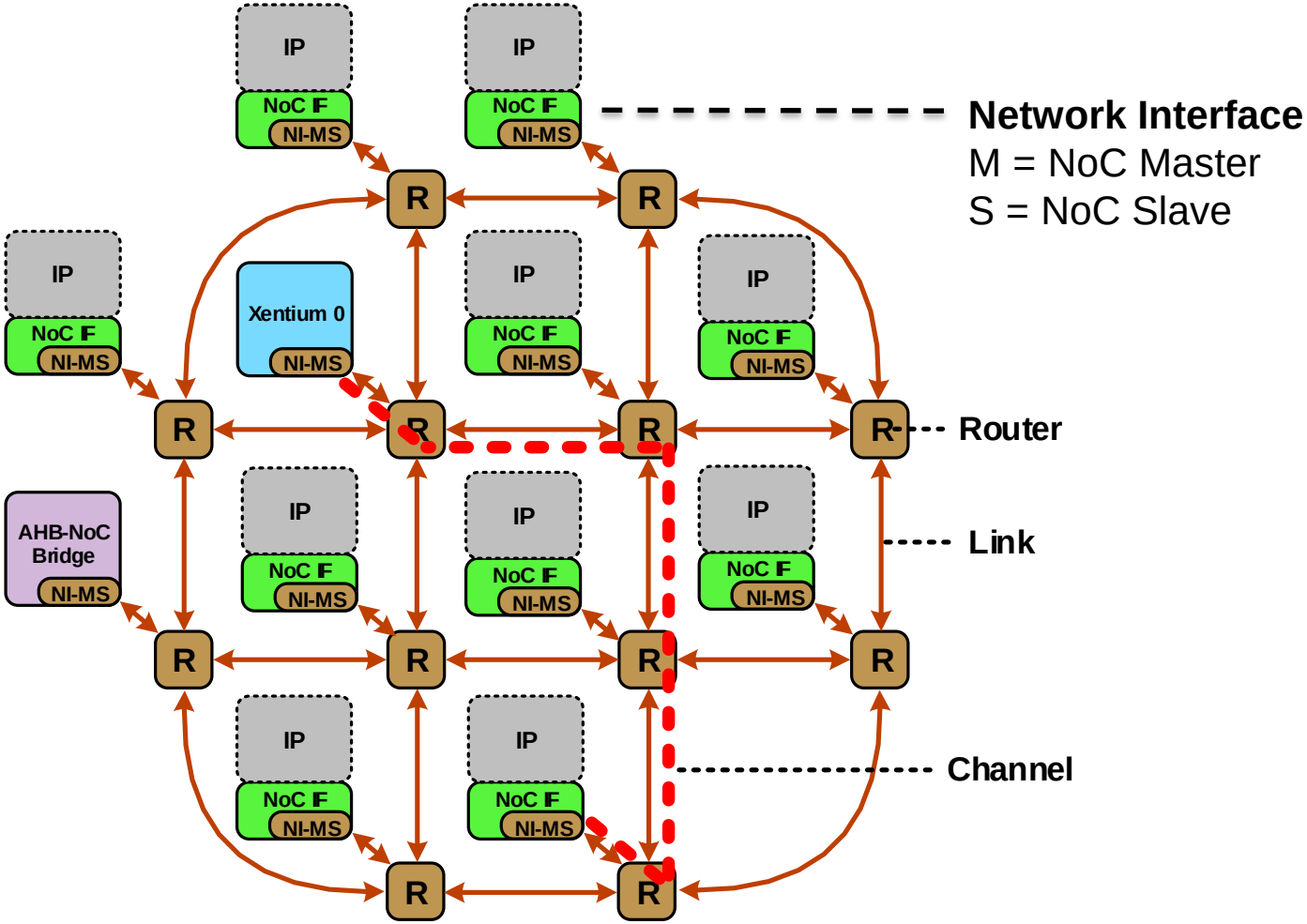




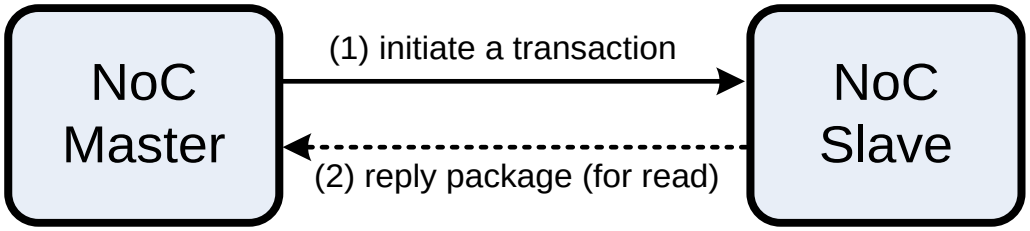
- Adaptive XY-routing to provide data rerouting in the NoC
- Flit-level flow control
- Enable the insertion of EDAC on data links to increase robustness of flits



NoC architecture

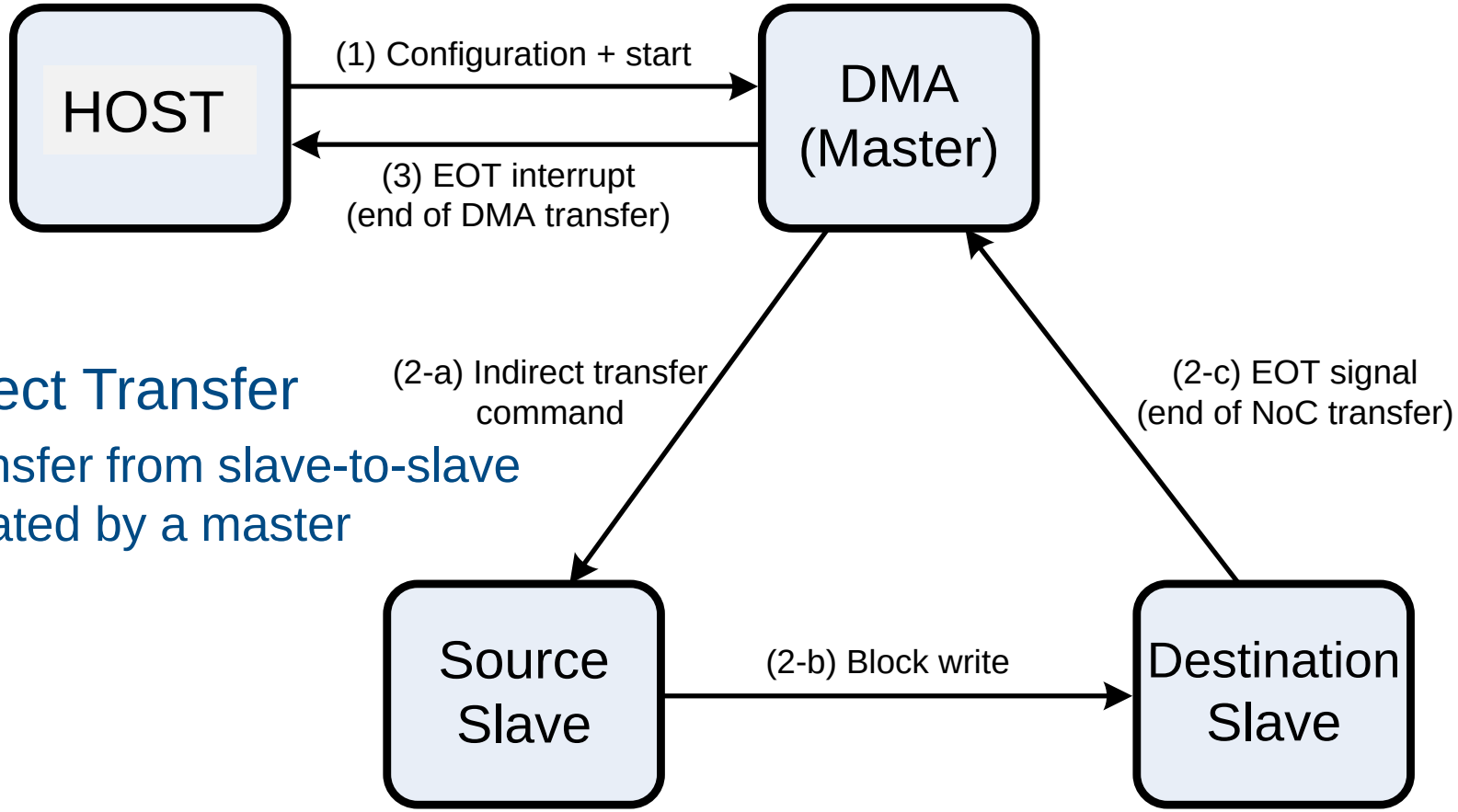


NoC protocol – Transactions (1/3)



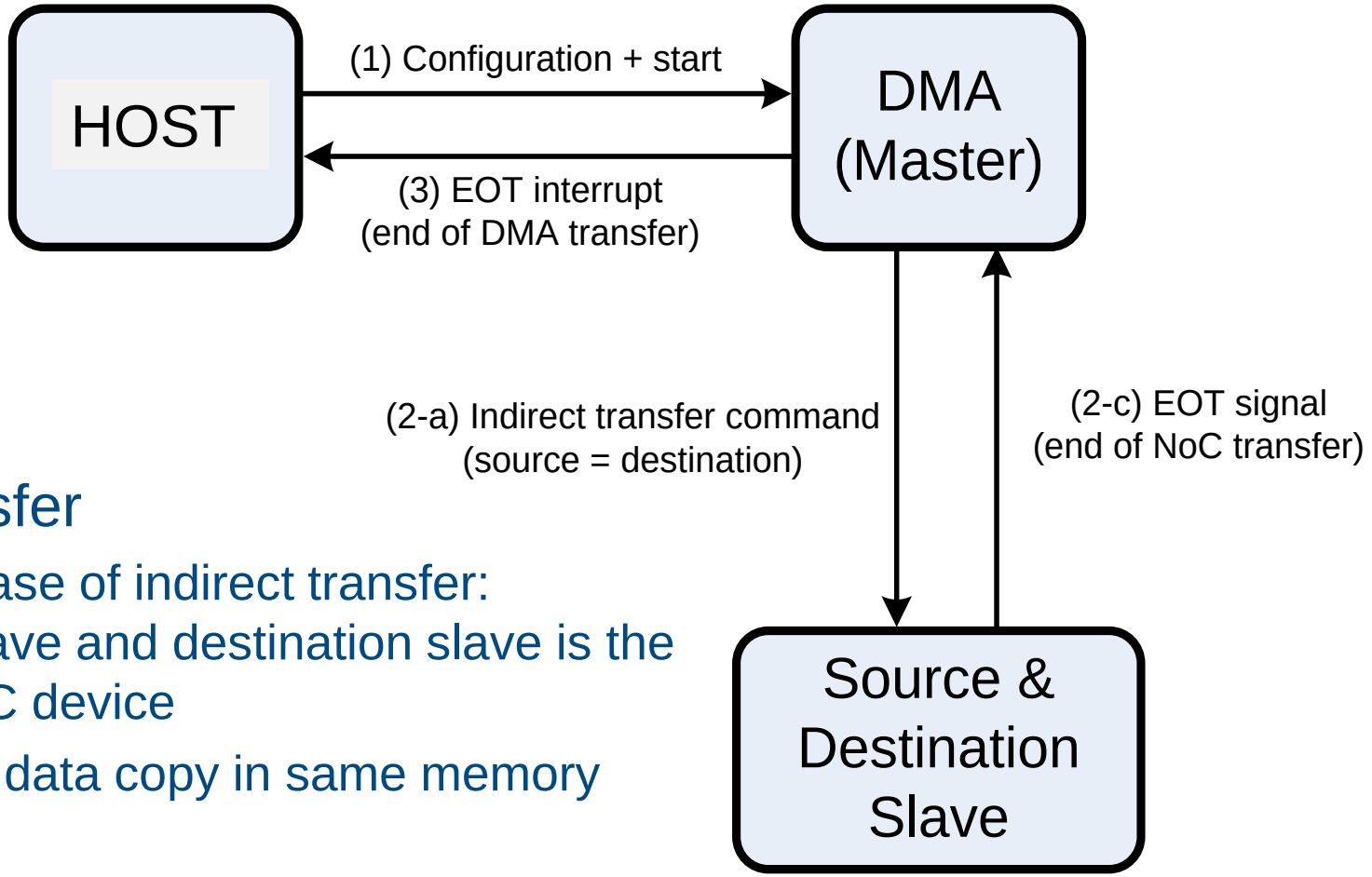
- Each transaction is built from a couple of flits of different types (e.g., header, payload, and tail):
  - Interrupt / Signaling
  - Single Read
  - Single Write (no Acknowledgement reply)
  - Block Read
  - Block Write (no Acknowledgement reply)
  - *Block Write with Interrupt reply*

NoC protocol – Transactions (2/3)



- Indirect Transfer
  - Transfer from slave-to-slave initiated by a master

NoC protocol – Transactions (3/3)

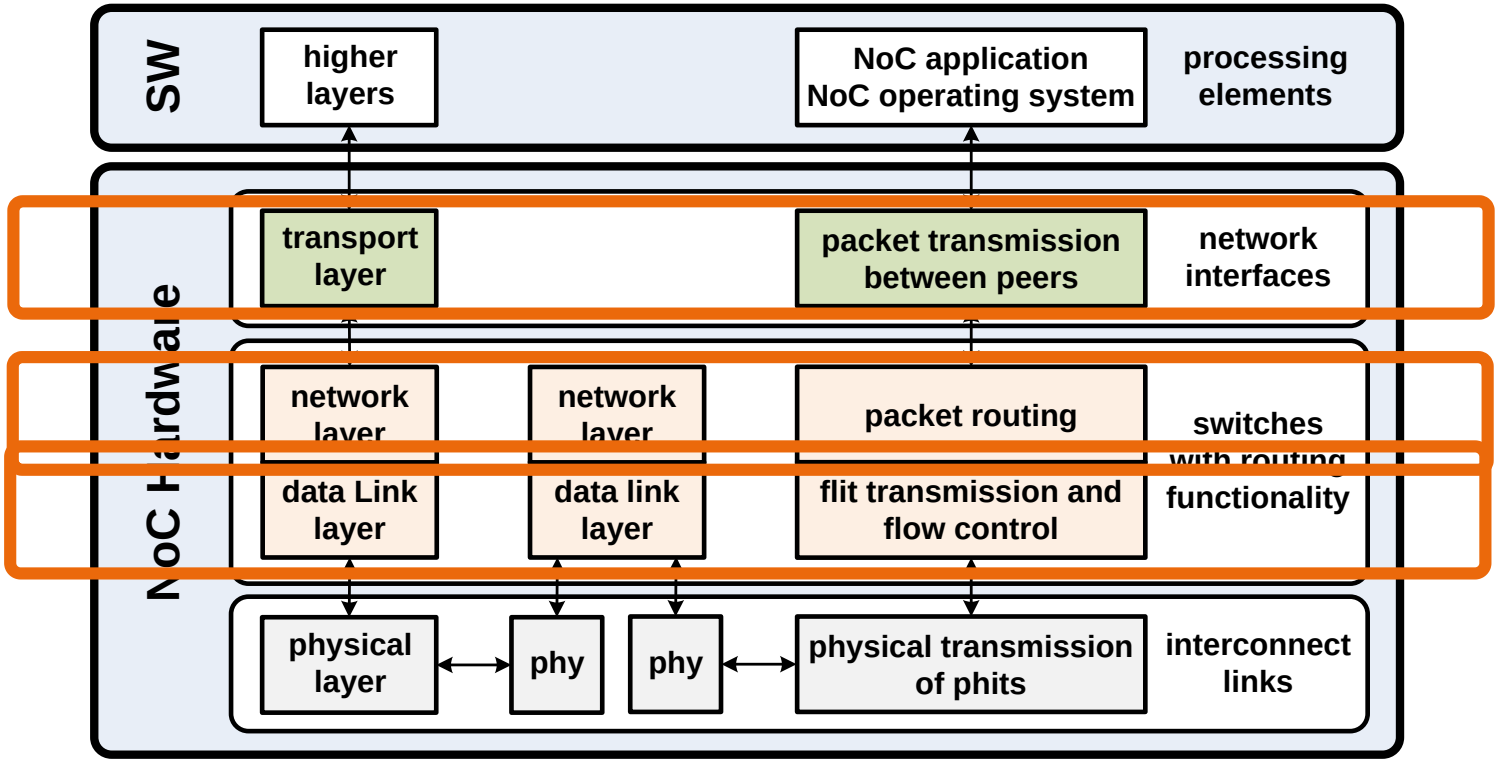


- Self Transfer
  - Special case of indirect transfer: source slave and destination slave is the same NoC device
  - Example: data copy in same memory

Fault Resilience

Investigations and extensions on baseline NoC

NoC layered architecture



Network-on-Chips layers and modules

M. Radetzki, et al., “Methods for Fault Tolerance in Networks on Chip”, ACM Computing Surveys, 2013

Fault Model

Layer	Scope	Fault Type	Cause
Data-Link	Link & Router	Data Corruption	SEU/SET, Stuck-at, crosstalk, etc.
		Flit Insertion	
		Flit Loss	
Network	Channel	Misrouting	unresolved data-link layer error, routing algorithm error, address mapping error, etc.
		Broken-route	
Transport	Connection	Packet Loss	unresolved data-link layer error, unresolved network layer error, network interface error, etc.
		Packet Corruption	

Fault Mitigation Techniques

Layer	Mitigation Techniques	Fault Type						
		Data Corruption	Flit Duplication	Flit Loss	Misrouting	Broken-route	Packet Loss	Packet Corruption
Data-Link	Error Detection and Correcting Codes (EDAC)	√ √				√		
	Flit-Level Flow Control		√ √	√				
Network	Detour	√				√		
Transport	End-to-End Retransmission	√	√	√	√		√	√
	Packet-Level Flow Control				√		√	

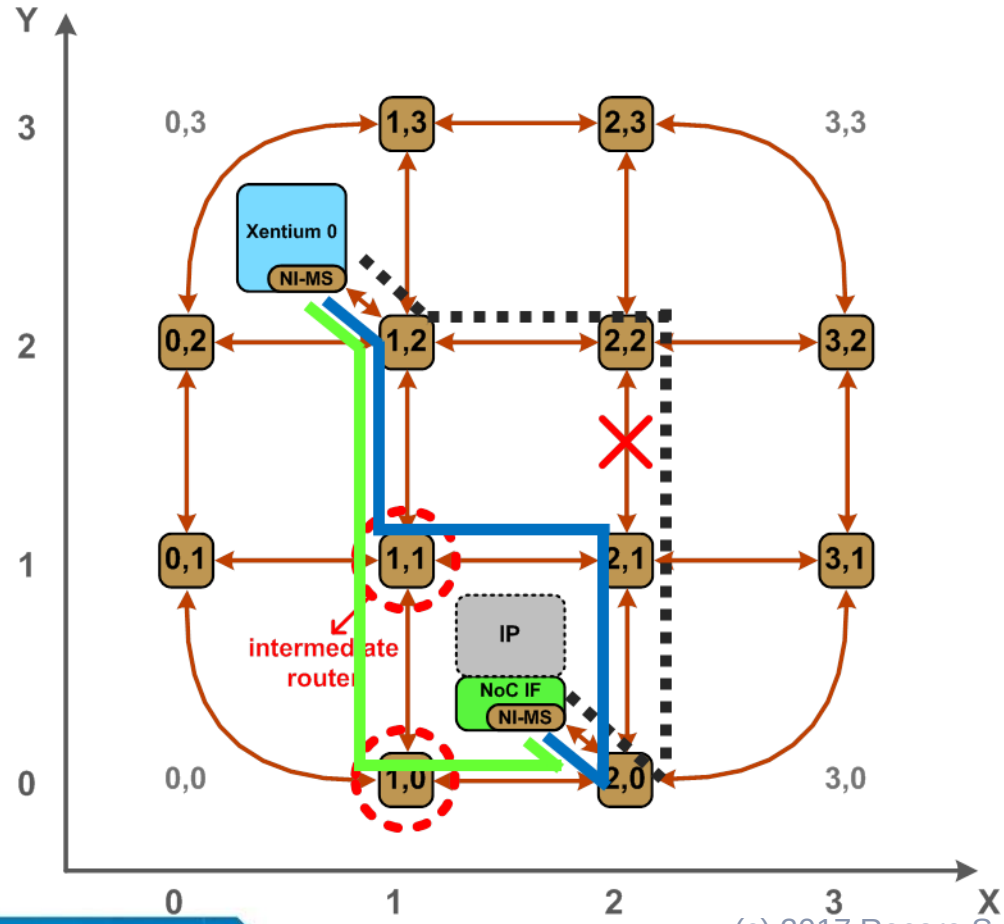
√ detection √ correction

- Mitigation techniques are proposed to be implemented in data-link and network layer.

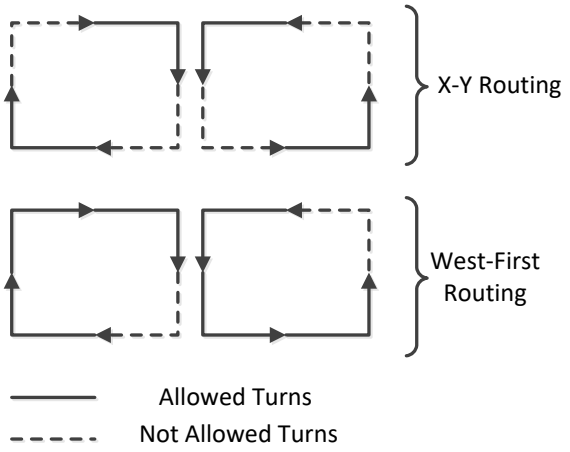
NoC improvements

- Robustness
  - Error handling, error signalling → embedded as side-signals in flit
- Static error correction
  - Detour/rerouting of traffic in NoC → also improves traffic load balance
- Transient error resilience
  - FF hardening (e.g. ST65Space, DARE180) → synthesis support
  - Transient error detection / correction → instantiate & integrate with error signalling
    - EDAC mechanisms on data
    - CRC on payload
    - EDAC flit hardening
    - …

NoC improvements
Data rerouting in NoC (1/2)

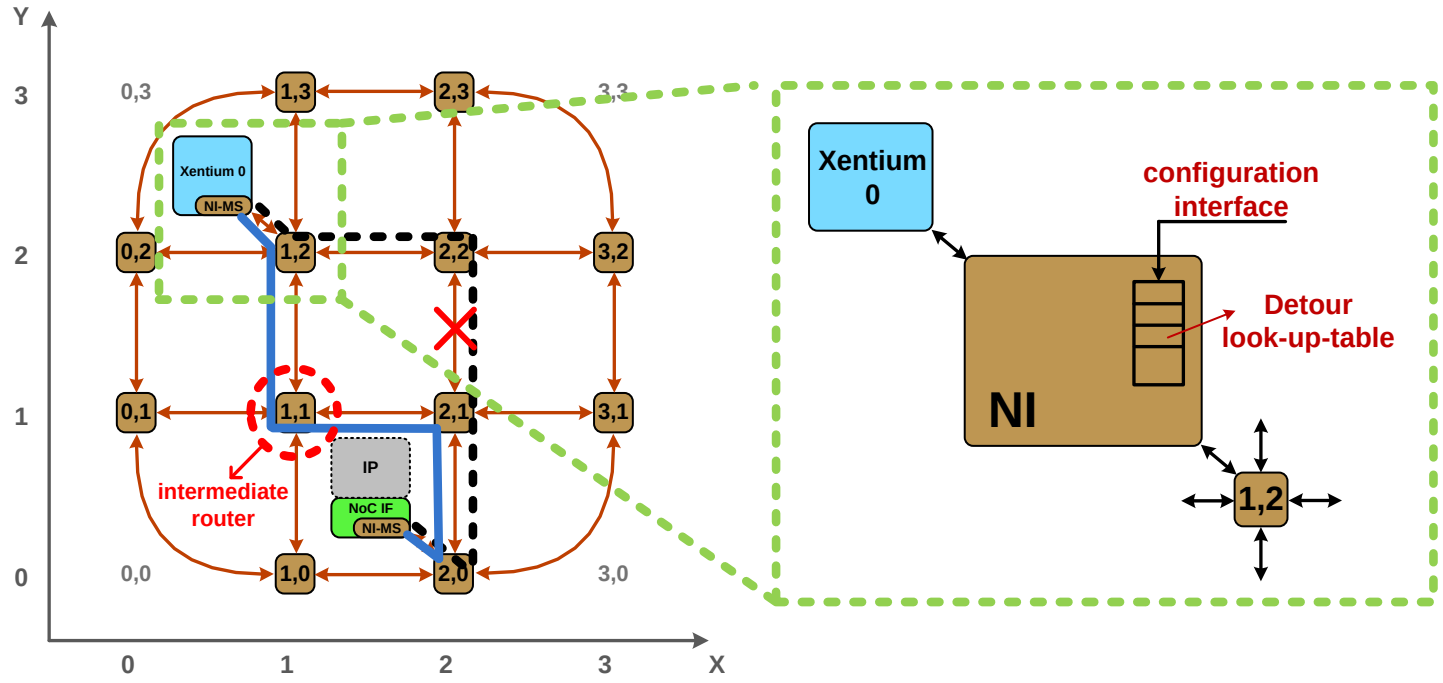


- Xentium 0 → IP
  - X-Y routing
  - detour from (1, 1)
  - detour from (1, 0)



NoC improvements
Data rerouting in NoC (2/2)

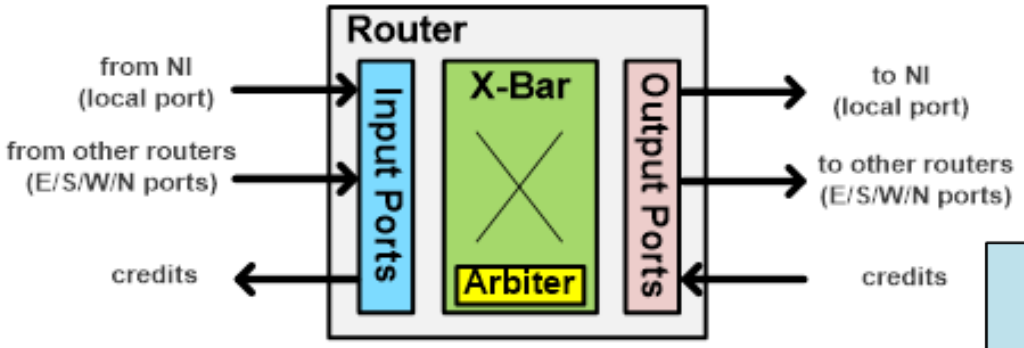
- Detour LUT registers contain modified packet header information with intermediate router coordinates



NoC IP

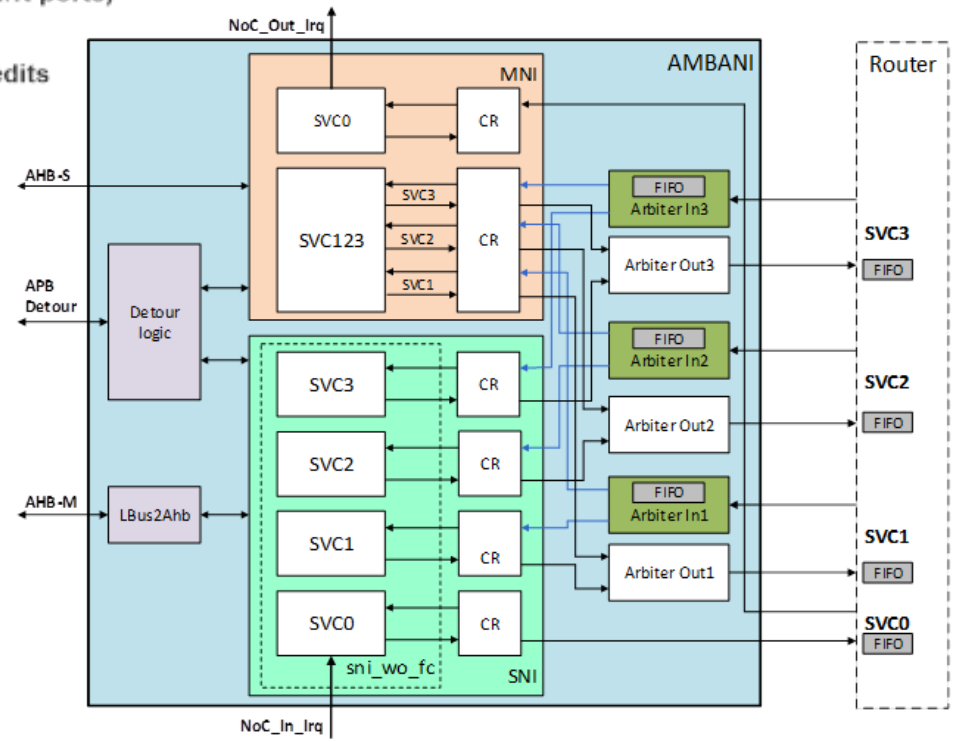
NoC IP components and testbenches

NoC IP components

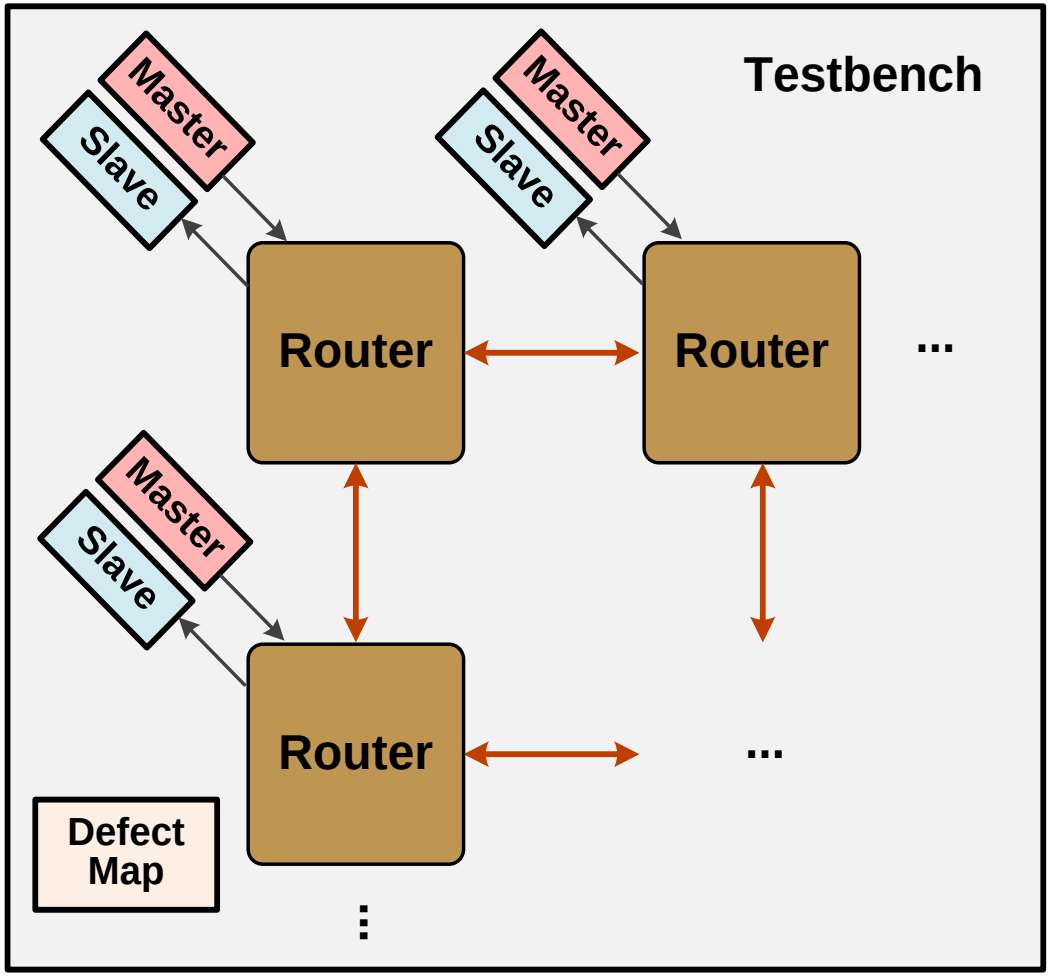


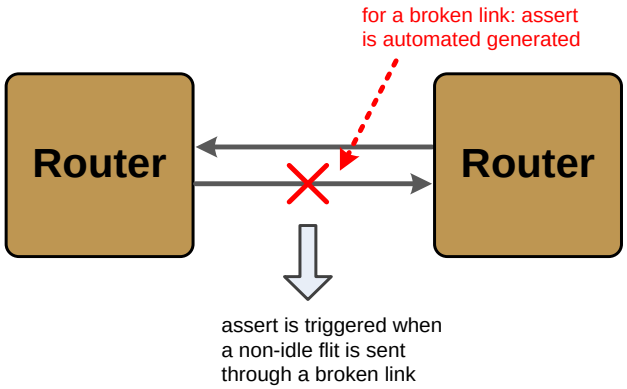
NoC router

AMBA NI
(NoC bridge interface)

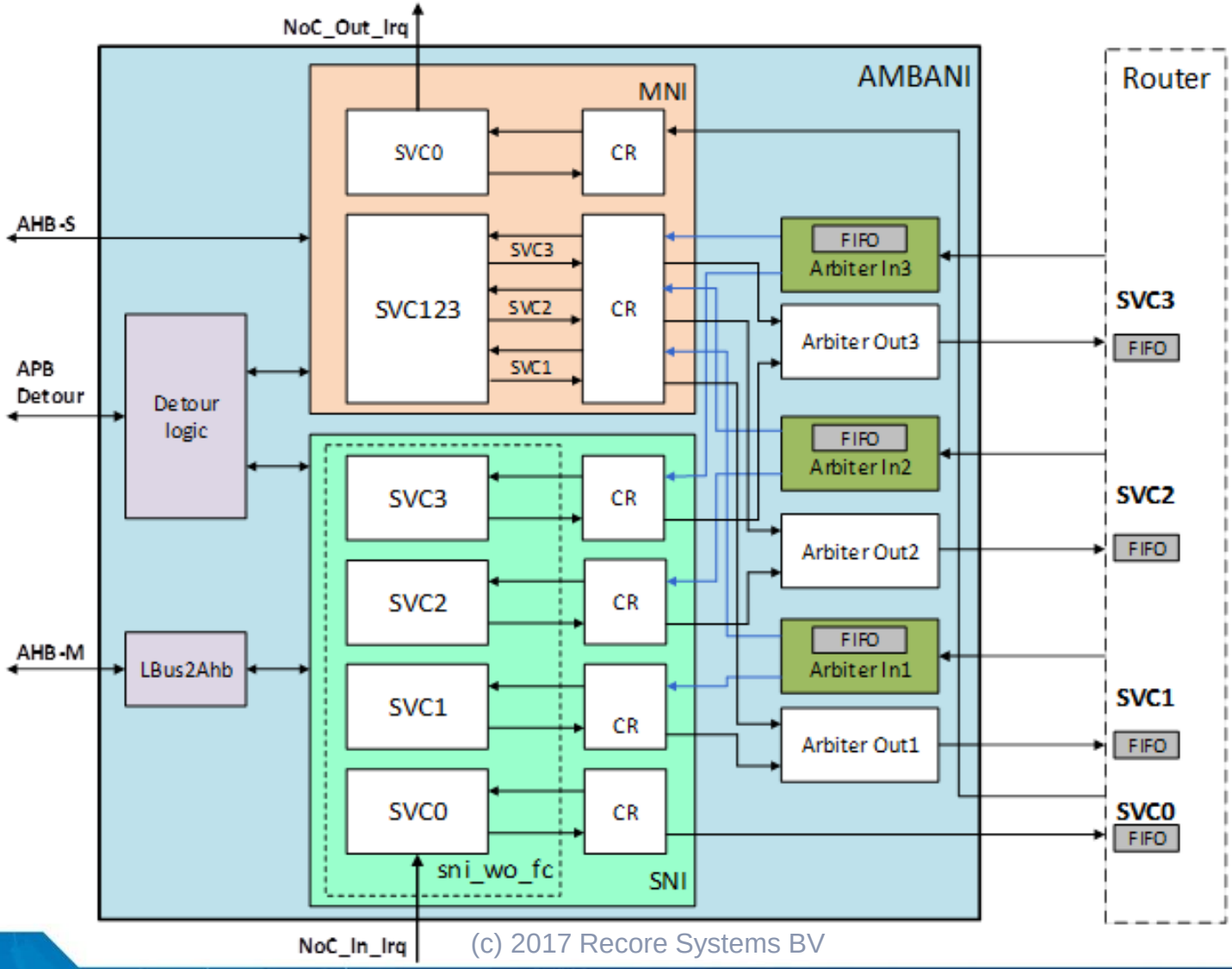


NoC router testbench





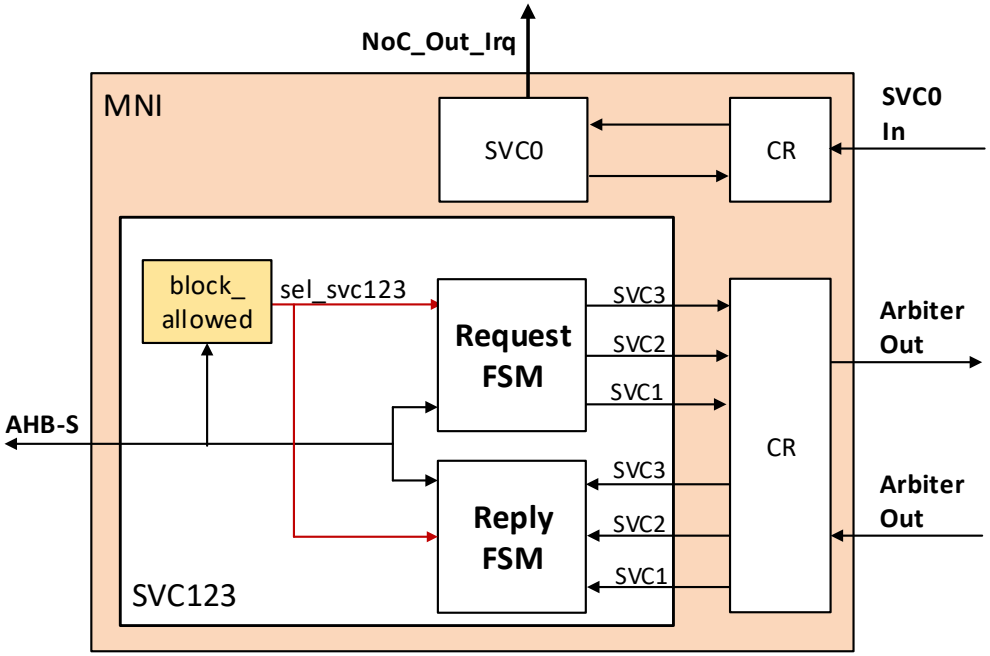
AMBA NI



AMBA NI (MNI)

Master Network Interface:

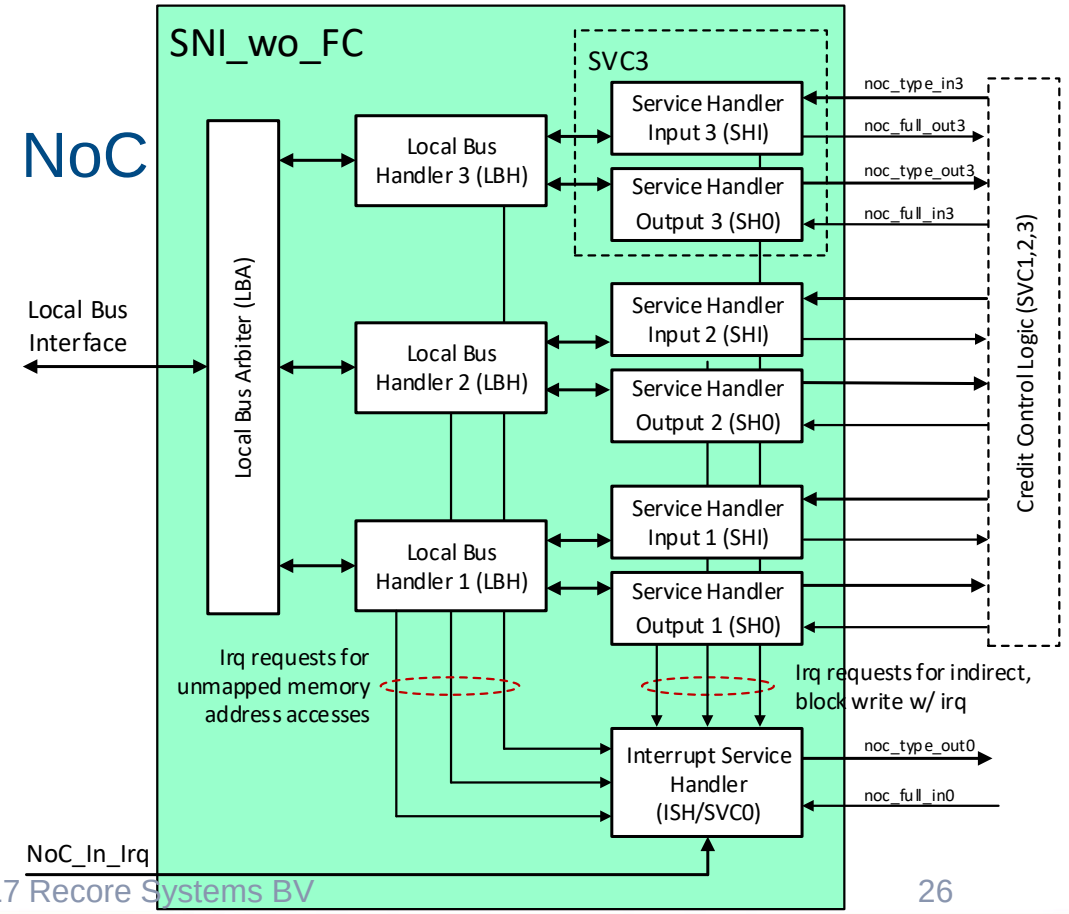
- Initiates requests on NoC to Slaves
- Reacts on replies from Slaves
- Reacts on IRQ messages from NoC



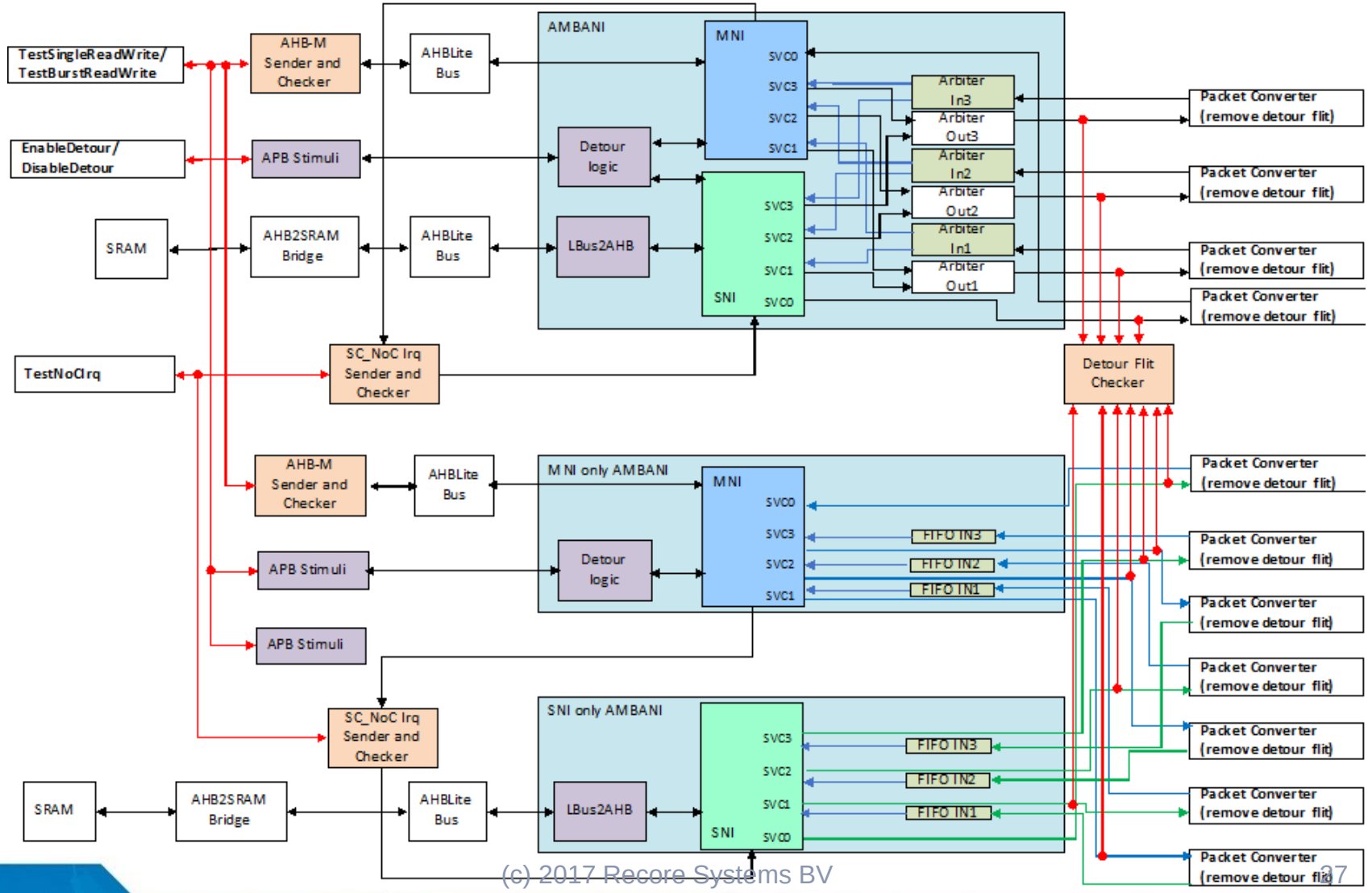
AMBA NI (SNI)

Slave Network Interface:

- Reacts on requests from Master
- Initiates replies to Master
- Initiates IRQ messages on NoC



AMBA NI test bench



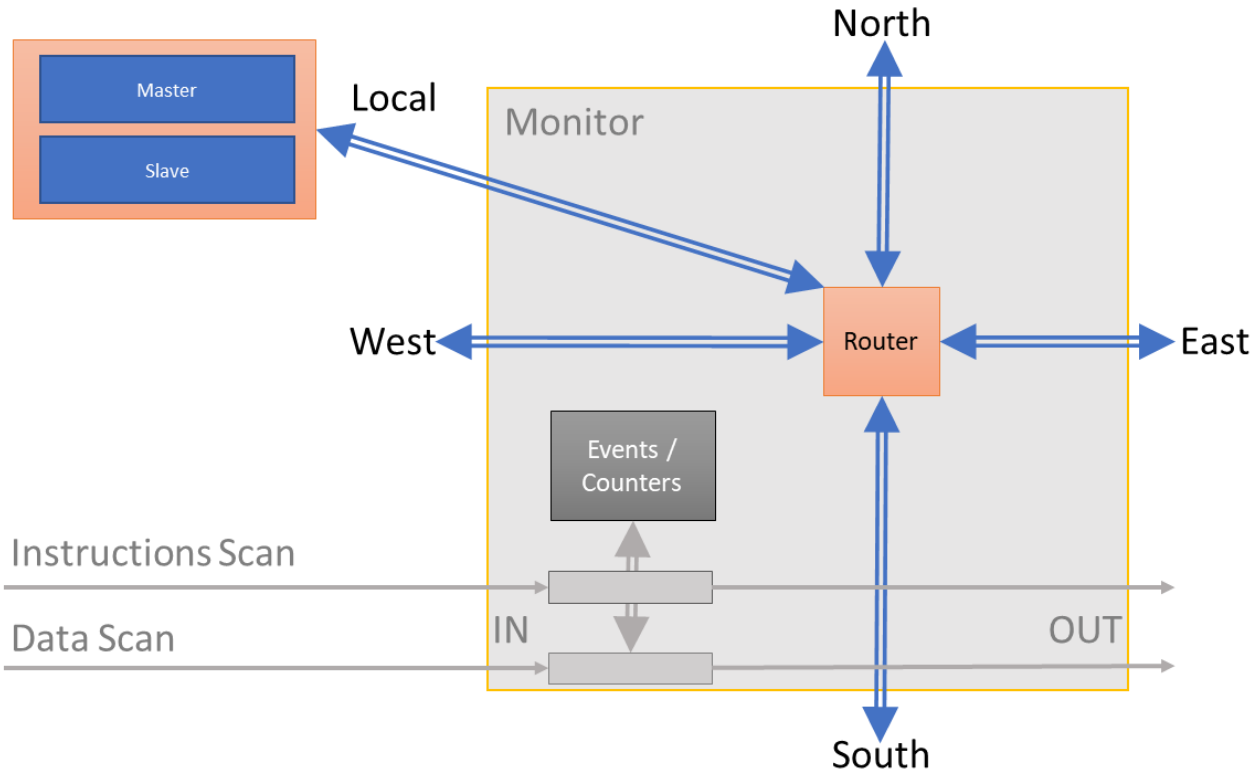
AMBA-NI functional verification

- AMBA-NI IP Configurations
  - Full with both AHB master and slave IF
  - Only AHB master IF (SNI - NoC2AHB)
  - Only AHB slave IF (MNI - AHB2NoC)
- AMBA-NI Verification Configurations
  - IP testbench (released with IP package)
  - IP NoC mesh test bench (in-house)
  - SNI IP Block test bench (in-house)

NoC performance testing

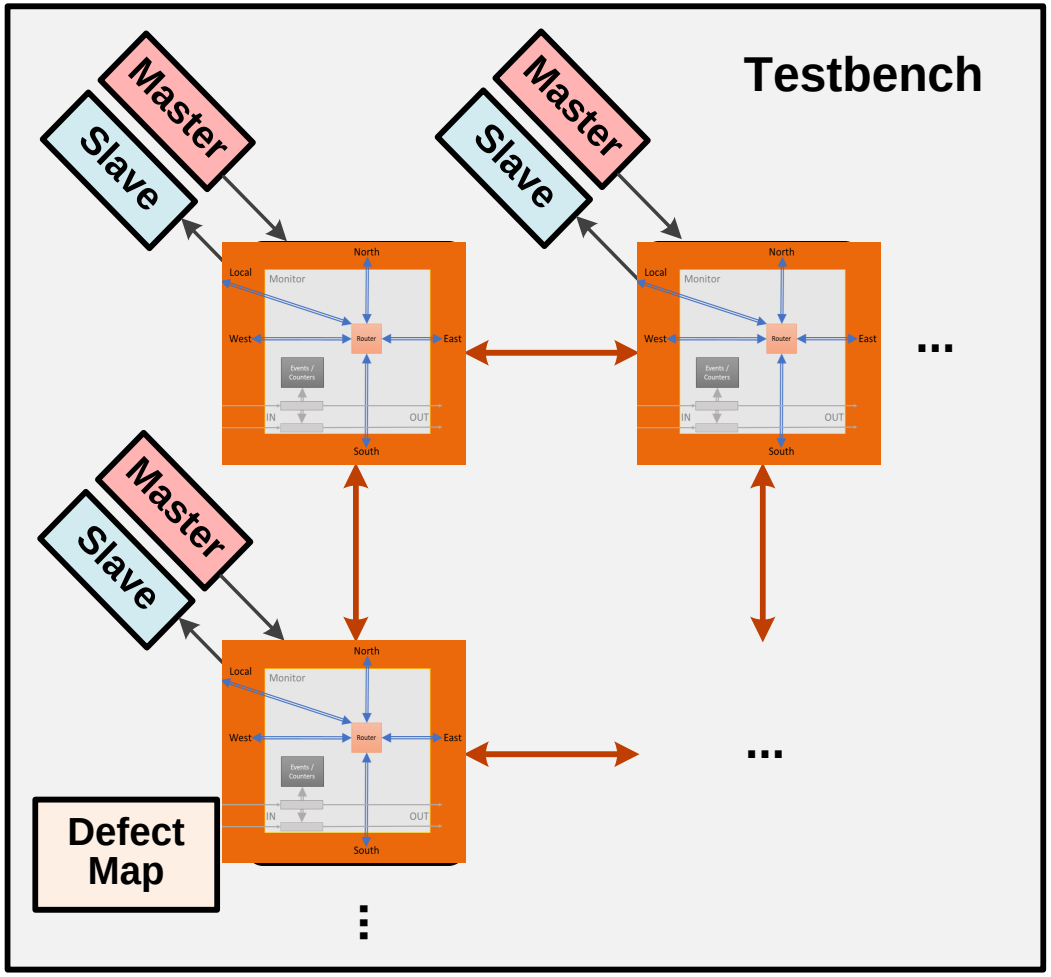
NoC IP performance monitoring

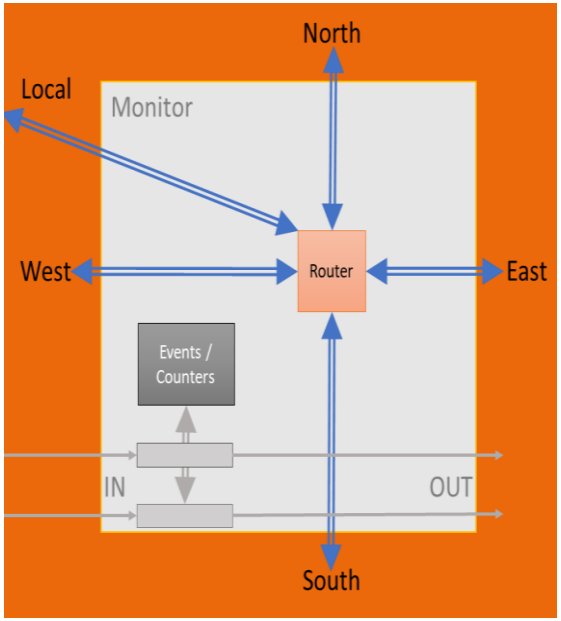
NoC event monitor



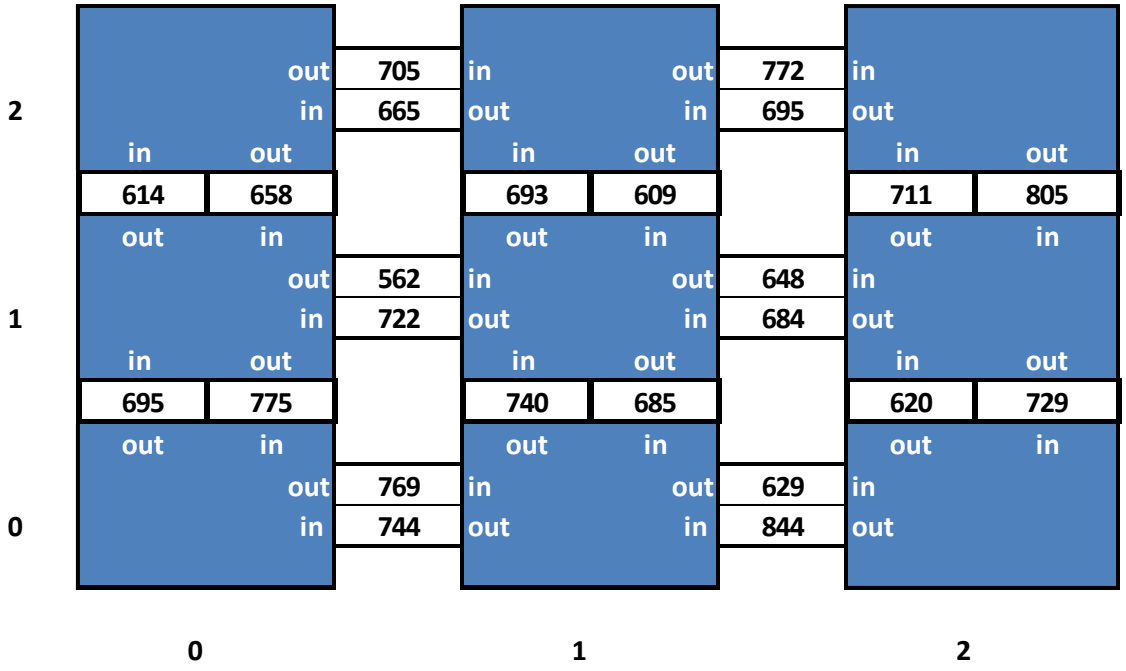
- NoC monitor wrapped around each router; monitors
  - Throuhput, latency,
  - Error Events

NoC router testbench extension

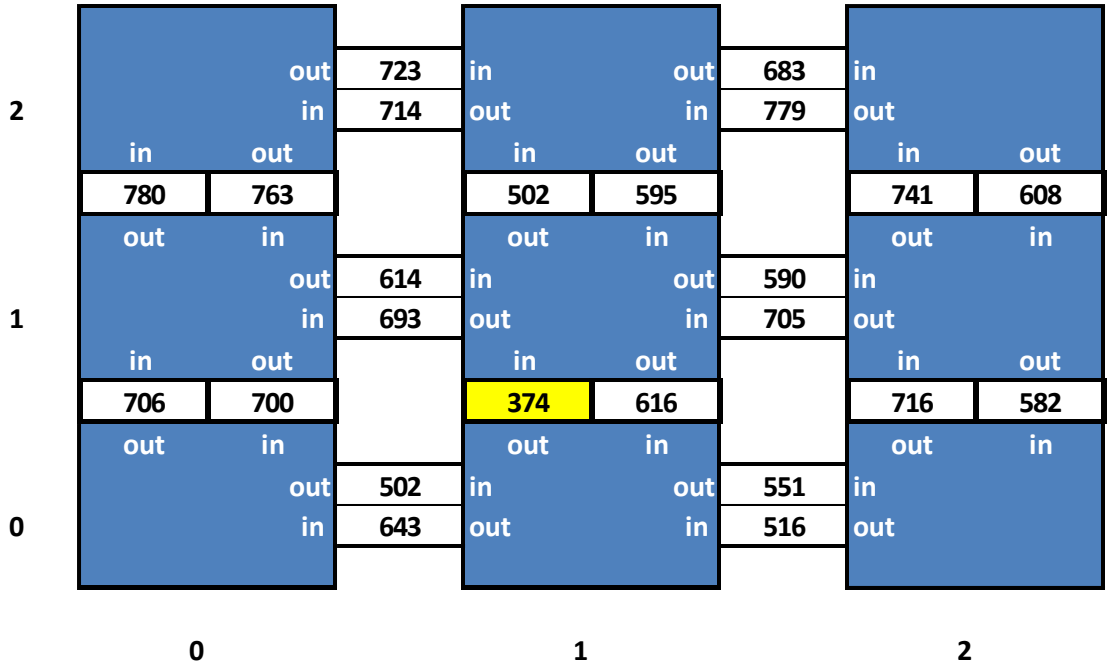




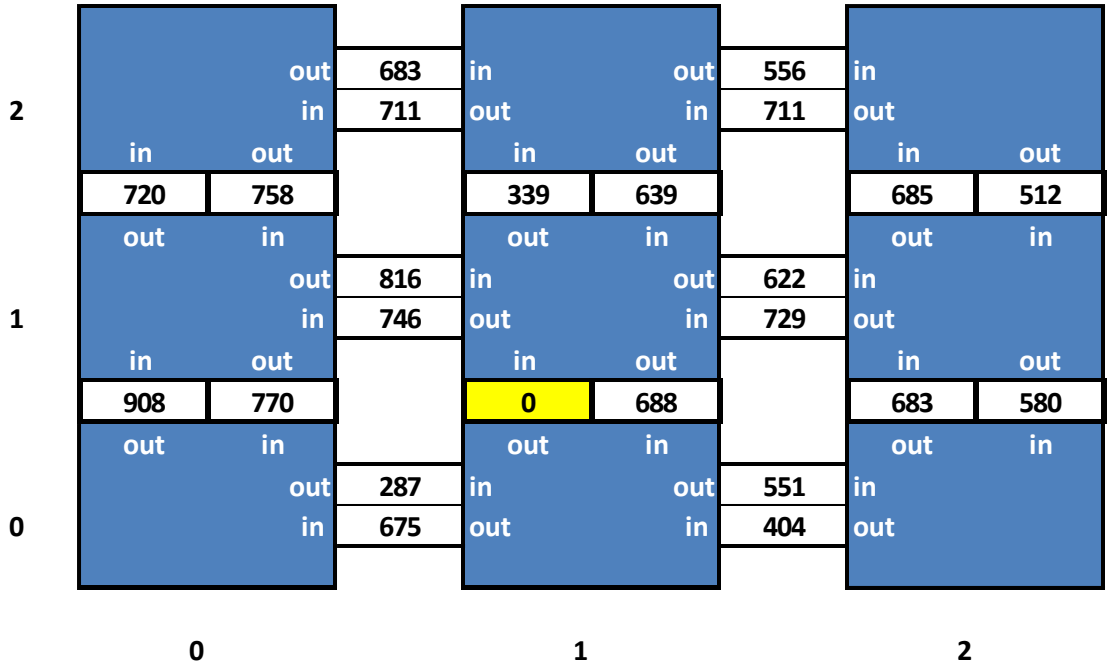
Heatmap (no detour)



Heatmap (detour for traffic balance)



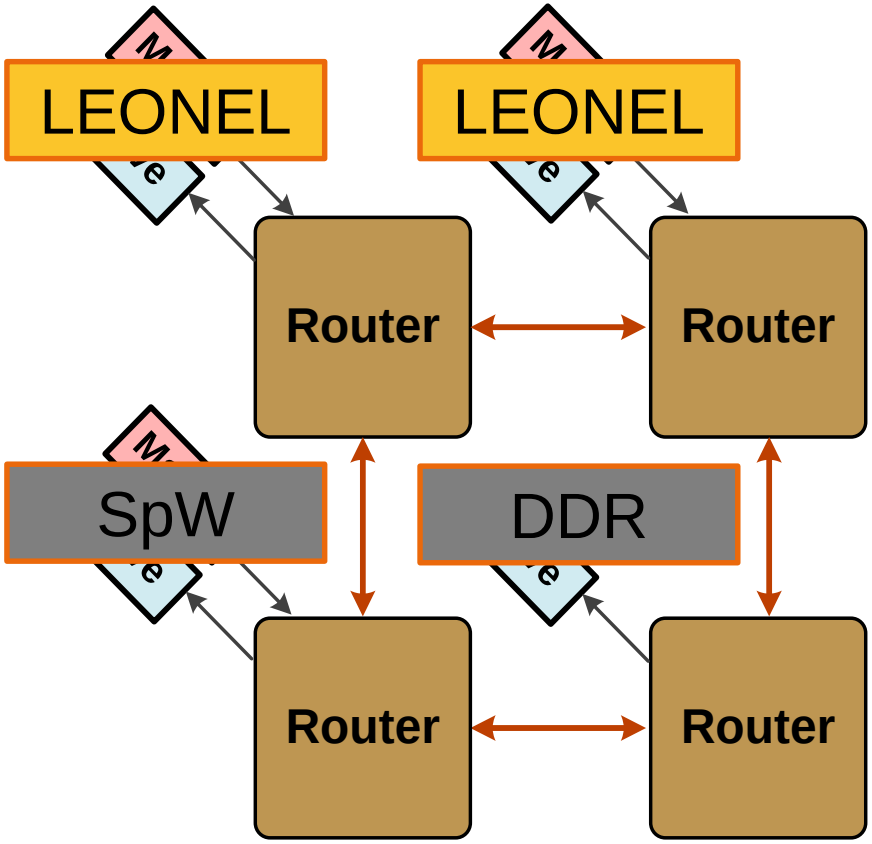
Heatmap (detour broken link)



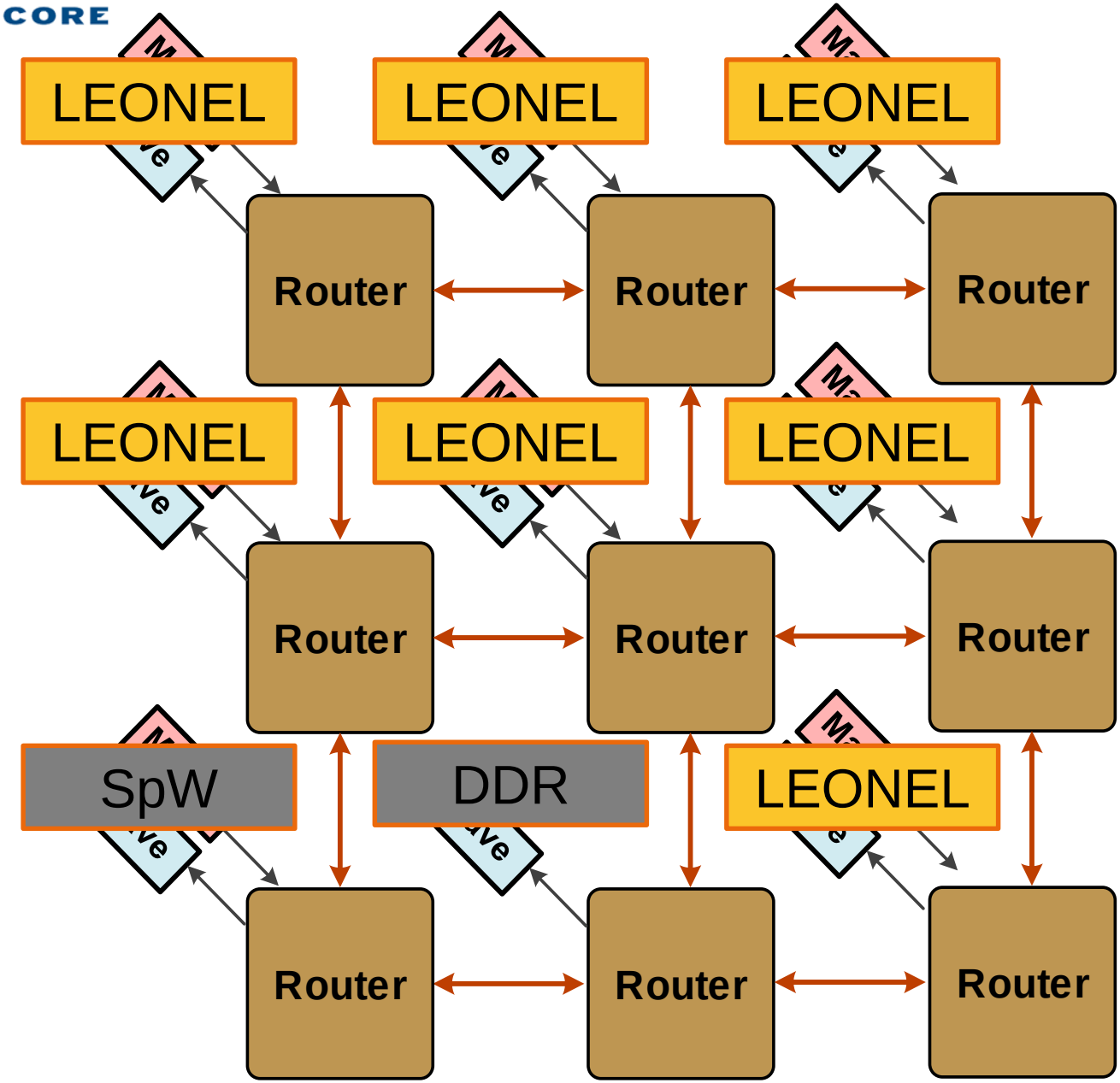
NoC reference system

FPGA reference NoC implementation and multi-core software use-case

Scalable 2D-mesh many-core architecture



- SpaceWire element (0,0): connects GRSPW2 SpaceWire controller
- Memory element (0,1): AHB slave memory
- LEONEL (1,0): connects LEON3FT Processing Element
- LEONEL (1,1): connects LEON3FT Processing Element


LEONEL
LEONEL
LEONEL
Router
Router
Router
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SpW
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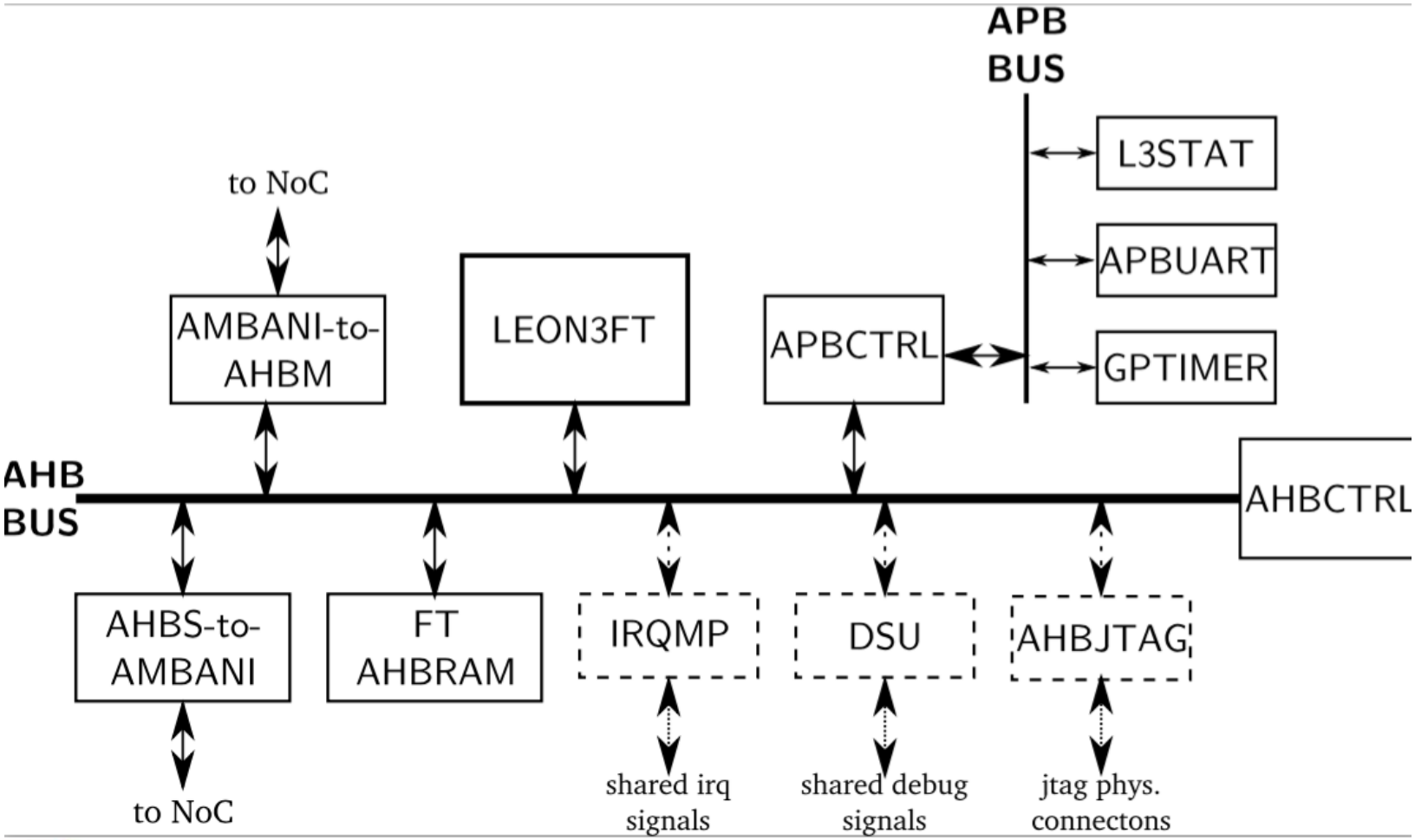
Router

LEONEL: Leon3 Processing Element



Synthesis

- Target clock frequencies 180MHz, 500MHz and 1GHz for DARE180, ST C65SPACE and ST 28nm FD-SOI.
  - NoC router is estimated ~25 kGates (version with all directions connected)
  - full AMBA Network Interface is estimated ~70 kGates (full version)
- Reference system available for Xilinx 7-Series and Virtex-5
  - NoC Router: 2854 - 4637 Slices / 2316 - 3541 LUTs
  - AMBANI: 4963 - 5996 Slices / 6910 - 7265 LUTs

Test case validation software

- The NoC reference system includes validation software
  - The test software uses a parallelized version of the OpenJPEG library to compress an image.
  - The program is divided into one main control program that handles the sequential part of the code *running on LEONEL0*, and
  - multiple worker programs that perform the parallel part of the work *running on LEONEL1-LEONEL7.*

Wrapup

Final results

ESA IP core availability

- NoC IP available as ESA IP core for ESA's own requirements.

- VHDL implementation of NoC IP
- SystemC model of NoC IP for early software development
- ASIC Synthesis scripts
- FPGA reference projects compatible with GRLIB
  - with compression software use case

Conclusion

- The activity resulted in NoC IP:
  - NoC router
  - AMBA-to-NoC Network Interface (AMBANI)
- The IP has been integrated in a reference design
- The IP can be synthesized and targetted to different ASIC and FPGA technologies
- Performance tools are integrated in the NoC mesh testbench
- SystemC models for early software development are available

Ready for the next step? Heterogeneous many-core SoC

- Xentium VLIW DSP core in rad.-hard 65nm CMOS
  - Clock: 300 MHz
  - Performance: 1.8 GFLOPs/s
  - NoC per link: 9.6 Gbit/s
  - Area: 1.1 mm^2
    - 75% gates utilization
    - Including NoC interface
- Many-core SoC example
  - 48 Xentium processing tiles
  - 16 memory tiles
  - 60 NoC routers
    - 8×8 mesh

→60 Giga MACs/s
→90 GFLOPs/s