Network on Chip (NoC) for Many-Core System on Chip in Space Applications

by X (Recore Systems)

The continuous advances in instrument technology and increases in demand for on-board autonomy and intelligence translate into an ever increasing demand for on-board data processing performance. The recent availability of hardened sub-micron ASIC technology (65nm and beyond) opens new opportunities for higher integration and also sets new challenges when tomorrow's SoC designs for space applications exhibits tens of Millions of gates.

Recore Systems B.V. (prime) and Cobham Gaisler AB (subcontractor) have successfully completed the "Network on Chip (NoC) for Many-Core System on Chip in Space Applications" project delivering generally available NoC IP technology for the ESA IP core portfolio. The NoC IP is based on Recore's NoC technology also used in previous (Massively Parallel Processor Breadboard (MPPB) and XentiumDARE) and on-going activities (Scalable Sensor Data Processor (SSDP)). The activity includes comprehensive validation with state-of-the-art proven space relevant component and ASIC technology.

The NoC IP implements packet-switched NoC technology using xy-routing and wormhole switching. The NoC provides scalable, deterministic, predictable, and deadlock free communication. Moreover, the NoC combines the determinism of xy-routing with explicitly programmable adaptiveness that allows a controlled manner for routing traffic around congested or faulty network elements while preserving determinism and dead-lock freedom. Besides the router IP block, the NoC IP includes an AHB network interface IP block. The AHB network interface provides AHB slave and master interfacing for connecting IP components to the NoC. The AHB network interface makes it straightforward to connect AHB-based IP blocks in memory-mapped NoC-based systems.

The IP validation included synthesis for state-of-the-art space ASIC technologies and the creation of a test case system integrating off-the-shelf space-proven IPs in a NoC-based multi-core SoC. This reference implementation includes a NoC-based multi-core platform with seven LEON3FT cores.