Passion for Technology

# European LVDS Octal Repeater

TEC-ED & TEC-SW Final Presentation Days

December 13, 2017

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# ABOUT ARQUIMEA



**ARQUIMEA** and **ARQUIMEA DEUTSCHLAND** are Sister Companies with complementary capabilities

**Fabless Design Houses** specialized in **hi-rel technologies** for **space applications**

Suppliers of **electronics, microelectronics** and **mechanisms**

Strong **R&D** activity and **product-oriented** strategy

**EUR 6.5M revenues in FY17**

**34 employees**


# ABOUT ARQUIMEA
## Customers and Partners

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**ITAR free** | **Fabless** | **Design house** | **Space & hi-rel** | **Multinational**

## MEMBER OF

ASD-EUROSPACE The Space group in ASD
SME4SPACE
BBAA Berlin-Brandenburg Aerospace Allianz e.V.
tedae Asociación Española de Empresas Tecnológicas de Defensa, Aeronáutica y Espacio
enterprise europe network

## BUSINESS AREAS

- ELECTRONICS & MICROELECTRONICS
- ACTUATORS & MECHANISMS
- NUCLEAR WASTE DISPOSAL TECHNOLOGIES

## MAIN COSTUMERS & PARTNERS

esa
ThalesAlenia Space
AIRBUS DEFENCE & SPACE
TTTech
European Commission
STI
SURREY SATELLITE TECHNOLOGY LTD
中国航天 CASC
中国空间技术研究院 China Academy of Space Technology
SITAEL
TRYO Aerospace
ihp
KONGSBERG
INTA
Micro Drive
LUXSPACE An OHB Company
Atmel MICROCHIP

# ABOUT ARQUIMEA

## Microelectronics – General Capabilities

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## SPACE APPLICATIONS

**Space-qualified** electronic systems and components

**1500+ flight chips** delivered to date

Turnkey projects: **ASIC, FPGA** and **electronic systems**

**Analog, Digital** and **Mixed-Signal**

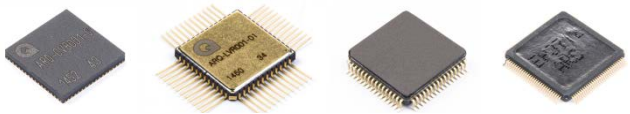
Low power, low frequency, high voltage

Technology characterization

Design Centers in **Spain** and **Germany**

Main customers:

esa · AIRBUS DEFENCE & SPACE · ThalesAlenia Space



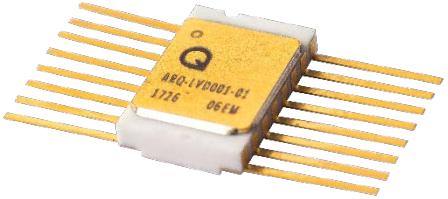
## PRODUCTS

**Space**

- **LVDS** driver, receiver, repeater, transceiver
- **Space Ethernet** PHY transceiver
- Rad-hard **IP cores**
- Signal conversion, signal processing

**Non-space** (under development)

- Hi-rel. Rad-tolerant
- Defence & Security, Nuclear, Aeronautics, Telecom…



## TECHNOLOGIES & TOOLS

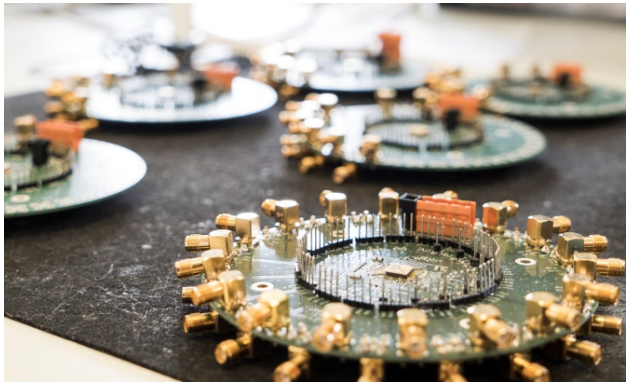
Own proprietary **rad-hard IPs** and **libraries** in several technologies

UMC · Atmel MICROCHIP · ihp · ON Semiconductor

**Reliable design flow** and EDA tools

cadence · Mentor Graphics

**In-house** radiation simulation tools, Electronic Labs, PCB design and test setup development



# ABOUT ARQUIMEA

## Microelectronics – Flight Heritage

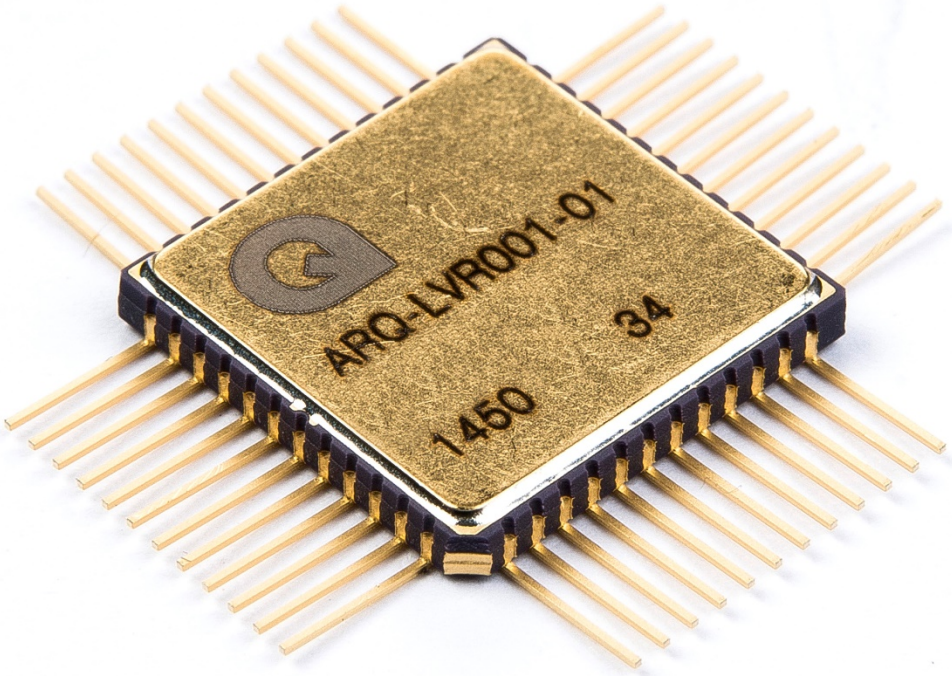

FLIGHT PROVEN

Supplier of Hispasat 36W-1 GEO communications satellite.

**624 spaceflight chips in a single mission**

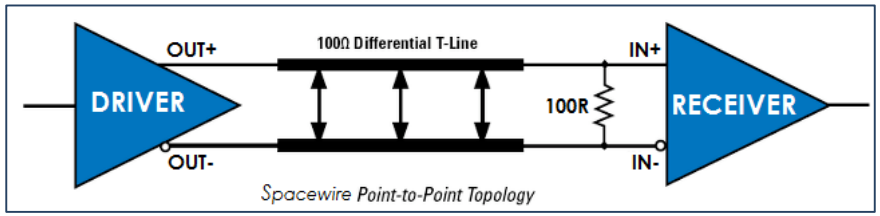
Mission video

# RAD-HARD 500Mbps LVDS OCTAL REPEATER



# LVDS REPEATER
## Introduction

### CONTEXT




- **SpaceWire increased demand** for European space programs
- **Existing rad-hard devices** coming from the US market – ITAR
- **Existing Commercial devices** without **key features** like fail-safe, cold sparing or extended common mode

### **ECI** (European Components Initiative)

- **ITAR Free – LVDS European alternative**
- **Compatible with existing products**
- **Availability, Cost and Schedule**
- **Suitability for Space** (technical, radiation and reliability features)

### LVDS PRODUCT FAMILY

- **ARQUIMEA** self-funded activity
- Development of a **European rad-hard LVDS family** based on **ESA Project outcomes**

# LVDS REPEATER

## Objectives and Requirements

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### REFERENCES

- **ESTEC/ITT** AO/1-6922/11/NL/LvH
- **ESA Contract** ESTEC-4000105886

### PROJECT OBJECTIVES

- **LVDS European alternative** without ITAR restriction
- **LVDS Octal Repeater IC** development and qualification
- **LVDS Driver & LVDS Receiver** IP cores
- **Added Features** (cold spare, fail-safe, extended common mode)
- **Application to EPPL** Parts List

# LVDS REPEATER

## Objectives and Requirements

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### GENERAL REQUIREMENTS

- **500Mbps operation** requirement
- **LVDS standard TIA/EIA-644** Full Compliance
- **Compatible** with US Devices
- **IHP SGB25V Library** (Hot Carrier Injection, ESD protections & Cold-spare)
- **5V tolerant TTL Digital Input**

### ADDITIONAL FEATURES

- **Extended Input Common Mode** [-4V to +5V] (Attenuator network required)
- **Input Hysteresis** (25mV)
- **Fail-safe Protection** (Patent compliance, Input Threshold Levels)

# LVDS REPEATER

## Objectives and Requirements

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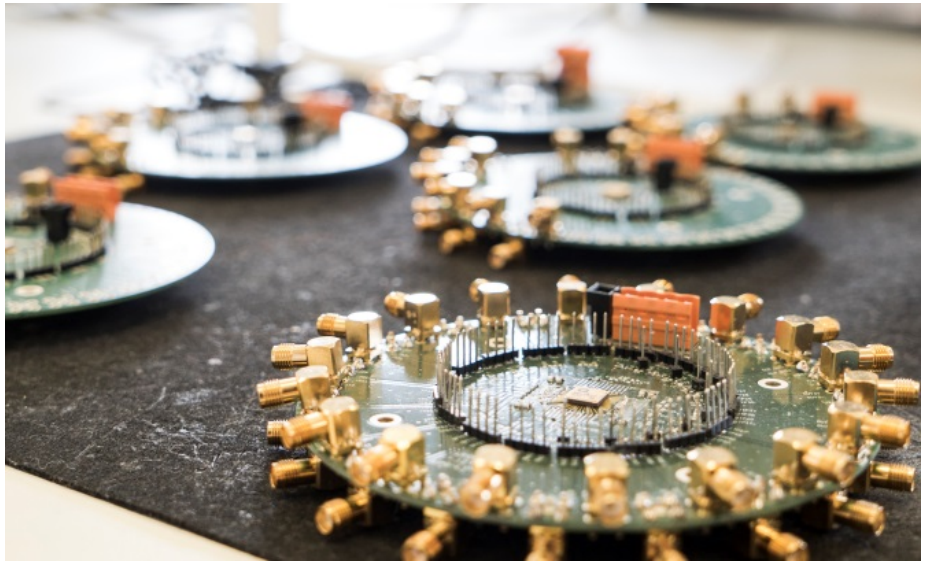
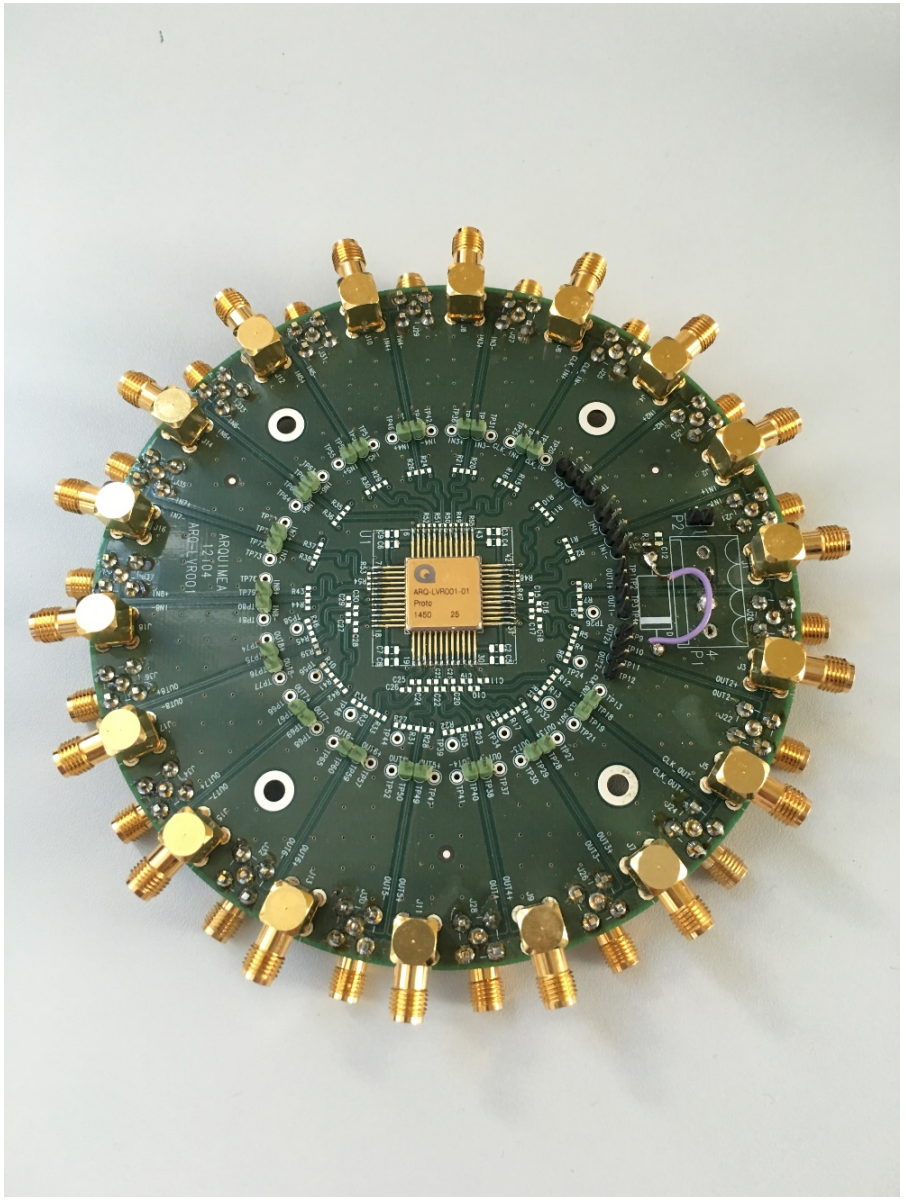
### TEST SET-UP challenges

- Jitter
- Propagation time
- Skew Parameters
- Leakage Currents

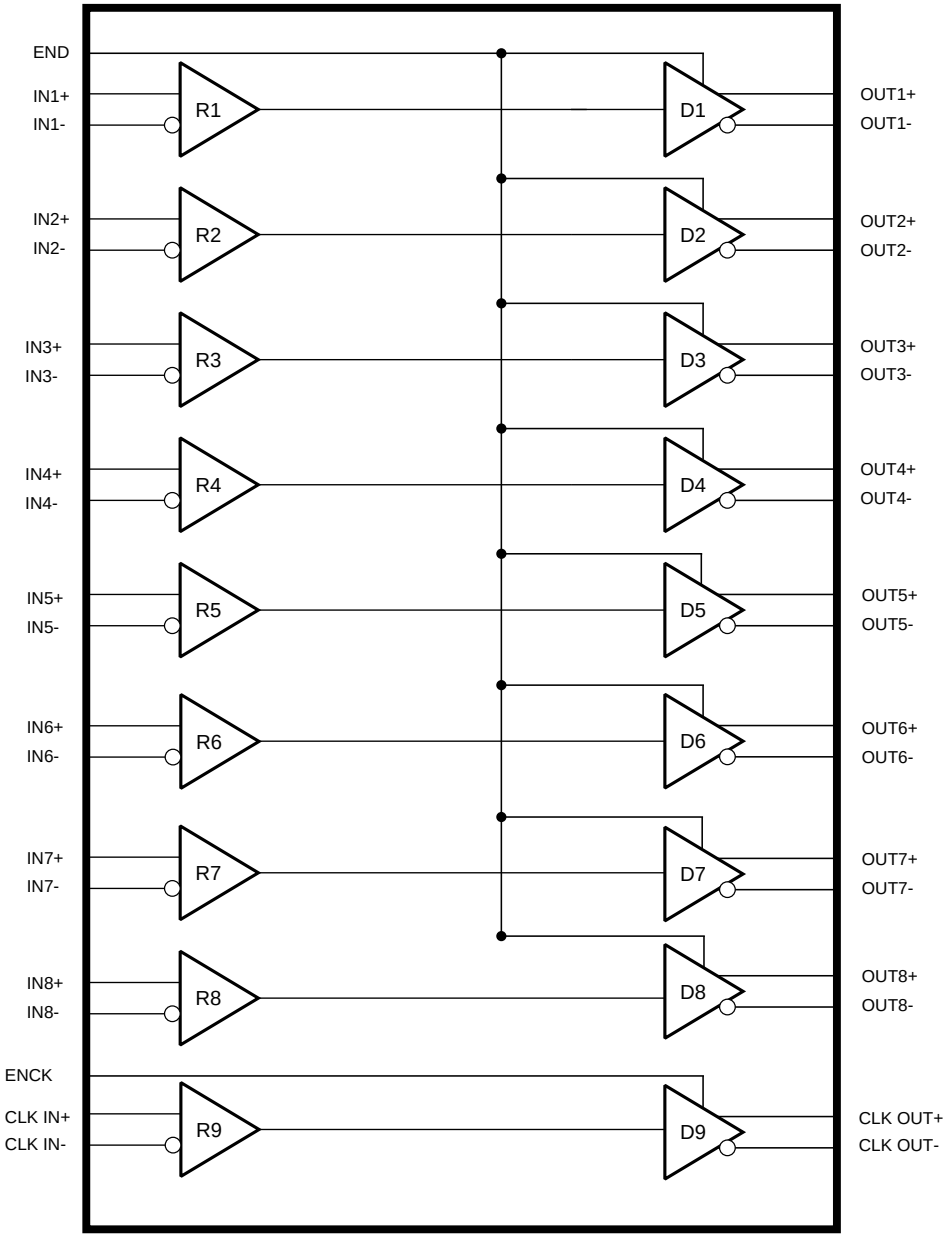




# LVDS REPEATER

Features

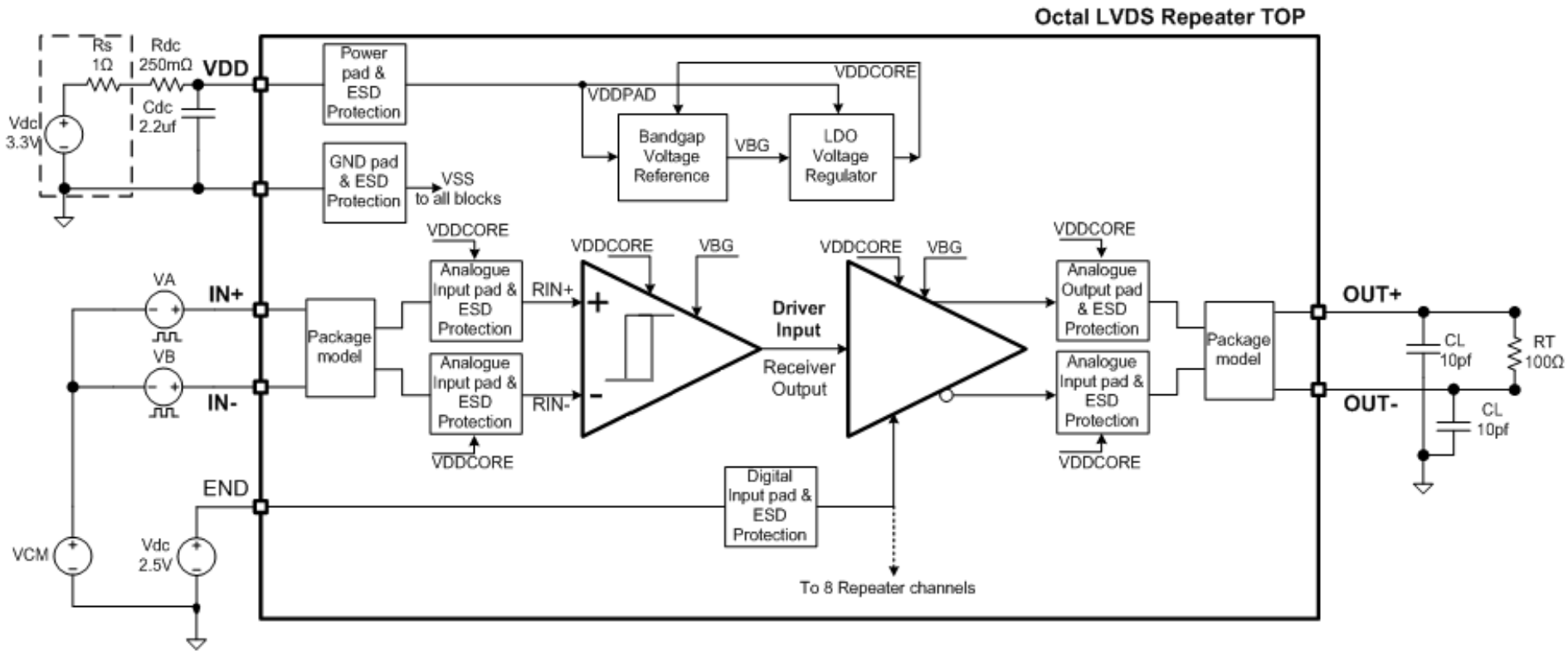
## BLOCK DIAGRAM



# LVDS REPEATER

## Features

## TOP LEVEL SCHEMATIC



# LVDS REPEATER

Features

## PROJECT PARTNERS

| DEVELOPMENT FLOW | SUPPLY CHAIN | |
|---|---|---|
| DEFINITION & FEASIBILITY ANALYSIS | ARQUIMEA | ARQUIMEA |
| DESIGN – OVERALL | ARQUIMEA | ARQUIMEA |
| DESIGN – ESD PROTECTIONS | SOFICS | SOFICS |
| DESIGN VERIFICATION | ARQUIMEA | ARQUIMEA |
| MANUFACTURING (SGB25V MPW) | IHP | ihp |
| ASSEMBLY | SERMA (HCM) | SERMA HCM.SYSTREL |
| VALIDATION | ALTER | ALTER TECHNOLOGY |

# LVDS REPEATER

Features

## FOUNDRY PROCESS

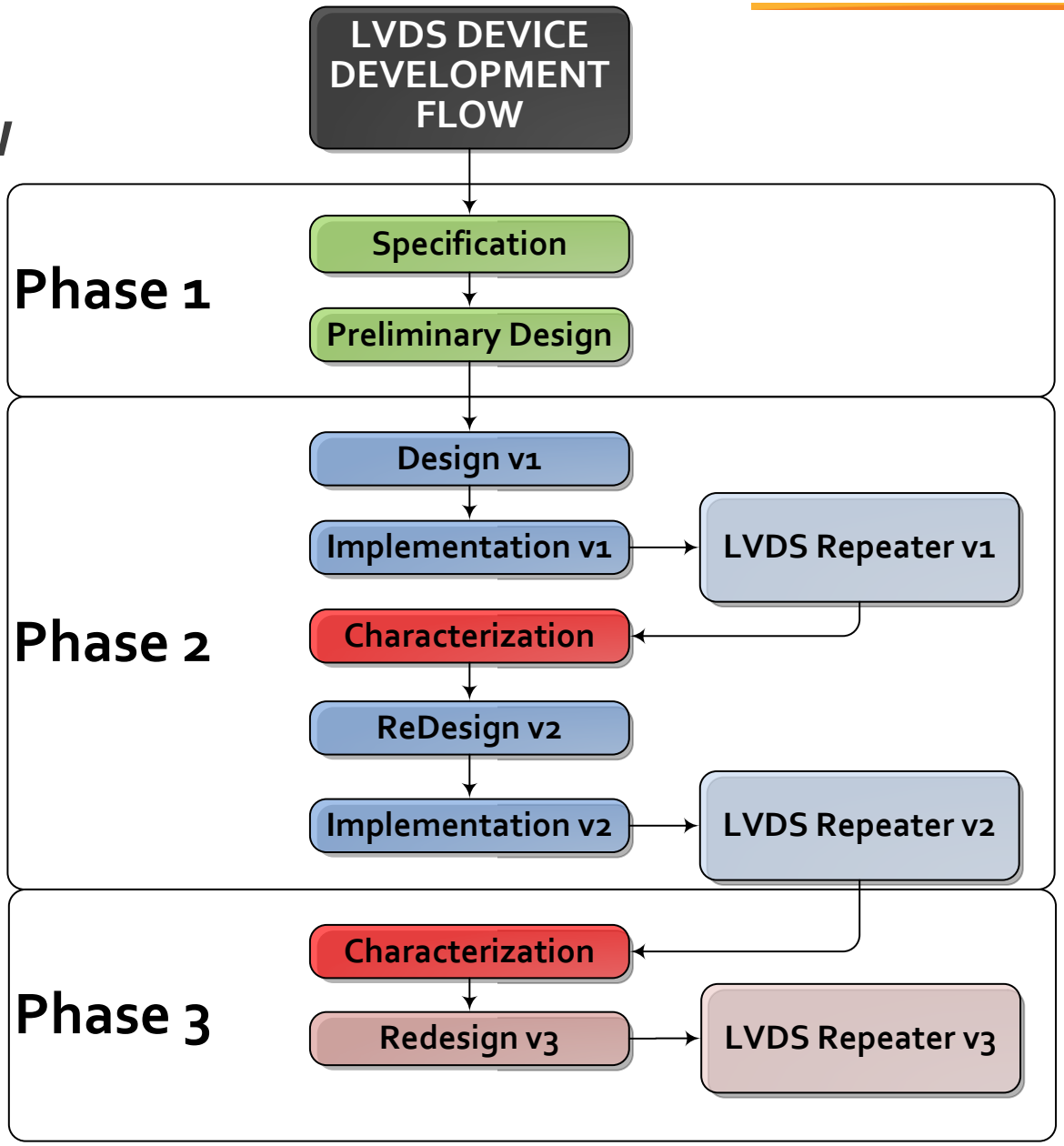
- **IHP Microelectronics** (Germany)
- **SGB25V – 250nm SiGe BiCMOS** Technology
- **Qualified process** based on JEDEC Standard JP001.01
- **Rad-hard** (TID, SEL free)

## TECHNOLOGY CHALLENGES

- **Hot Carrier Injection Issue** at 3.3V → Use of Level Shifters for Digital Pads
- **ESD protections** and **cold-spare** for IO pads

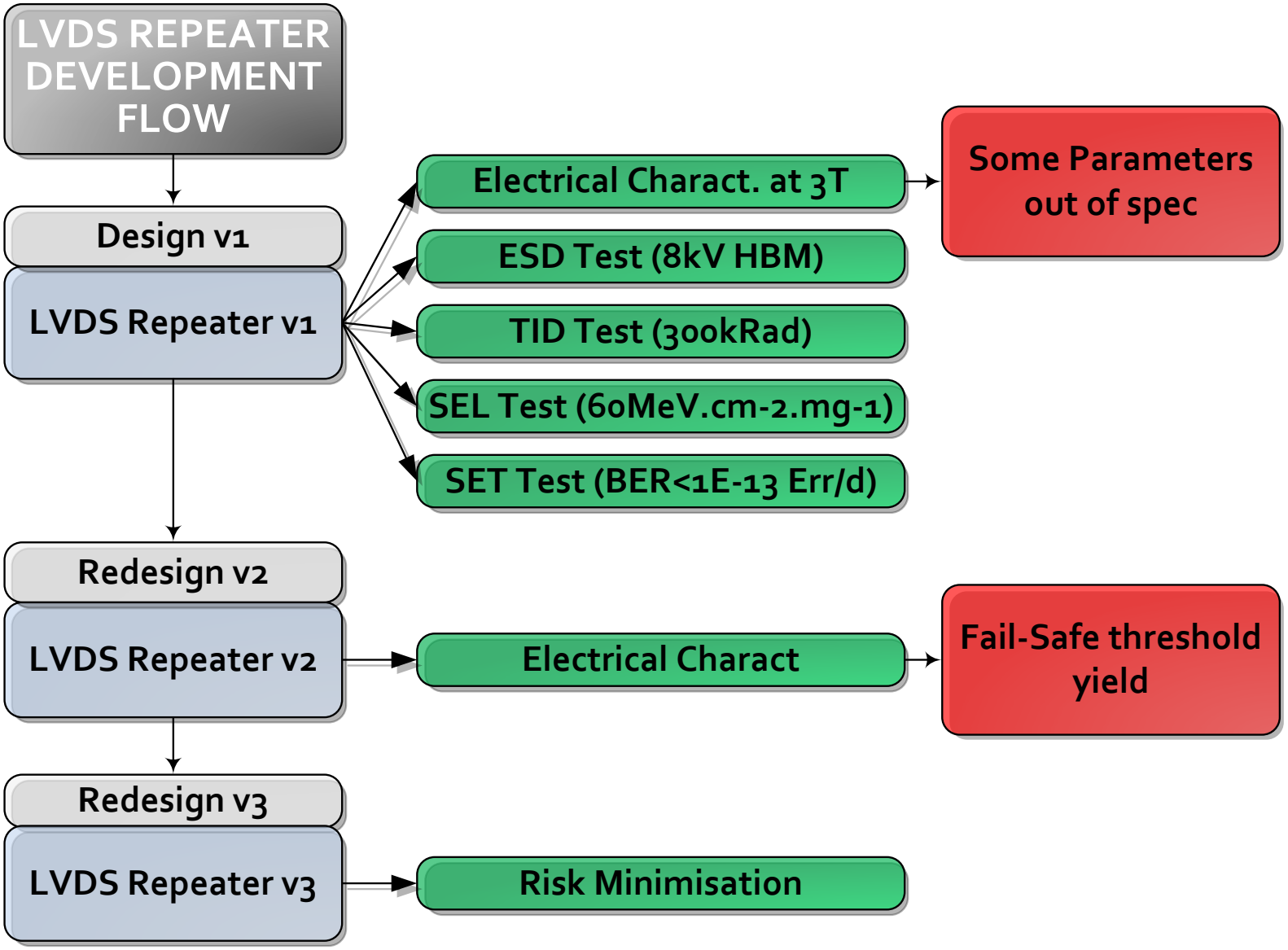
# LVDS REPEATER
## Implementation

### DEVELOPMENT FLOW



# LVDS REPEATER

## Implementation



# LVDS REPEATER
Implementation

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## REDESIGN

- **ESD protection improvement** to lower **cold-spare leakage** current
- **Passive circuits slight modifications** to improve **Jitter, Iccz** and **Ioz**
- **Active circuit update** with know topologies to improve:

  **Differential Output Voltage** (**VOD**) at low temperature

  **Vt Input threshold** including Hysteresis

  **Fail-safe Voltage Threshold** (Extensive simulation to insure the yield)

## RISK MINIMISATION

- **Extensive simulation** in corners, Montecarlo
- Very Low **Parametric Risk**
- Very Low **TID Risk**
- Very Low **ESD risk**
- Very Low **SEE risk**
- **Metal Fix** possibility

# LVDS REPEATER

Results

## GENERAL PERFORMANCES

**Low Power Consumption** (<100mA)

**High speed Operation** (tested up to 800Mbps)

**8kV HBM ESD** protection and **rad-hard** design

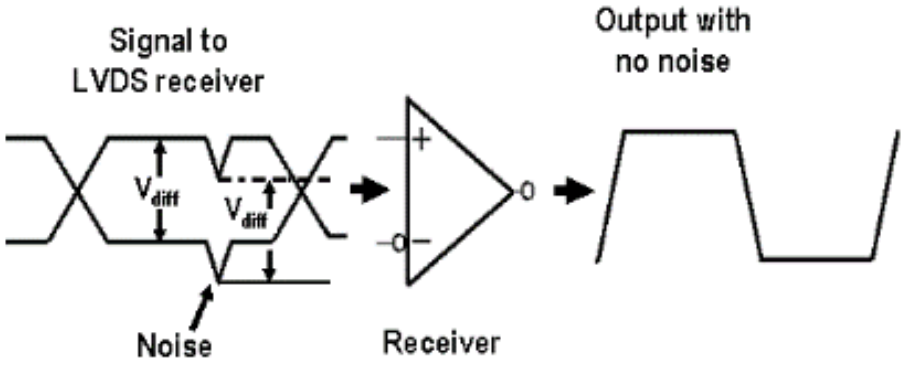
## RECEIVER PERFORMANCES

**25mV input Hysteresis** (impact in Noise performance)

**Cold Spare protection** (avoid failure propagation in case of shut-off power supply)

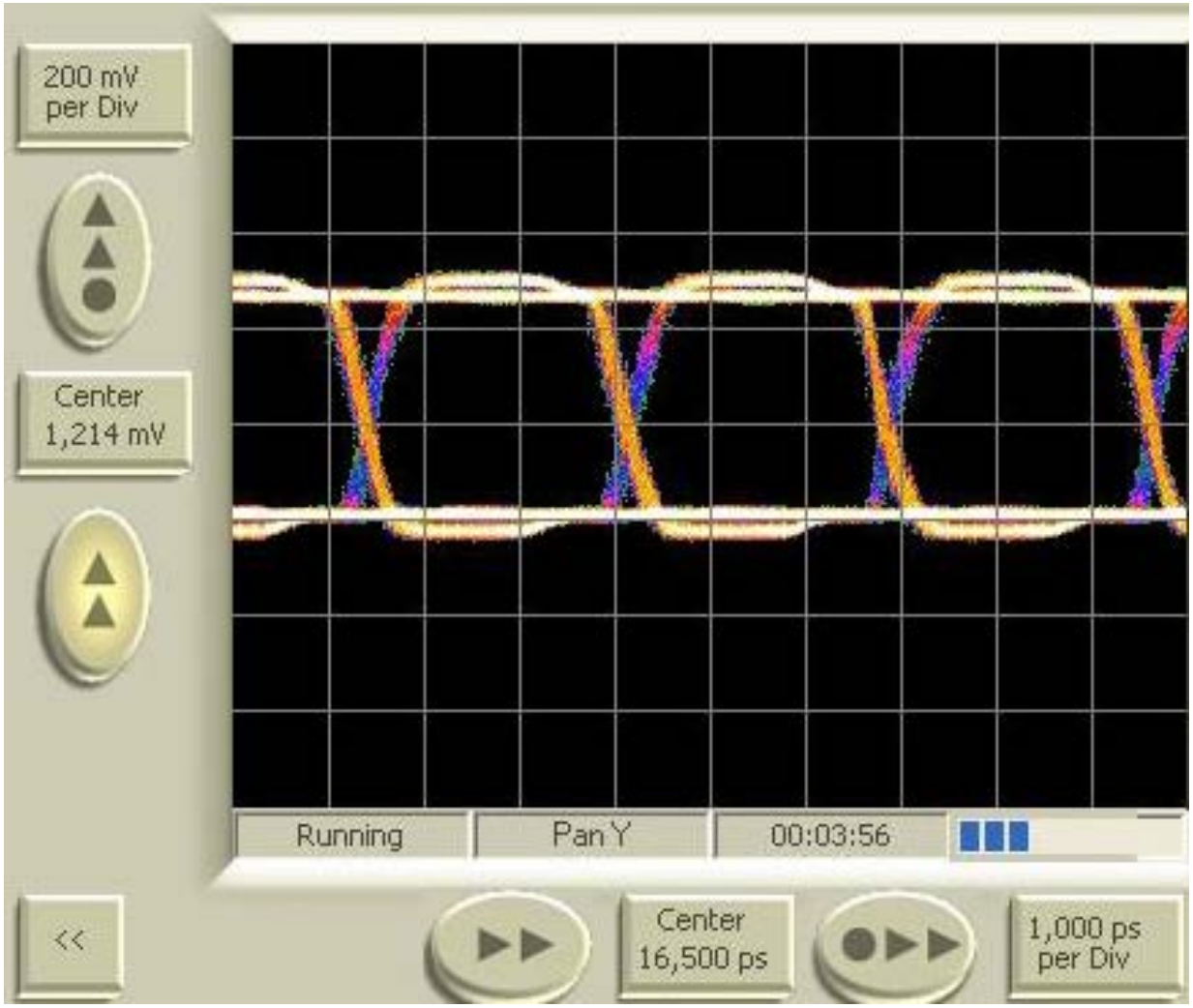
**Fail-Safe protection** (avoid failure propagation in case of SC or OC on differential Input lines)

**Extended Common Mode Range** (-4V to 5V; Good behavior against **EM and Ground bouncing**)



# LVDS REPEATER
Results

## EYE DIAGRAM (400Mbps)



# LVDS REPEATER
## Flight Opportunities

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### PLATO (ESA program)

**Under Analysis** for potential use in the program

**Cold Spare buffer** for other non-cold-spare LVDS devices

**Low Power consumption** contrary to LVDM devices


**PLAnetary Transits and Oscillations of stars (PLATO)** is the third medium-class mission in ESA's Cosmic Vision programme. Its objective is to find and study a large number of extrasolar planetary systems, with emphasis on the properties of terrestrial planets in the habitable zone around solar-like stars.

# LVDS REPEATER

## EPPL Application

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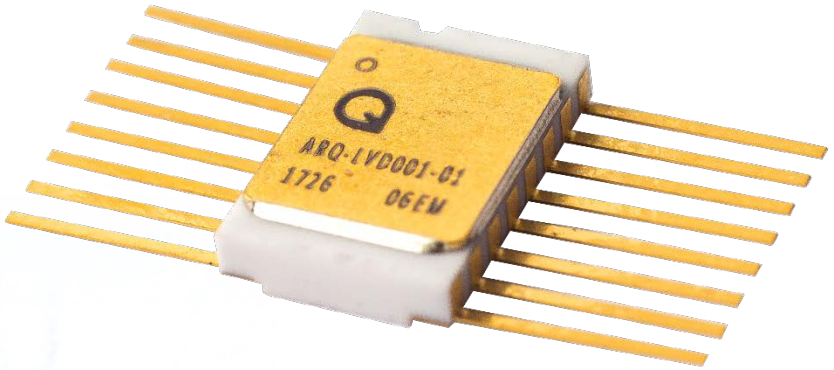
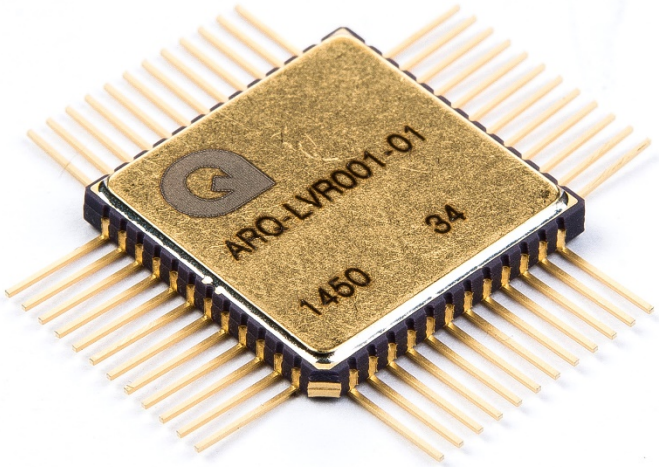
### EPPL Requirements

- ☒ **Potential use in flight hardware** (SpW)
- ☒ **Potential use for current or future program** (e.g. PLATO)
- ☒ **Space-Level Supply chain**
- ☒ **No Export Restriction** for ESCC user industries
- ☒ **No Notice of obsolescence**
- ☒ **Radiation performance**
- ☒ **Available US or European equivalents** (e.g. ST, COBHAM/AEROFLEX)

- ❑ **No Quality or Reliability problems** (High confidence)
- ❑ **Procurement Specification** (Pending Qualification)
- ❑ **ESCC Qualified or Evaluated Components** (LVDS Family)

# LVDS FAMILY



# LVDS FAMILY

## General

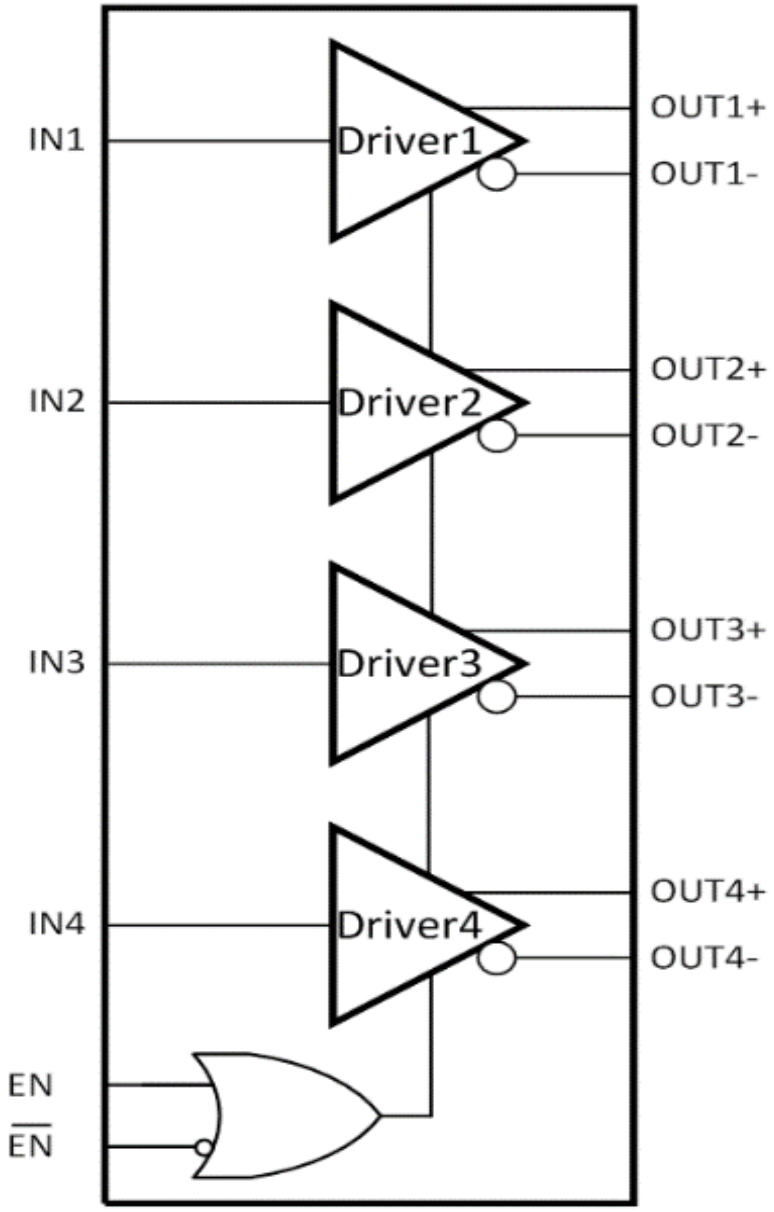
- **Development** and **qualification** of **European LVDS product family:**
  Driver, Receiver, Transceiver, Repeater
- ARQUIMEA's self-funded product development
  Using **synergies from ESA LVDS Repeater project**
- **Pin-to-pin compatible** with existing US products
- **Same package type** and **dimensions in all devices**
  (except Repeater CQFP-48 vs FP-48)
- **Fully European supply chain, ITAR-free**

# LVDS FAMILY

## General – Design

### BLOCK DIAGRAM

Quad Driver ARQ-LVD001

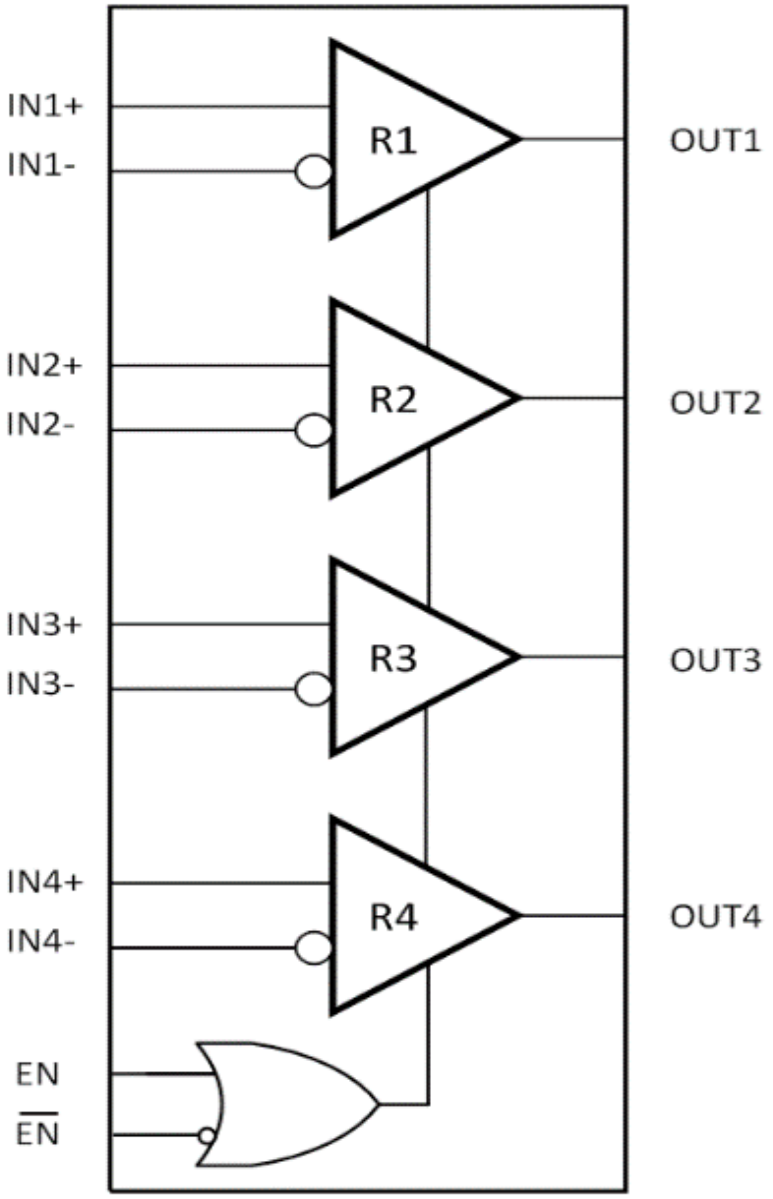


# LVDS FAMILY

## General – Design

### BLOCK DIAGRAM

Quad Receiver ARQ-LVR002

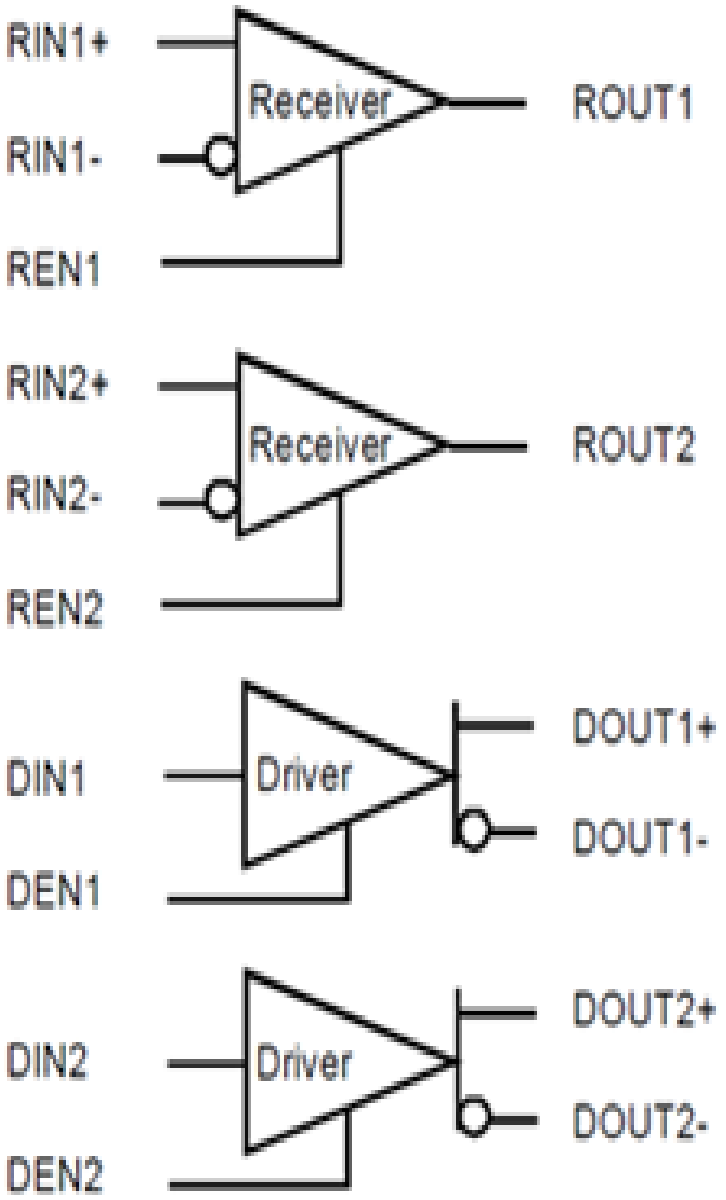


# LVDS FAMILY

General – Design

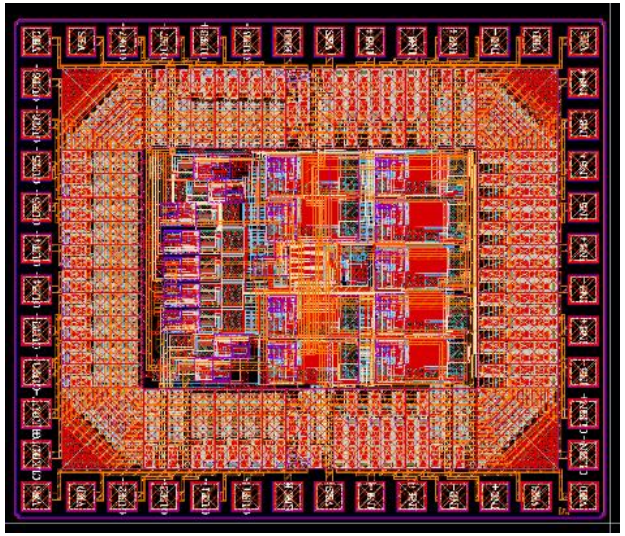
## BLOCK DIAGRAM

Quad Transceiver ARQ-LVT001

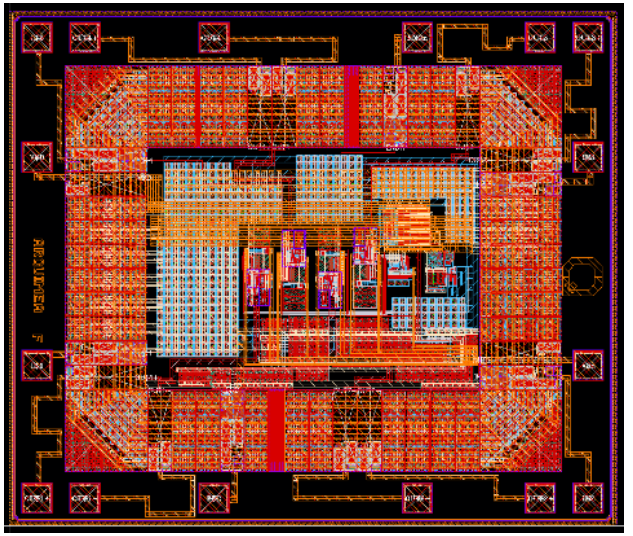


# LVDS FAMILY

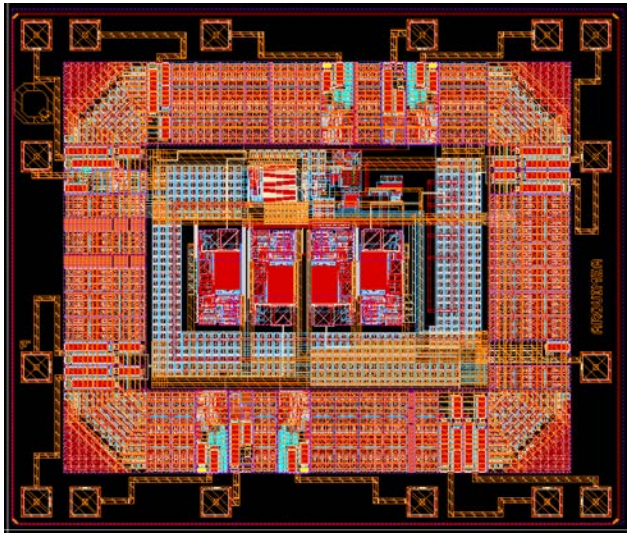
## General – Layout



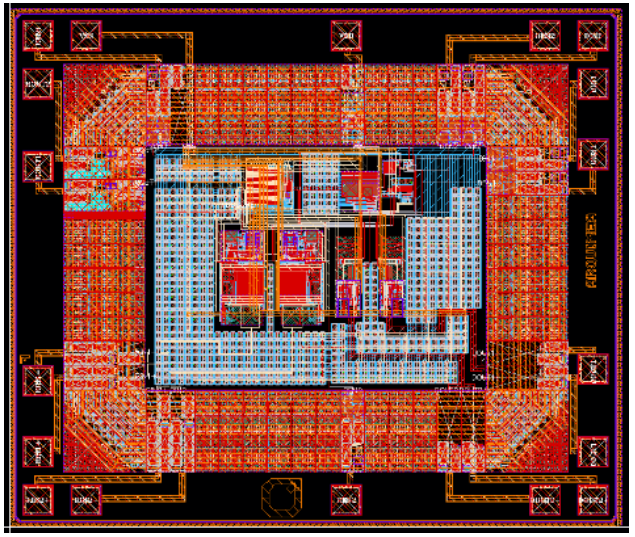
Octal Repeater ARQ-LVP001



Quad Driver ARQ-LVD001



Quad Receiver ARQ-LVR002

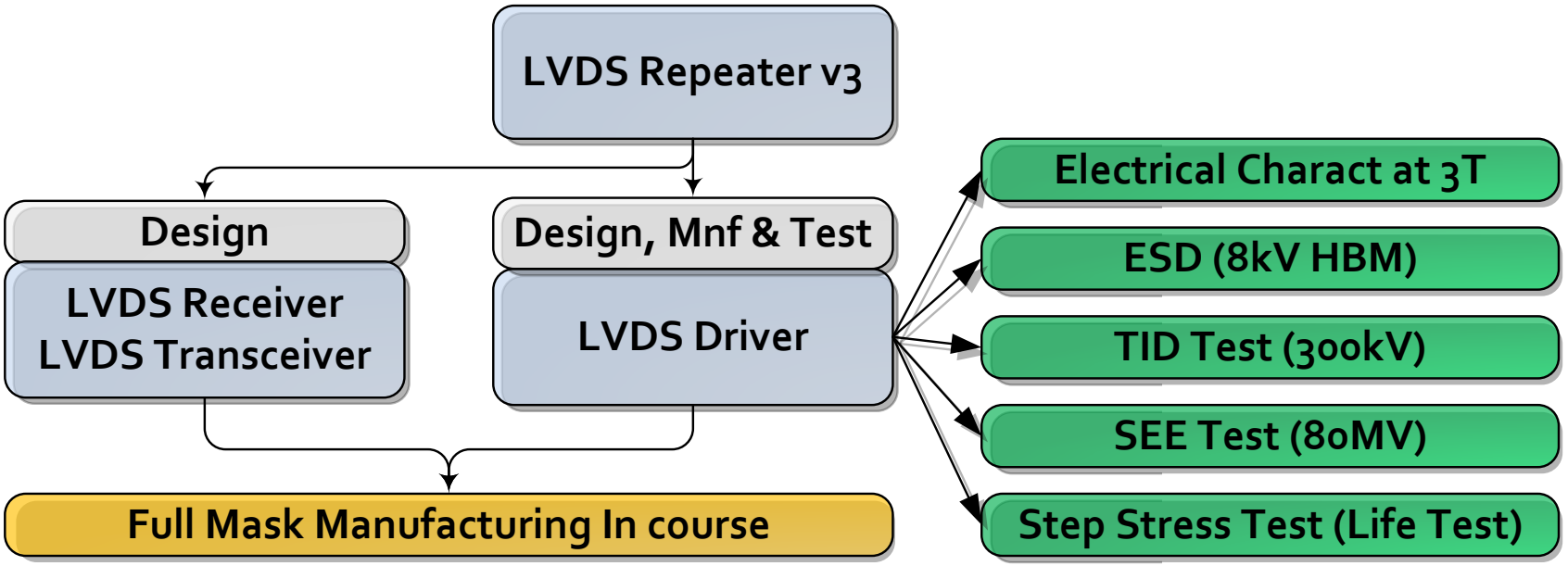


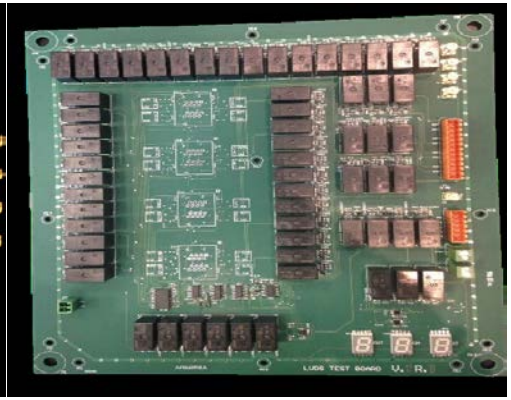
Dual Transceiver ARQ-LVT001

# LVDS FAMILY

## Development Status

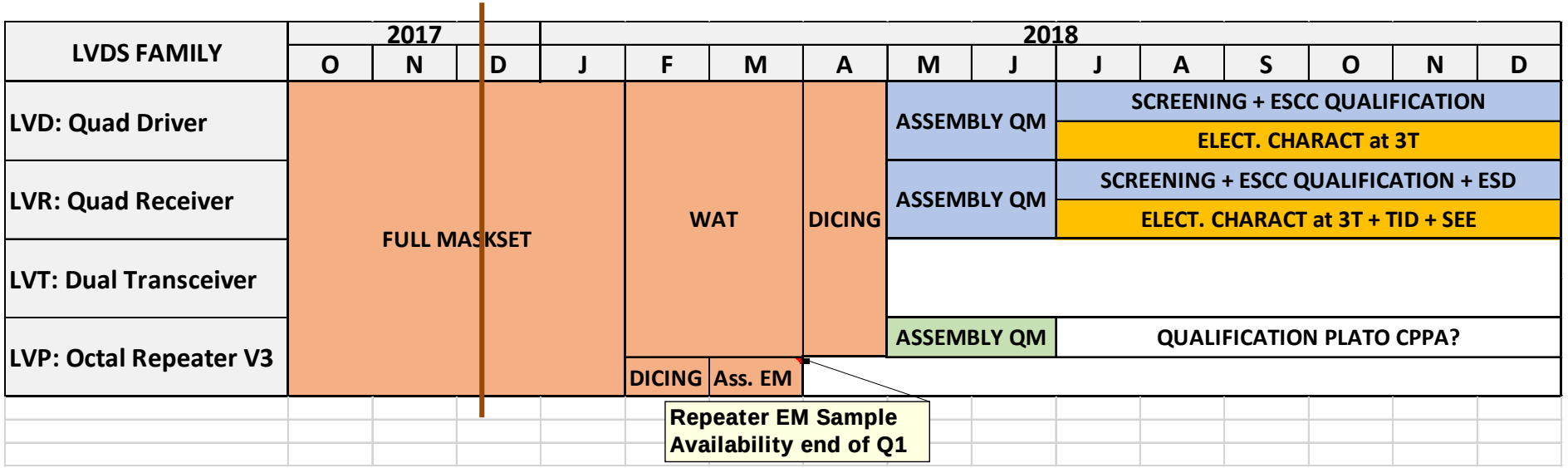




# LVDS FAMILY

## Development Status




| | |
|---|---|
| | MICROSS |
| | HCM |
| | IHP |
| | ARQ |

# LVDS FAMILY

## Development Status

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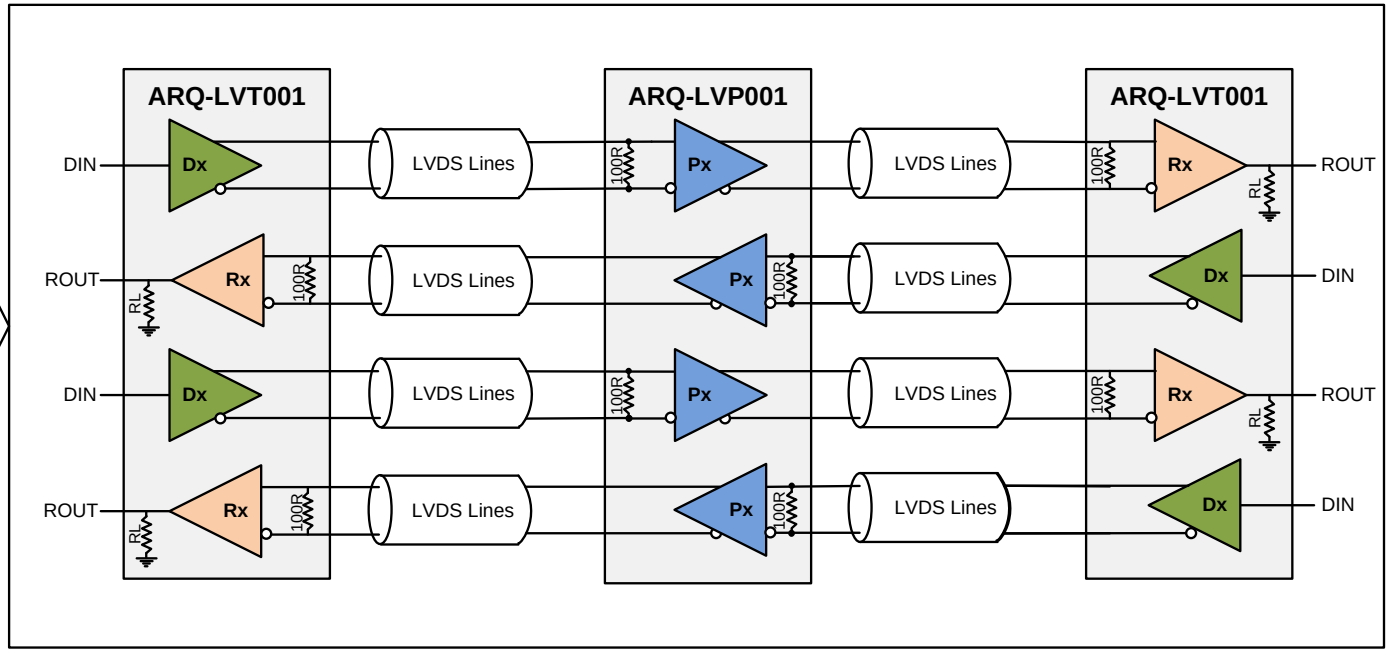
**DEMONSTRATION KIT based on ECSS-E-ST-50-12 (SpW standard)**

- LVDS devices **emulation**
- **Cabling (type, length)** and **connectors** effects on performances

  Verification of **PHY layer** & Data **Transfer protocol**
- **Compatibility verification** with other LVDS devices

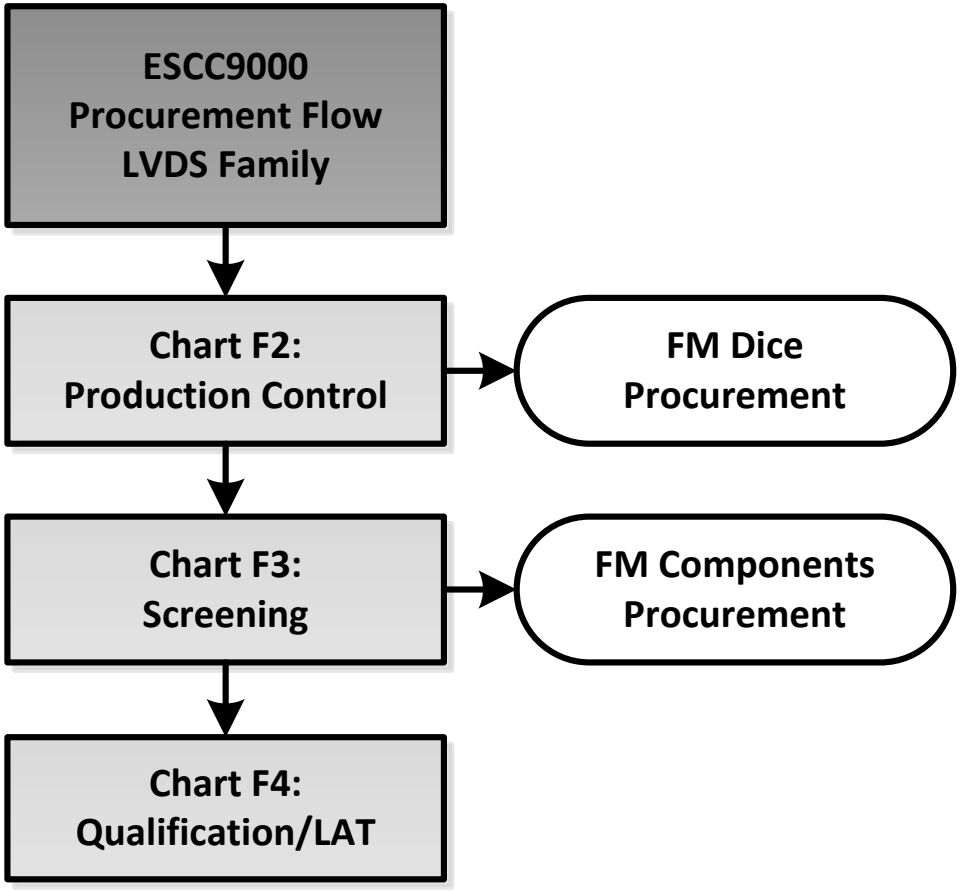
Space-wire Controller Signal Link Analyzer



# LVDS FAMILY

## Procurement Flow

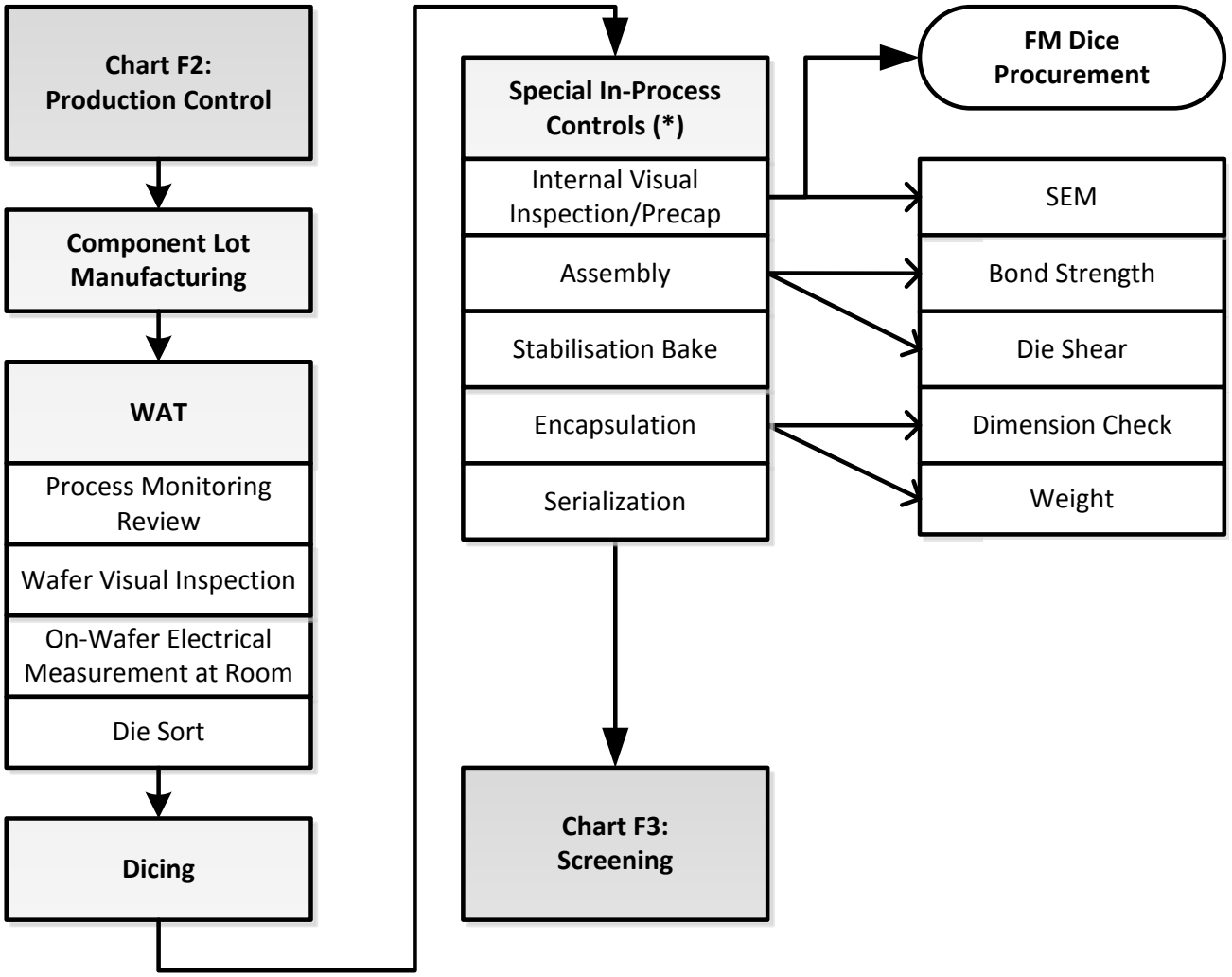
### GENERAL



# LVDS FAMILY

## Procurement Flow

## PRODUCTION CONTROL



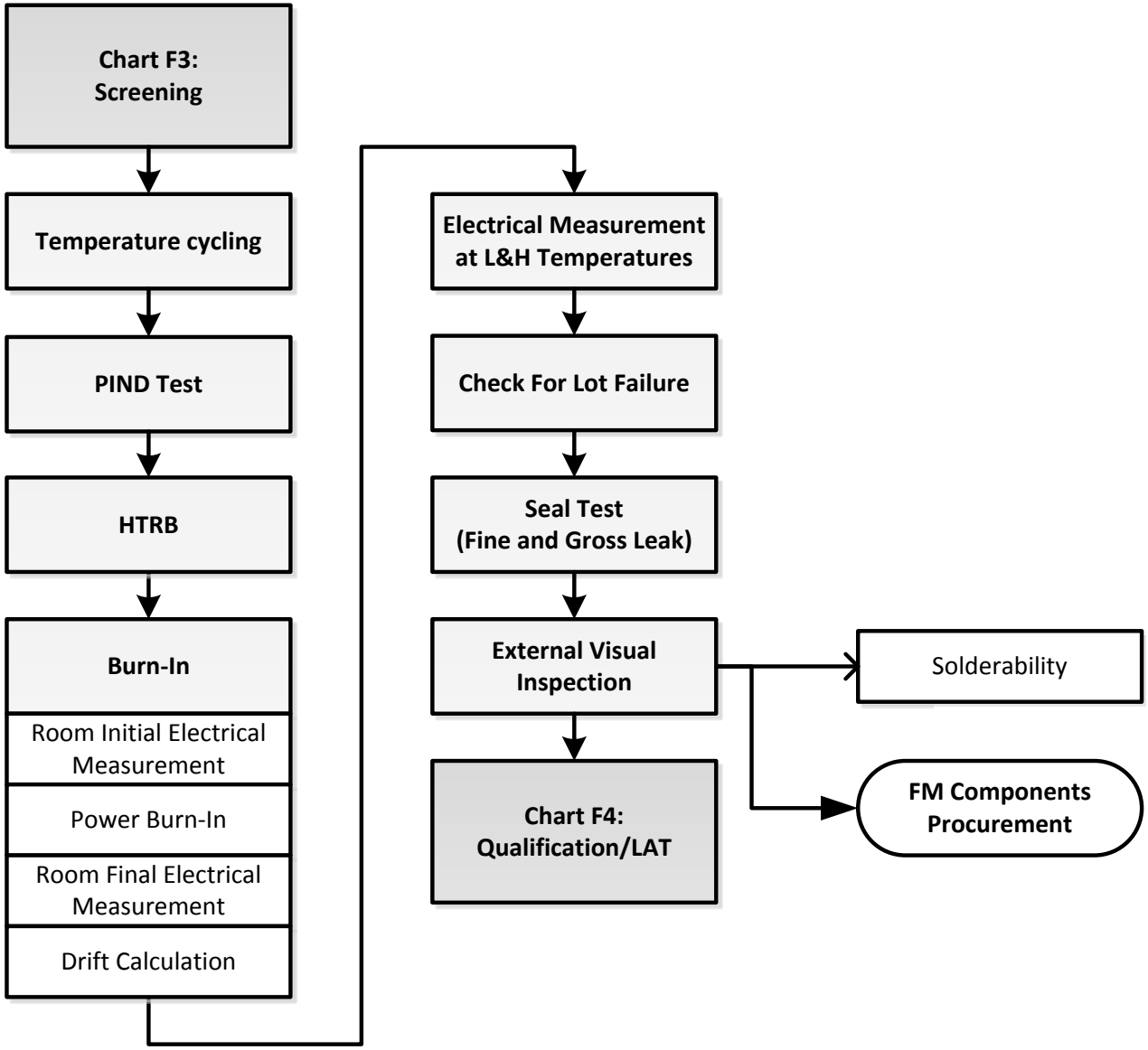

**Notes:**

**(*) Precap Inspection can be proposed to third party**

# LVDS FAMILY

## Procurement Flow

## SCREENING



# LVDS FAMILY
## Procurement Flow

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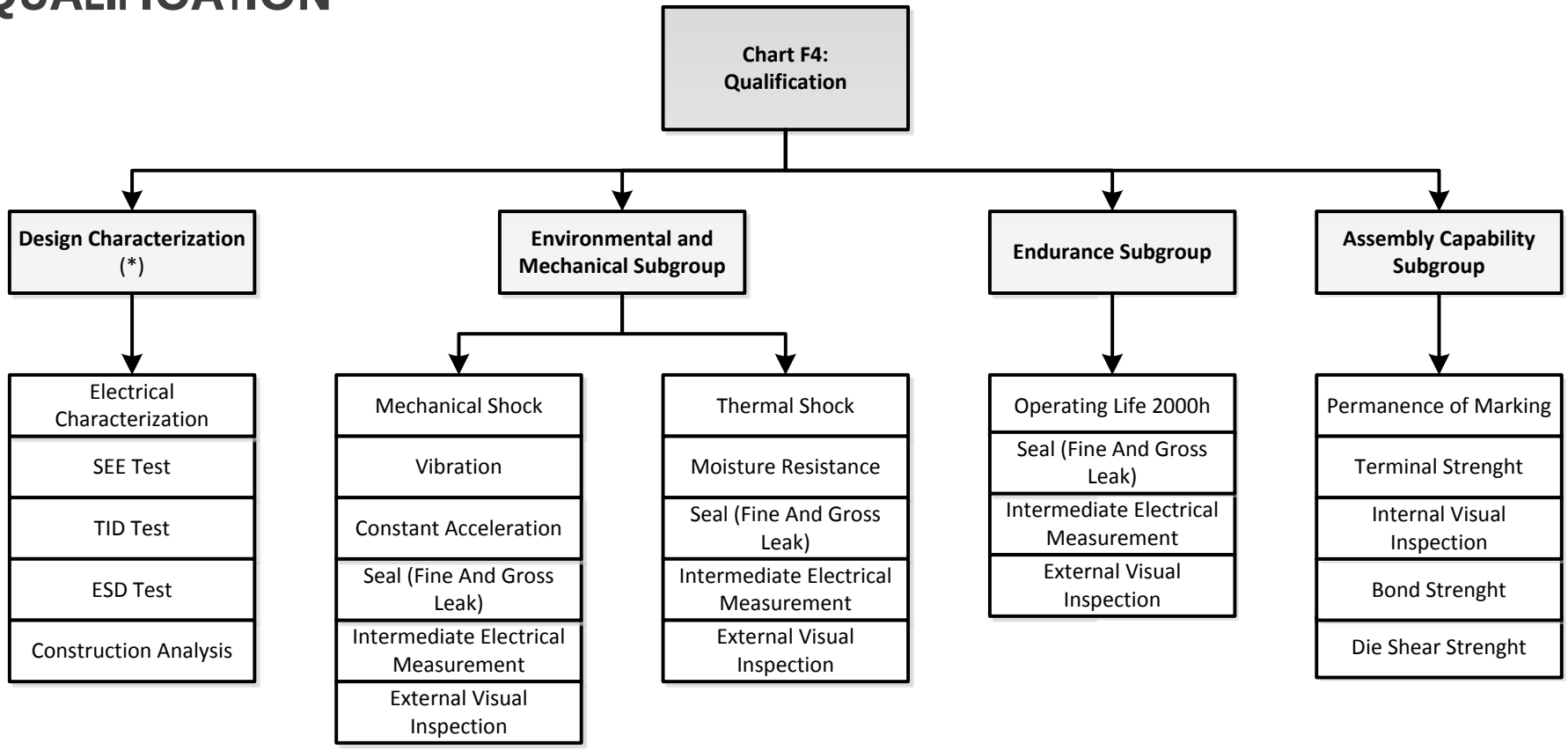
## QUALIFICATION




** If no representative data available*

# LVDS FAMILY

## Results & Conclusions

- ✓ **LVDS Octal Repeater** – ESA project **successfully completed**
- ✓ Additionally, an **entire LVDS family** was developed

  **Driver, Receiver, Transceiver and Repeater**
- ✓ **Compatible** with US devices. **Key parameters improved**
- ✓ **Fully European** supply chain. ITAR free
- ✓ First **space-qualified chips** using IHP processes
- ✓ Development and **qualification ongoing**

  Samples and evaluation boards already available (Driver and Repeater)

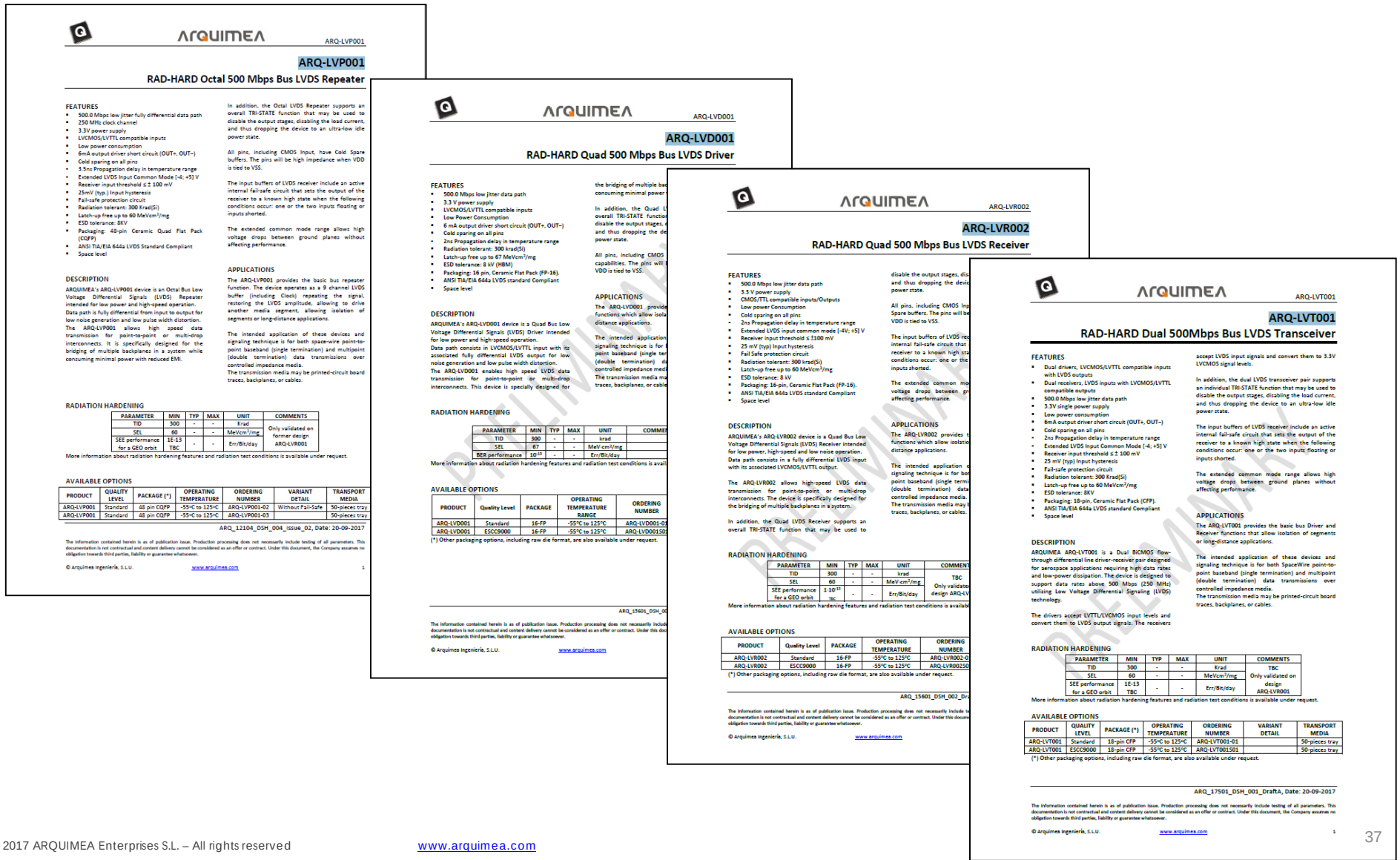
  QMs available in Q3-18

  FMs available in Q4-18

# LVDS FAMILY

## Results & Conclusions

## Preliminary Datasheets available



ARQUIMEA ARQ-LVP001

**ARQ-LVP001**

**RAD-HARD Octal 500 Mbps Bus LVDS Repeater**

FEATURES

- 500.0 Mbps low jitter fully differential data path
- 250 MHz clock channel
- 3.3V power supply
- LVCMOS/LVTTL compatible inputs
- Low power consumption
- 6mA output driver short circuit (OUT+, OUT–)
- Cold sparing on all pins
- 3.5ns Propagation delay in temperature range
- Extended LVDS Input Common Mode (-4; +5) V
- Receiver input threshold ≤ ± 100 mV
- 25mV (typ.) Input hysteresis
- Fail-safe protection circuit
- Radiation tolerant: 300 Krad(Si)
- Latch-up free up to 60 MeVcm²/mg
- ESD tolerance: 8KV
- Packaging: 48-pin Ceramic Quad Flat Pack (CQFP)
- ANSI TIA/EIA 644a LVDS Standard Compliant
- Space level

In addition, the Octal LVDS Repeater supports an overall TRI-STATE function that may be used to disable the output stages, disabling the load current, and thus dropping the device to an ultra-low idle power state.

All pins, including CMOS Input, have Cold Spare buffers. The pins will be high impedance when VDD is tied to VSS.

The input buffers of LVDS receiver include an active internal fail-safe circuit that sets the output of the receiver to a known high state when the following conditions occur: one or the two inputs floating or inputs shorted.

The extended common mode range allows high voltage drops between ground planes without affecting performance.

APPLICATIONS

The ARQ-LVP001 provides the basic bus repeater function. The device operates as a 9 channel LVDS buffer (including Clock) repeating the signal, restoring the LVDS amplitude, allowing to drive another media segment, allowing isolation of segments or long-distance applications.

The intended application of these devices and signaling technique is for both space-wire point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.
The transmission media may be printed-circuit board traces, backplanes, or cables.

DESCRIPTION

ARQUIMEA's ARQ-LVP001 device is an Octal Bus Low Voltage Differential Signals (LVDS) Repeater intended for low power and high-speed operation.
Data path is fully differential from input to output for low noise generation and low pulse width distortion.
The ARQ-LVP001 allows high speed data transmission for point-to-point or multi-drop interconnects. It is specifically designed for the bridging of multiple backplanes in a system while consuming minimal power with reduced EMI.

RADIATION HARDENING

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| TID | 300 | - | - | Krad | Only validated on former design ARQ-LVR001 |
| SEL | 60 | - | - | MeVcm²/mg | |
| SEE performance for a GEO orbit | 1E-13 | - | - | Err/Bit/day | |
| | TBC | | | | |

More information about radiation hardening features and radiation test conditions is available under request.

AVAILABLE OPTIONS

| PRODUCT | QUALITY LEVEL | PACKAGE (*) | OPERATING TEMPERATURE | ORDERING NUMBER | VARIANT DETAIL | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| ARQ-LVP001 | Standard | 48 pin CQFP | -55ºC to 125ºC | ARQ-LVP001-02 | Without Fail-Safe | 50-pieces tray |
| ARQ-LVP001 | Standard | 48 pin CQFP | -55ºC to 125ºC | ARQ-LVP001-03 | | 50-pieces tray |

ARQ_12104_DSH_004_issue_02, Date: 20-09-2017





ARQUIMEA ARQ-LVD001

**ARQ-LVD001**

**RAD-HARD Quad 500 Mbps Bus LVDS Driver**

FEATURES

- 500.0 Mbps low jitter data path
- 3.3 V power supply
- LVCMOS/LVTTL compatible inputs
- Low Power Consumption
- Cold sparing on all pins
- 2ns Propagation delay in temperature range
- Radiation tolerant: 300 krad(Si)
- Latch-up free up to 67 MeVcm²/mg
- ESD tolerance: 8 kV (HBM)
- Packaging: 16 pin, Ceramic Flat Pack (FP-16).
- ANSI TIA/EIA 644a LVDS standard Compliant
- Space level

DESCRIPTION

ARQUIMEA's ARQ-LVD001 device is a Quad Bus Low Voltage Differential Signals (LVDS) Driver intended for low power and high-speed operation.
Data path consists in LVCMOS/LVTTL input with its associated fully differential LVDS output for low noise generation and low pulse width distortion.
The ARQ-LVD001 enables high speed LVDS data transmission for point-to-point or multi-drop interconnects. This device is specially designed for

RADIATION HARDENING

| PARAMETER | MIN | TYP | MAX | UNIT | COMME |
|---|---|---|---|---|---|
| TID | 300 | - | - | krad | |
| SEL | 67 | - | - | MeV·cm²/mg | |
| BER performance | $10^{-13}$ | - | - | Err/Bit/day | |

More information about radiation hardening features and radiation test conditions is avail

AVAILABLE OPTIONS

| PRODUCT | Quality Level | PACKAGE | OPERATING TEMPERATURE RANGE | ORDERING NUMBER |
|---|---|---|---|---|
| ARQ-LVD001 | Standard | 16-FP | -55ºC to 125ºC | ARQ-LVD001-01 |
| ARQ-LVD001 | ESCC9000 | 16-FP | -55ºC to 125ºC | ARQ-LVD001501 |

(*) Other packaging options, including raw die format, are also available under request.

ARQ_15601_DSH_00



ARQUIMEA ARQ-LVR002

**ARQ-LVR002**

**RAD-HARD Quad 500 Mbps Bus LVDS Receiver**

FEATURES

- 500.0 Mbps low jitter data path
- 3.3 V power supply
- CMOS/TTL compatible inputs/Outputs
- Low power Consumption
- Cold sparing on all pins
- 2ns Propagation delay in temperature range
- Extended LVDS input common mode [-4V; +5] V
- Receiver input threshold ≤ ±100 mV
- 25 mV (typ) Input hysteresis
- Fail Safe protection circuit
- Radiation tolerant: 300 krad(Si)
- Latch-up free up to 60 MeVcm²/mg
- ESD tolerance: 8 kV
- Packaging: 16-pin, Ceramic Flat Pack (FP-16).
- ANSI TIA/EIA 644a LVDS standard Compliant
- Space level

DESCRIPTION

ARQUIMEA's ARQ-LVR002 device is a Quad Bus Low Voltage Differential Signals (LVDS) Receiver intended for low power, high-speed and low noise operation.
Data path consists in a fully differential LVDS input with its associated LVCMOS/LVTTL output.

The ARQ-LVR002 allows high-speed LVDS data transmission for point-to-point or multi-drop interconnects. The device is specifically designed for the bridging of multiple backplanes in a system.

In addition, the Quad LVDS Receiver supports an overall TRI-STATE function that may be used to

RADIATION HARDENING

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENT |
|---|---|---|---|---|---|
| TID | 300 | - | - | krad | TBC |
| SEL | 60 | - | - | MeV·cm²/mg | Only validate design ARQ-L |
| SEE performance for a GEO orbit | $1.10^{-13}$ TBC | - | - | Err/Bit/day | |

More information about radiation hardening features and radiation test conditions is availabl

AVAILABLE OPTIONS

| PRODUCT | Quality Level | PACKAGE | OPERATING TEMPERATURE | ORDERING NUMBER |
|---|---|---|---|---|
| ARQ-LVR002 | Standard | 16-FP | -55ºC to 125ºC | ARQ-LVR002-0 |
| ARQ-LVR002 | ESCC9000 | 16-FP | -55ºC to 125ºC | ARQ-LVR00250 |

(*) Other packaging options, including raw die format, are also available under request.

ARQ_15601_DSH_002_Dra



ARQUIMEA ARQ-LVT001

**ARQ-LVT001**

**RAD-HARD Dual 500Mbps Bus LVDS Transceiver**

FEATURES

- Dual drivers, LVCMOS/LVTTL compatible inputs with LVDS outputs
- Dual receivers, LVDS inputs with LVCMOS/LVTTL compatible outputs
- 500.0 Mbps low jitter data path
- 3.3V single power supply
- Low power consumption
- 6mA output driver short circuit (OUT+, OUT–)
- Cold sparing on all pins
- 2ns Propagation delay in temperature range
- Extended LVDS Input Common Mode (-4; +5) V
- Receiver input threshold ≤ ± 100 mV
- 25 mV (typ) Input hysteresis
- Fail-safe protection circuit
- Radiation tolerant: 300 Krad(Si)
- Latch-up free up to 60 MeVcm²/mg
- ESD tolerance: 8KV
- Packaging: 18-pin, Ceramic Flat Pack (CFP).
- ANSI TIA/EIA 644a LVDS standard Compliant
- Space level

accept LVDS input signals and convert them to 3.3V LVCMOS signal levels.

In addition, the dual LVDS transceiver pair supports an individual TRI-STATE function that may be used to disable the output stages, disabling the load current, and thus dropping the device to an ultra-low idle power state.

The input buffers of LVDS receiver include an active internal fail-safe circuit that sets the output of the receiver to a known high state when the following conditions occur: one or the two inputs floating or inputs shorted.

The extended common mode range allows high voltage drops between ground planes without affecting performance.

APPLICATIONS

The ARQ-LVT001 provides the basic bus Driver and Receiver functions that allow isolation of segments or long-distance applications.

The intended application of these devices and signaling technique is for both SpaceWire point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.
The transmission media may be printed-circuit board traces, backplanes, or cables.

DESCRIPTION

ARQUIMEA ARQ-LVT001 is a Dual BiCMOS flow-through differential line driver-receiver pair designed for aerospace applications requiring high data rates and low-power dissipation. The device is designed to support data rates above 500 Mbps (250 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The drivers accept LVTTL/LVCMOS input levels and convert them to LVDS output signals. The receivers

RADIATION HARDENING

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| TID | 300 | - | - | Krad | TBC |
| SEL | 60 | - | - | MeVcm²/mg | Only validated on design ARQ-LVR001 |
| SEE performance for a GEO orbit | 1E-13 | - | - | Err/Bit/day | |
| | TBC | | | | |

More information about radiation hardening features and radiation test conditions is available under request.

AVAILABLE OPTIONS

| PRODUCT | QUALITY LEVEL | PACKAGE (*) | OPERATING TEMPERATURE | ORDERING NUMBER | VARIANT DETAIL | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| ARQ-LVT001 | Standard | 18-pin CFP | -55ºC to 125ºC | ARQ-LVT001-01 | | 50-pieces tray |
| ARQ-LVT001 | ESCC9000 | 18-pin CFP | -55ºC to 125ºC | ARQ-LVT001501 | | 50-pieces tray |

(*) Other packaging options, including raw die format, are also available under request.

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ARQUIMEA

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