

## European LVDS IC Development



Contractor: Arquimea Ingeniería S.L.U.			ESA Budget:	520 k€
ECI Contract #4000105886			TO's: J. Ilstad, R. Dittrich,	
TRL	Initial: -	At Project Closure: 4	J. Beister (TEC-EDC)	



## **Objective:**

To develop, evaluate and qualify a rad-hard LVDS octal repeater by Arquimea (IHP SiGe 0.25µm technology). This was a parallel activity to the contract with Gaisler on UMC DARE180

## **Achievements:**

- Electrically functional silicon from 1<sup>st</sup> and 2<sup>nd</sup> design
- Parts successfully tested in TID
- Component went through several design updates/ fixes
- Electrical validation on v1 showed need for a redesign due to several non-compliances with planned spec.
- > CDR on v2 took place in January 2016. IHP MPW slot in February used for the manufacturing.
- Most non compliances were solved in the v2, however an issue with the failsafe behavior occured.

  Decision was taken to reallocate the remaining budget from electrical test to implement a design fix
- Failsafe issue solved in 3<sup>rd</sup> design, but further process of tape-out, manufacturing and testing was out of this activity, thus closure on design data with TRL 4.

## **Next steps:**

After project completion Arquimea continued with manufacturing, electrical and radiation testing of the 3<sup>rd</sup> design version.



Assembled LVDS test chip of first design version ARQ-LVR001-01 in CQFP48 package

ESA | 01/01/2016 | Slide 2

















