Radiation Characterization of DDR3 SDRAM and MRAM devices

- in the frame of
Contract 4000104887 "Technology Assessment of DRAM and Advanced Memory Products" -

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IDA TU Braunschweig

Outline

- Activity background
- Tests
- Tested devices
- Facilities and equipment
- Procedures and results
  - MRAM heavy-ion SEE
  - DDR3 SDRAM heavy-ion SEE
  - DDR3 SDRAM in-situ TID
- Conclusions

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Background

Technology Assessment of DRAM and Advanced Memory Products

Contract 4000104887

DEFENCE AND SPACE

13th December 2017

AIRBUS

Introduction

GOAL:

Characterize of the radiation hardness and the reliability of both, state of the art DRAM and advanced non-volatile memories in view of space applications.

Collaboration:

- Airbus Defense and Space (ADS), Elancourt (ELC) / Friedrichshafen (FHN)
- Thales Communications & Services (T3S), Toulouse
- Institut für Datentechnik und Kommunikationsnetze (IDA), Braunschweig
- Airbus Defense and Space (ADS), Bremen
- Airbus Group Innovation (AGI)

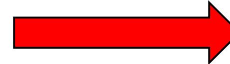
Comments:

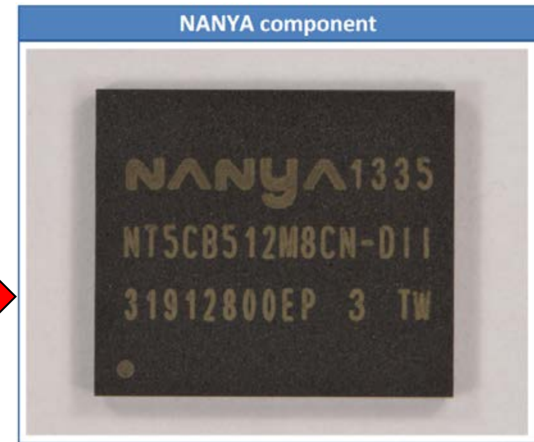
- Two Groups of activities:
  - Group A covering assessment of DRAM
  - Group A activities linked to ESA study T222-016QC “Radiation Hard Memory: Radiation Testing of Candidate Memory Devices for Laplace Mission” (RHM)
  - Group B covering assessment of NVM
  - Group B activities rearranged during the study

Work Package Description Group A

WP 1000: Product and reliability assessment of commercial DRAM parts

- WP1100: State of the art DRAM processes (ADS & AGI)
- WP1200: Reliability benchmarking (ADS & AGI)
- WP1300: Review of any DRAM radiation test results (ADS)
- WP1400: DRAM device selection (ADS)
- WP1500: RISK analysis (ADS)





WP 2000: Electrical and Radiation Characterization of the DRAM Device Type

- WP2100: Handling, Storage, Procurement Requirement (ADS)
- WP2200: Electrical Characterization (T3S)
- WP2300: Radiation Characterization (IDA)
  - Heavy Ion SEE Test
  - TID Test

WP 3000: Electrical and Radiation Characterization of the DRAM Device Type

- WP3100: DRAM ETP Definition (ADS)
- WP3200: DRAM ETP Execution (T3S)

Work Package Description Group B

WP 4000: Product and reliability assessment of commercial DRAM parts

- WP4100: State of the art NVM process technologies (IDA)
- WP4200: Reliability benchmarking (ADS)
- WP4300: Review of any NVM radiation test results (IDA & ADS)
- WP4400: Advanced NVM device selection (ADS)
- WP4500: RISK analysis (ADS)

WP 5000: Radiation Characterization of the DRAM Device Type

- WP5200: Review of any DRAM radiation test results (IDA)
  – Heavy Ion SEE Test

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Tests

Tests overview

Date	Type	Facility	Memories
11/2015	Heavy-ion SEE	RADEF	MRAM
4/2016	Heavy-ion SEE	RADEF	MRAM, DDR3
9/2016	In-situ TID	PTB	DDR3

Short Summary of Previous work – DDR3 (done in RHM study)

- TID:
- Hynix, Samsung: ≈400 krad (in-situ)
- Micron: ≈60 krad (in-situ)
- SEE:
- Hynix, Samsung
- SEE error mechanism with data loss: device SEFI
- No single-event latch-up, no destructive events

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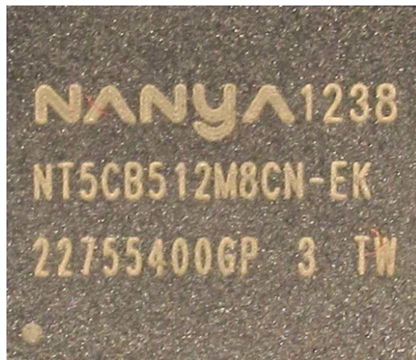
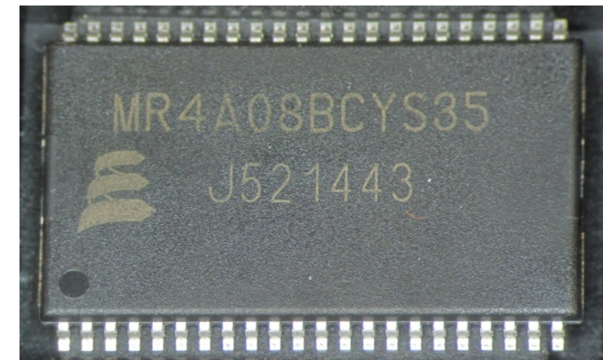
Tested devices

Tested device types

Label	Technology	Manufacturer	Capacity	Part number	Tests
Nan4	DDR3 SDRAM	Nanya	4 Gbit	NT5CB512M8C N-EK	SEE + TID
Es1	MRAM	Everspin	1 Mbit	MR0A08BCYS3 5	SEE
Es16	MRAM	Everspin	16 Mbit	MR4A08BCYS3 5	SEE



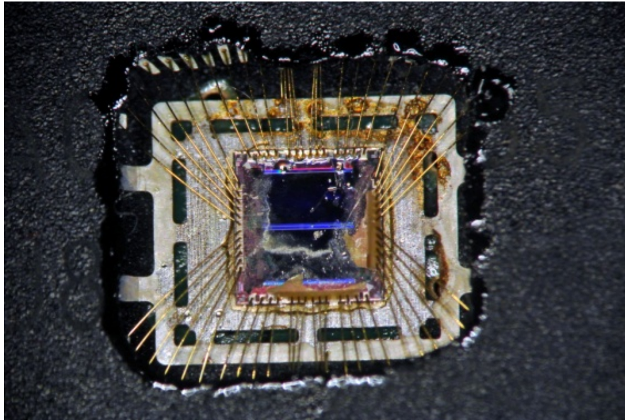


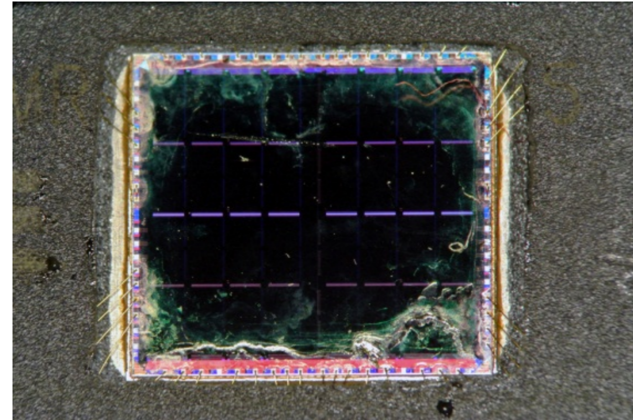
Sample preparation – DDR3

- Heavy-ion SEE test
  - Flip-chip BGA package – backside irradiation
  - Thinned to ≈ 60 µm
  - Performed by Fraunhofer IOF, Jena
- In-situ TID test
  - 8 samples soldered to SODIMM

Sample preparation – MRAM

- Heavy-ion SEE tests:
  - 0.8 mm TSOP package
  - Opened by nitric acid etching
  - Soldered to carrier PCB
  - Performed by IDA





Test modes

- Storage mode: write before irradiation, read after irradiation
- Read mode: continuous read during irradiation; errors accumulate in DUT
- Marching mode: during irradiation, immediately rewrite each cell with inverse and verify (read – write – verify)

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Test facilities and test equipment

Test facility – RADEF

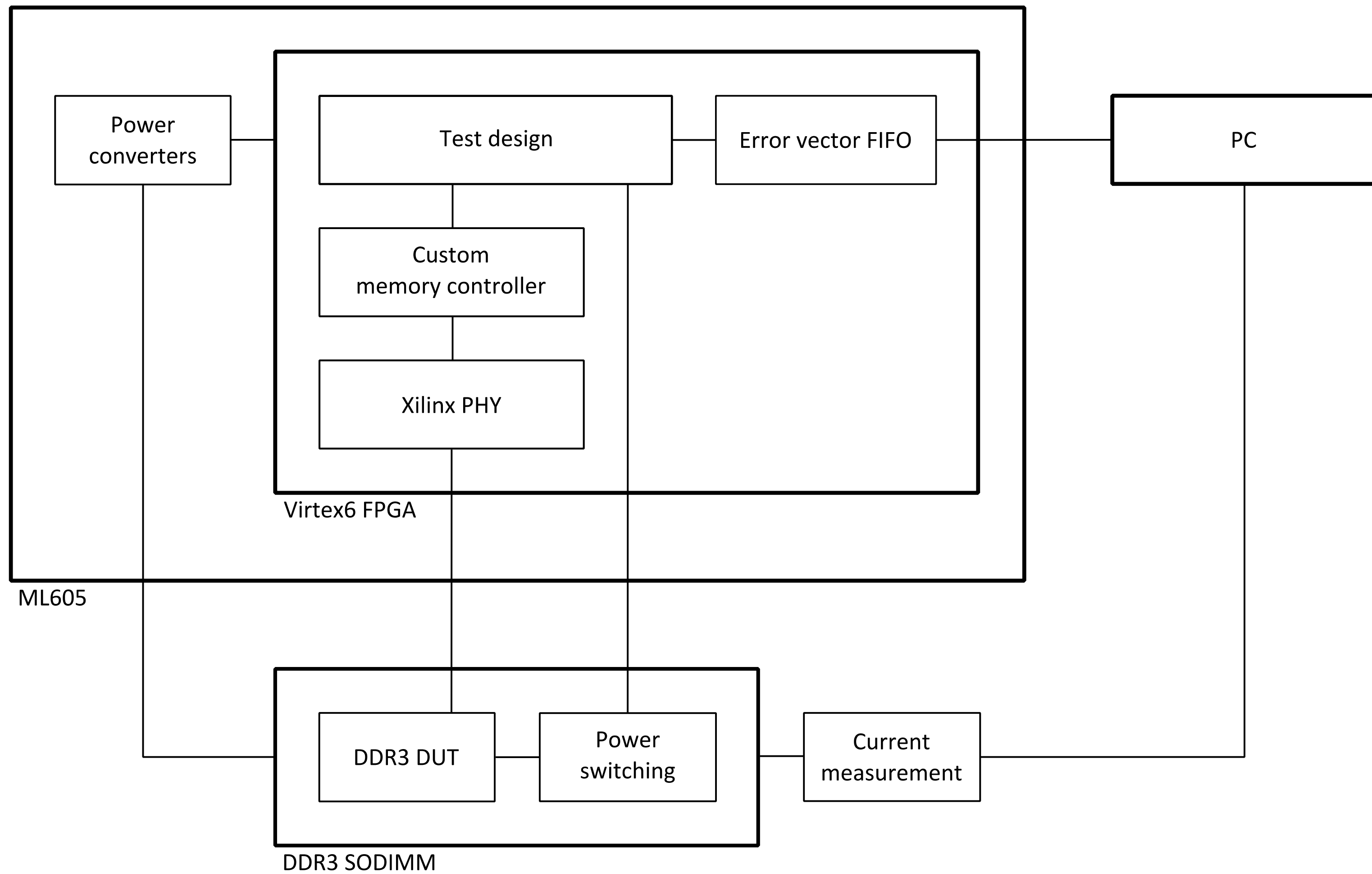
- 9.3 MeV/amu heavy-ion cocktail
- MRAM: Not all ions used due to time and source availability constraints

Ion	Energy [MeV]	Range [µm]	LET [MeV cm^2 mg^{-1}]	
			Surface	55 µm
^{15}N	139	202	1.8	2.2
^{20}Ne	186	146	3.6	4.5
^{40}Ar	372	118	10.2	12.9
^{56}Fe	523	97	18.5	25.3
^{82}Kr	768	94	32.2	39.8
^{131}Xe	1217	89	60.0	68.7

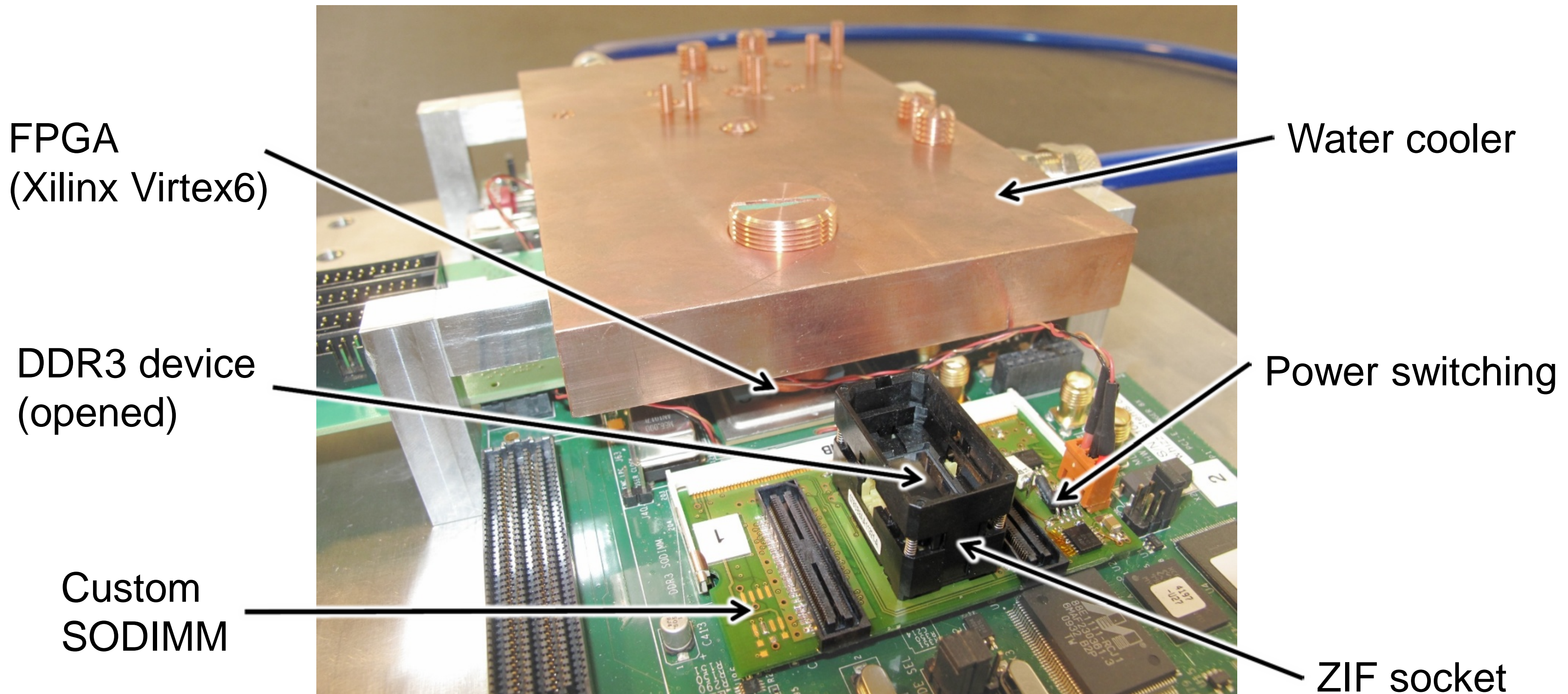
Test facility – PTB

- Physikalisch-technische Bundesanstalt, Braunschweig
- The national German metrology institute
- 2 krad/h (30 rad/min)

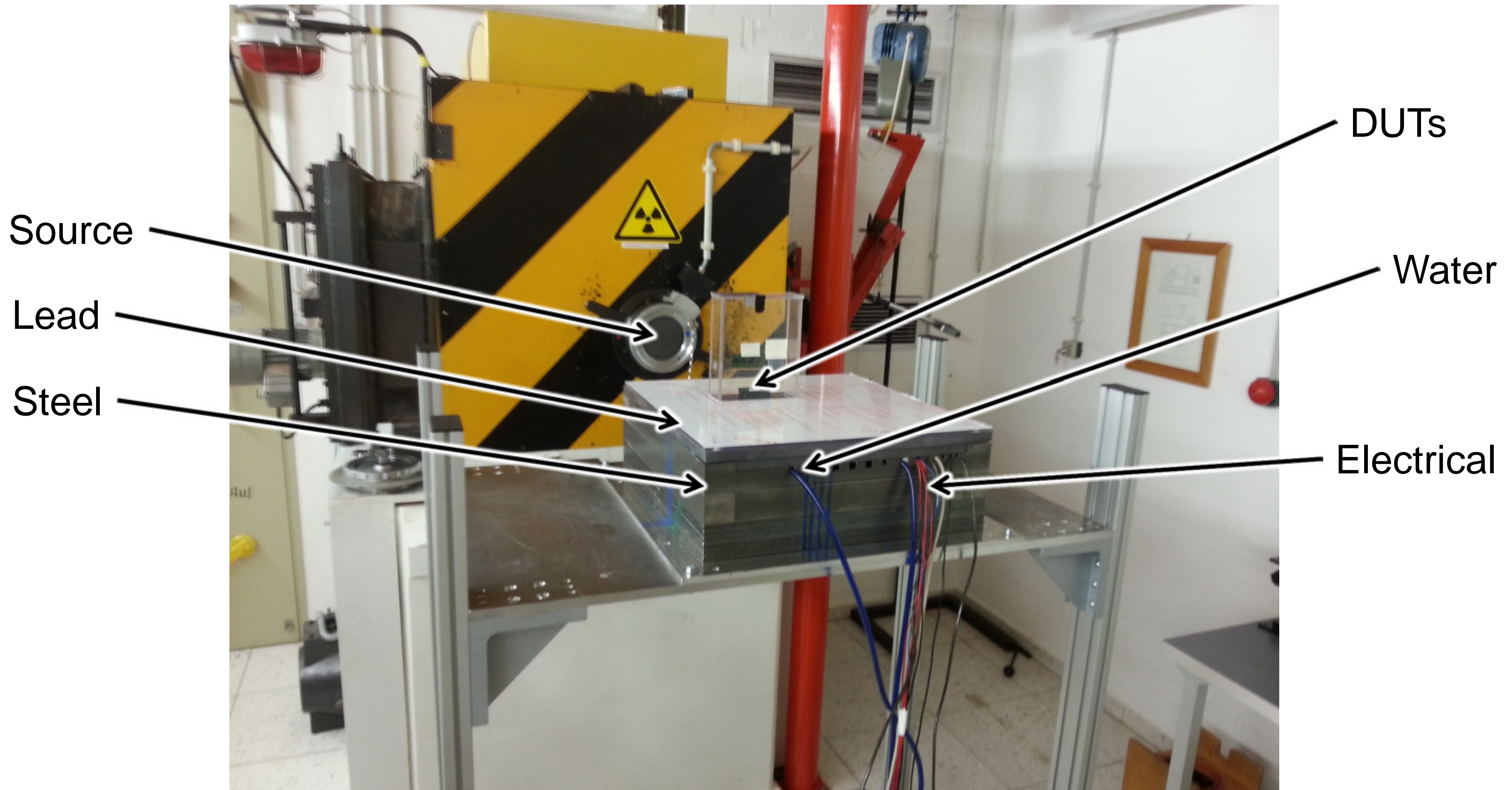
Test equipment – DDR3



Test equipment – DDR3 for SEE Test



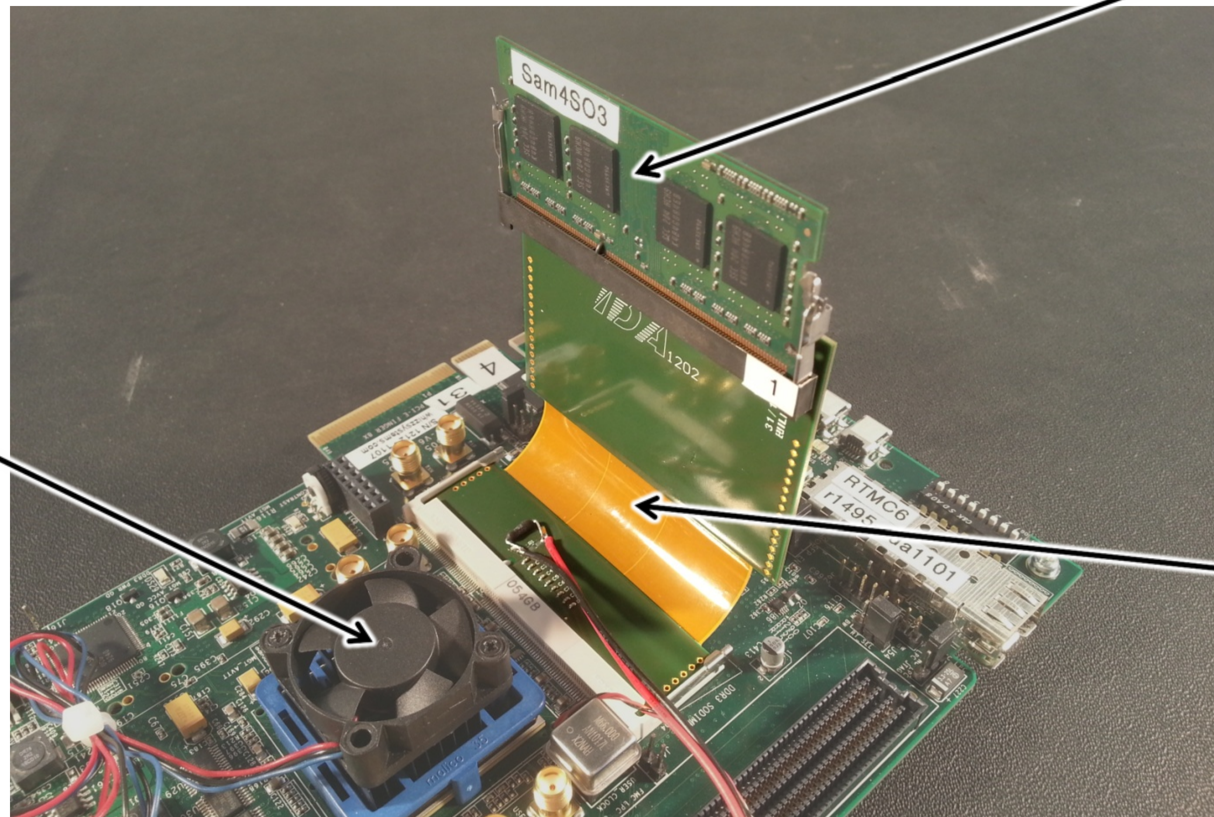
Test equipment – DDR3 TID



Test equipment – DDR3 TID

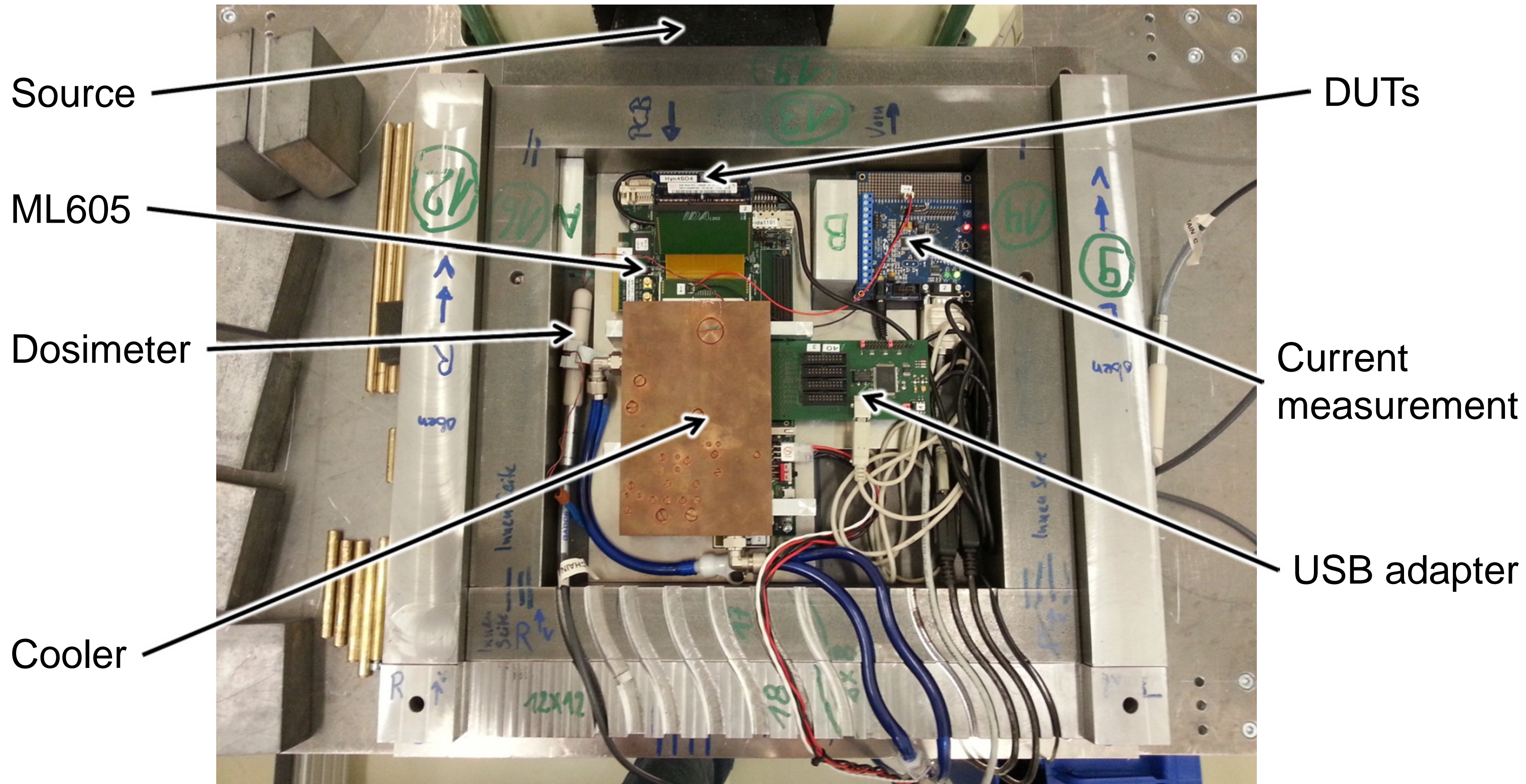
SODIMM DUT

FPGA
(Xilinx Virtex6)



Flexible
extension

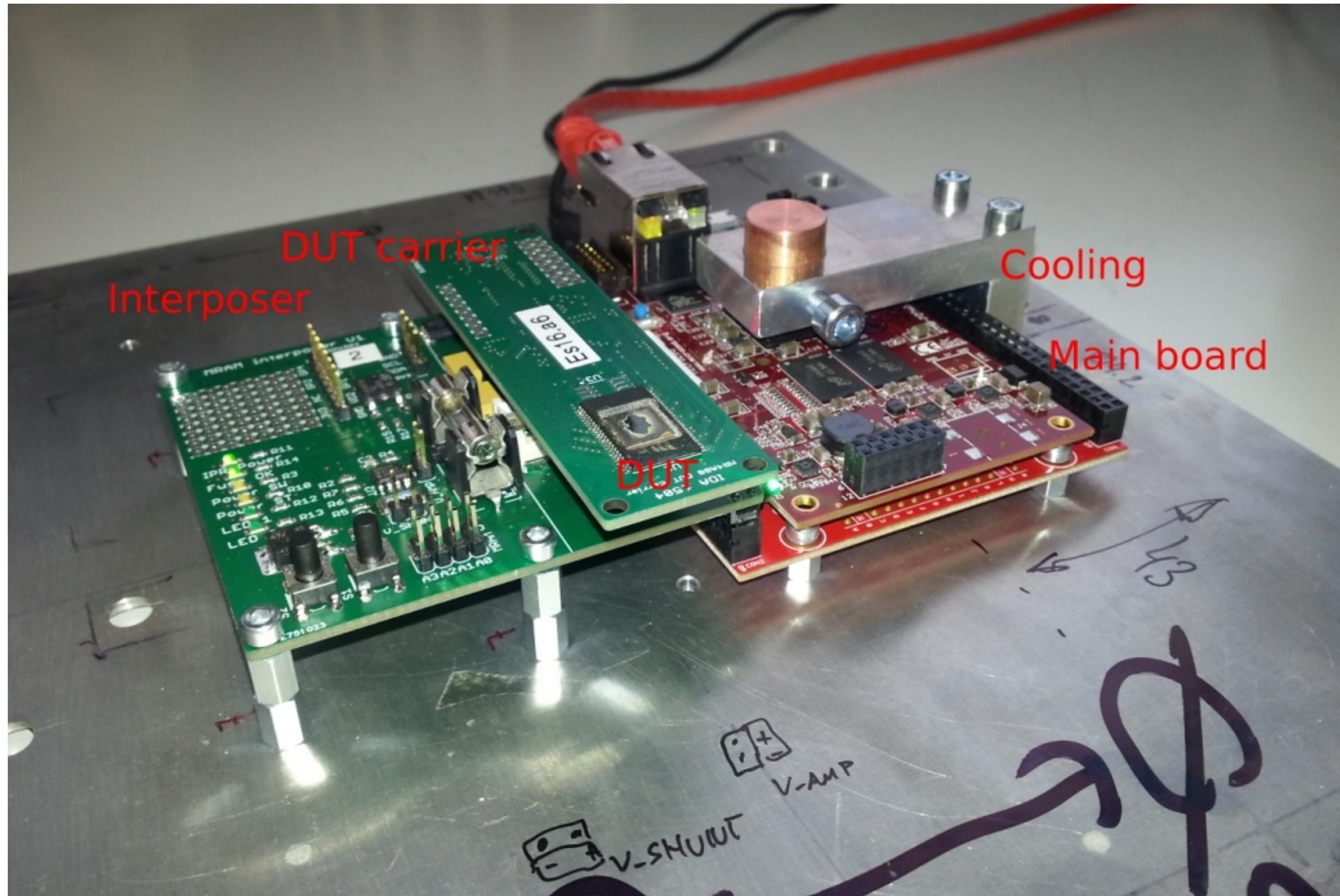
Test equipment – DDR3



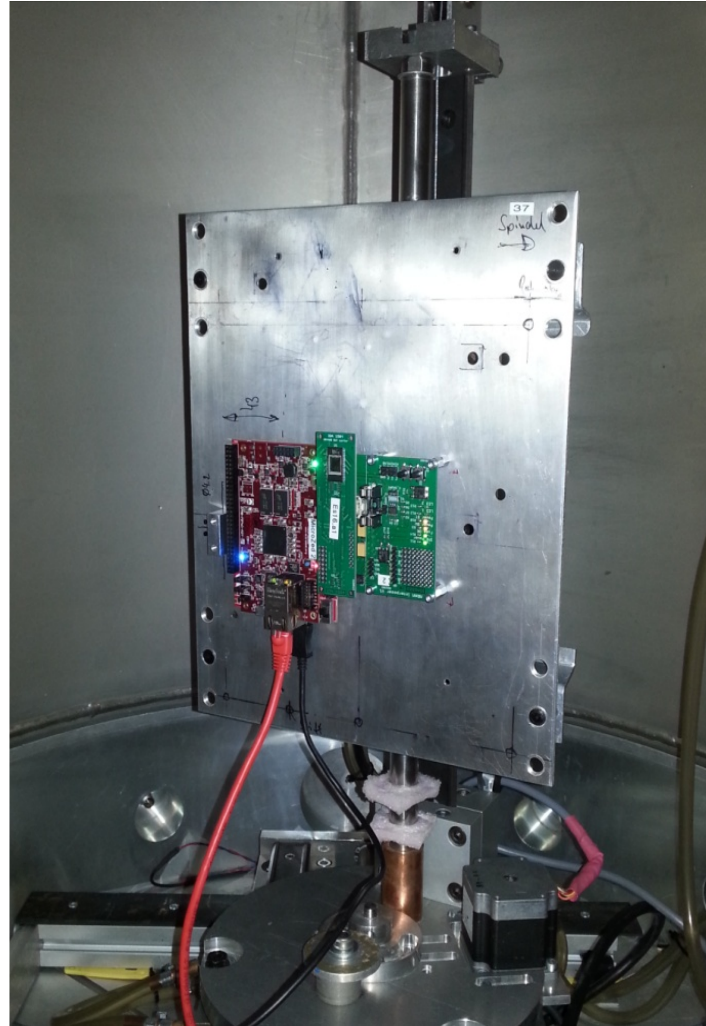
Test equipment – MRAM

- Xilinx Zynq-7000 AP SoC
  - FPGA
  - Dual-core ARM Cortex A9 (667 MHz)
  - Integrated dual 12-bit ADC
- Components:
  - Main board (Avnet MicroZed): Zynq, power supply, Ethernet
  - Interposer (custom PCB): power switching, current measurement
  - DUT carrier (custom PCB): DUT, ID EEPROM, temperature sensor
- Improvements over DDR3 tester:
  - Quick setup
  - Connection to PC via Ethernet
  - Small footprint

Test equipment – MRAM



Test equipment – MRAM



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Test procedures and test results

MRAM heavy-ion SEE

MRAM SEE – Test procedures

- Test conditions:
  - Test in vacuum without heating/cooling
  - Standard voltage 3.3 V
  - SRAM interface
  - Storage mode, read mode, marching mode
  - Pseudo-random pattern
  - Latch-up switch: 60 mA

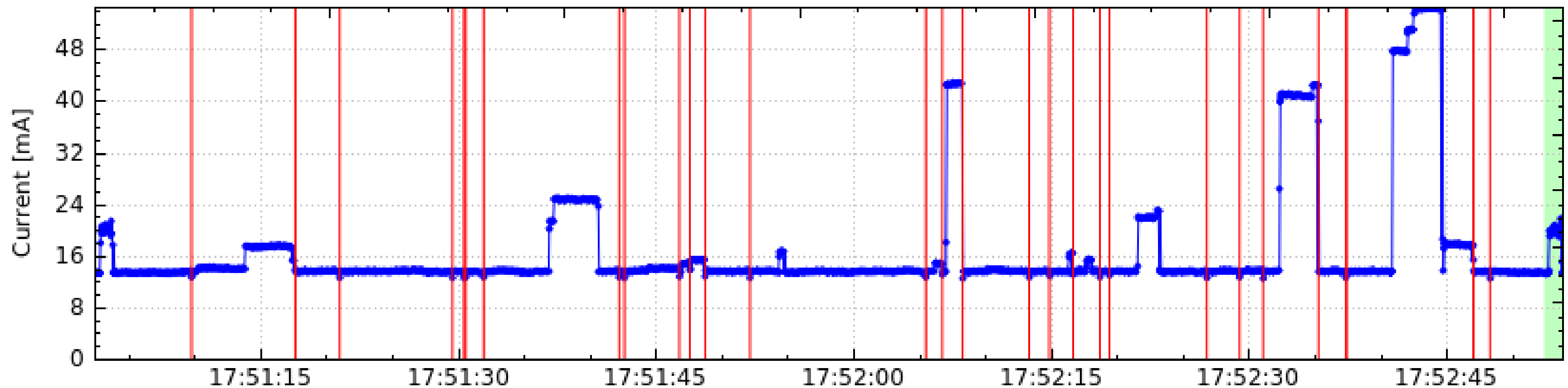
MRAM SEE – Error classification

- SEU (SBU or MBU)
- Stuck bit
- SEFI
  - no further distinction – linear address space
- Current increase

MRAM SEE – Current

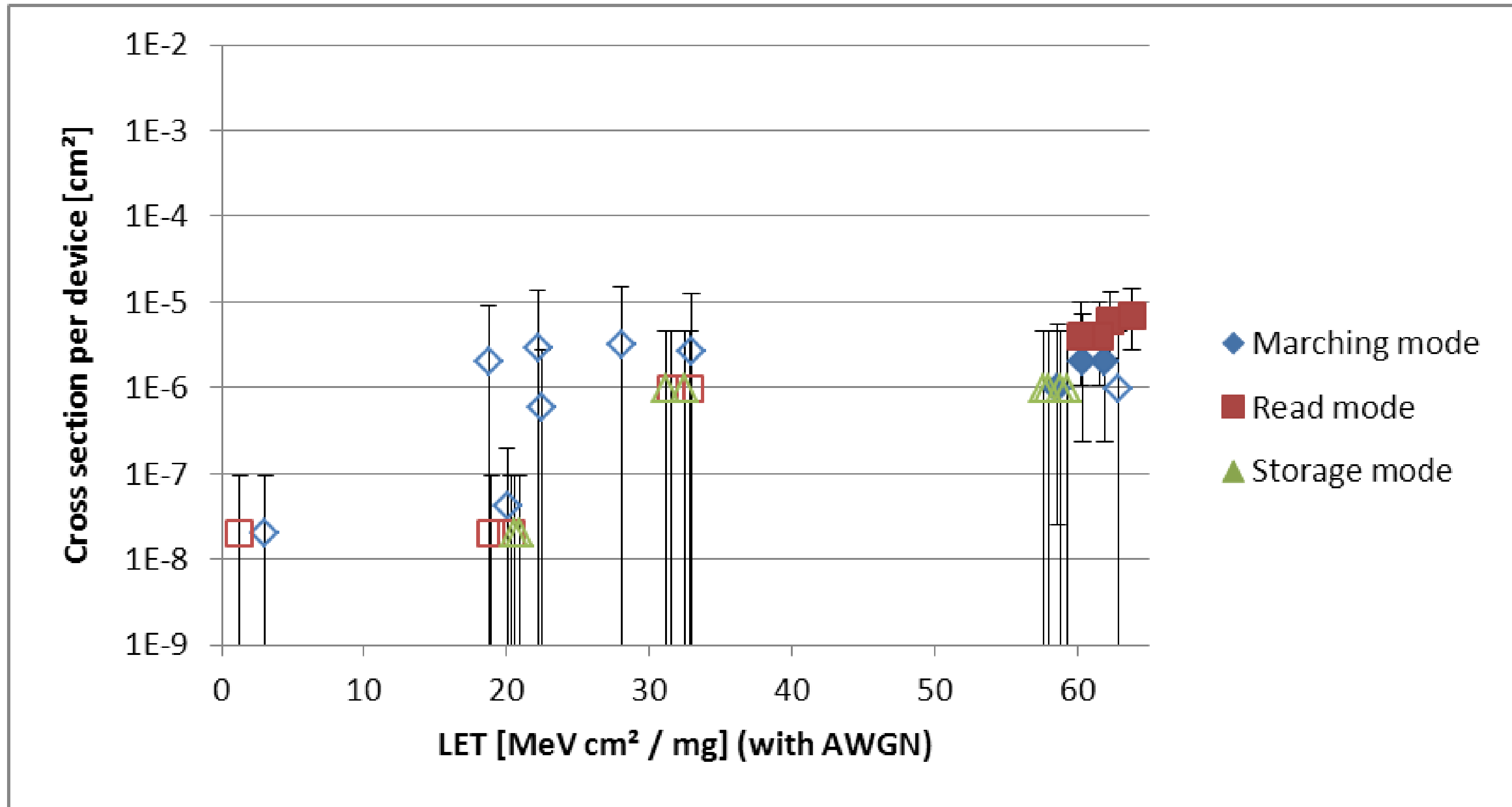
- Current increase observed
  - In steps
- Latch-up
  - Defined as current > 60 mA
  - Distinction from current increase by arbitrary threshold

MRAM SEE – Current increase



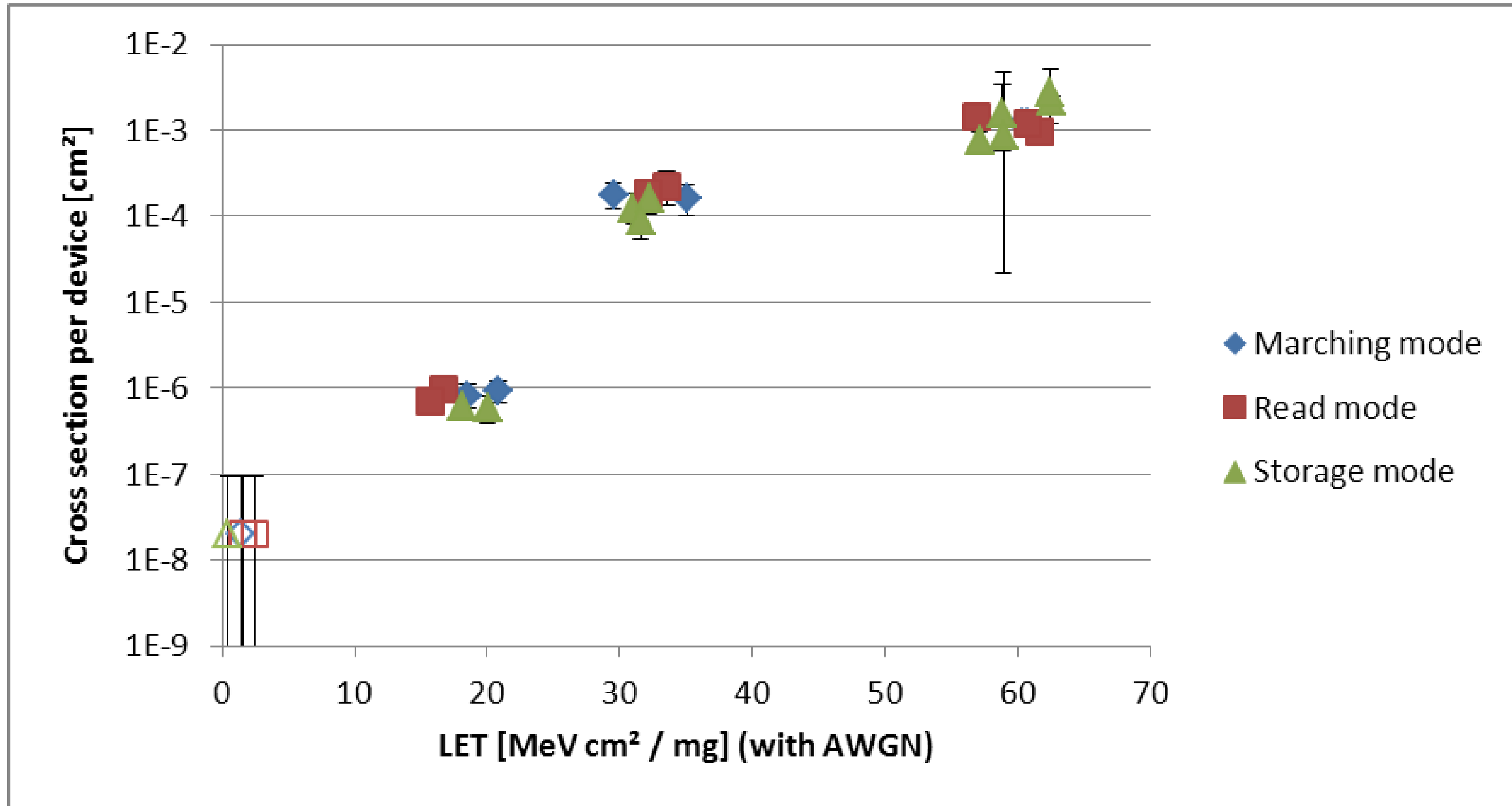
- Red lines: latch-up switch triggered
- Current increases in steps
- Current sometimes returns by itself
- No connection between data errors and current increase

MRAM SEE – Latch-up (1 Mbit)



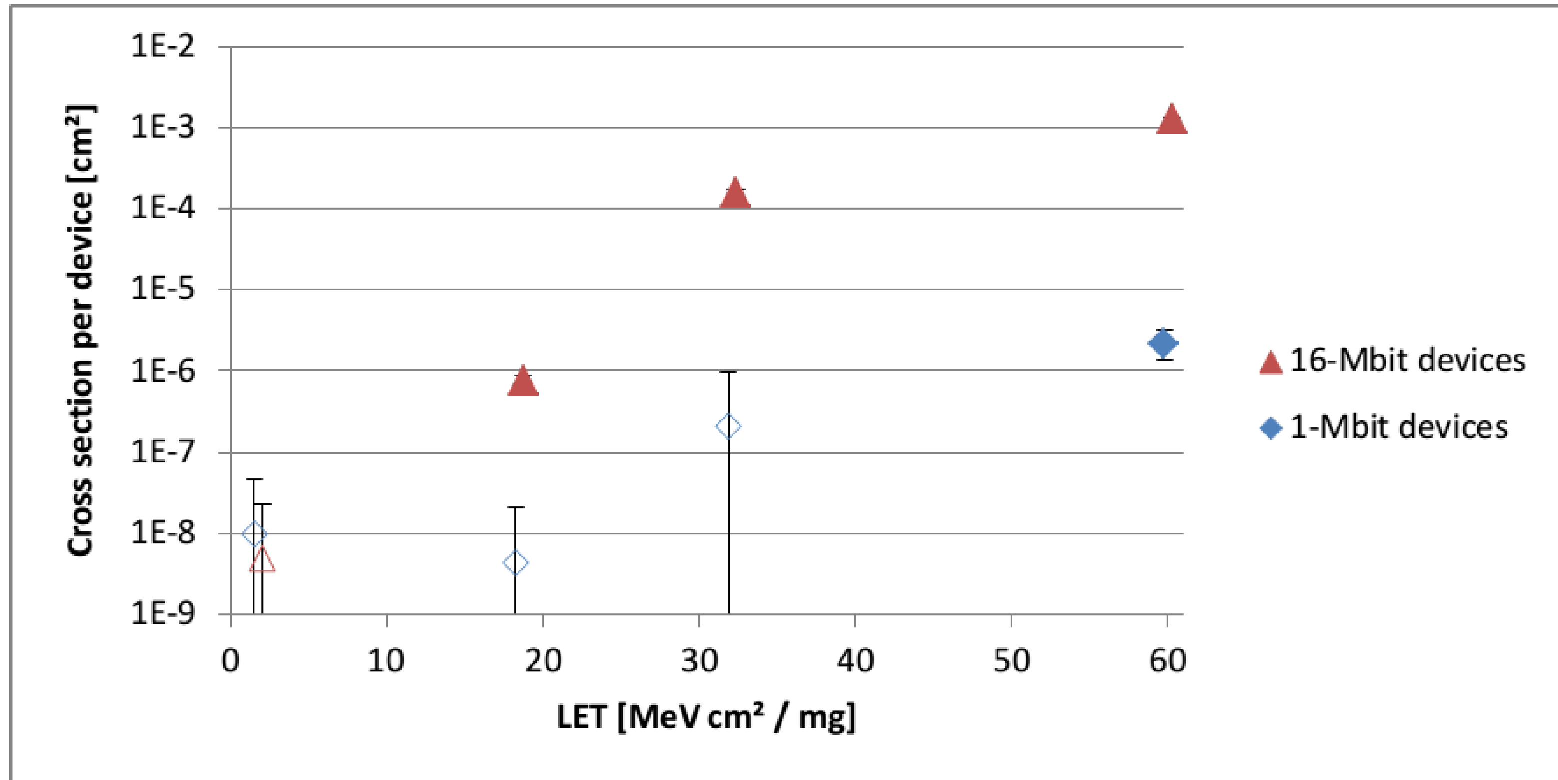
- Only at highest LET (xenon)
- Only in read and marching mode

MRAM SEE – Latch-up (16 Mbit)



- In all modes
- Not at lowest LET (nitrogen)

MRAM SEE – Latch-up (comparison)

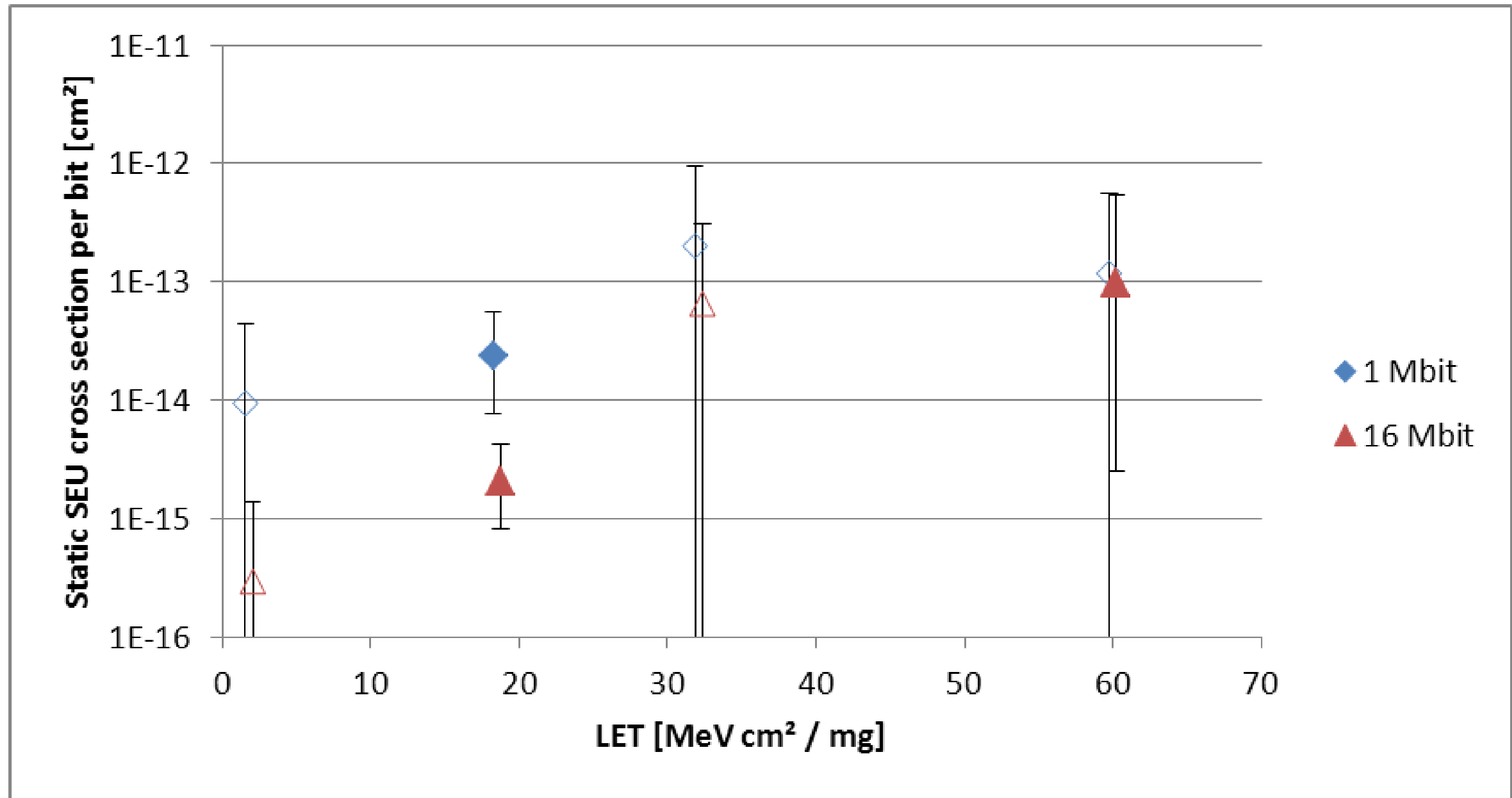


- All modes

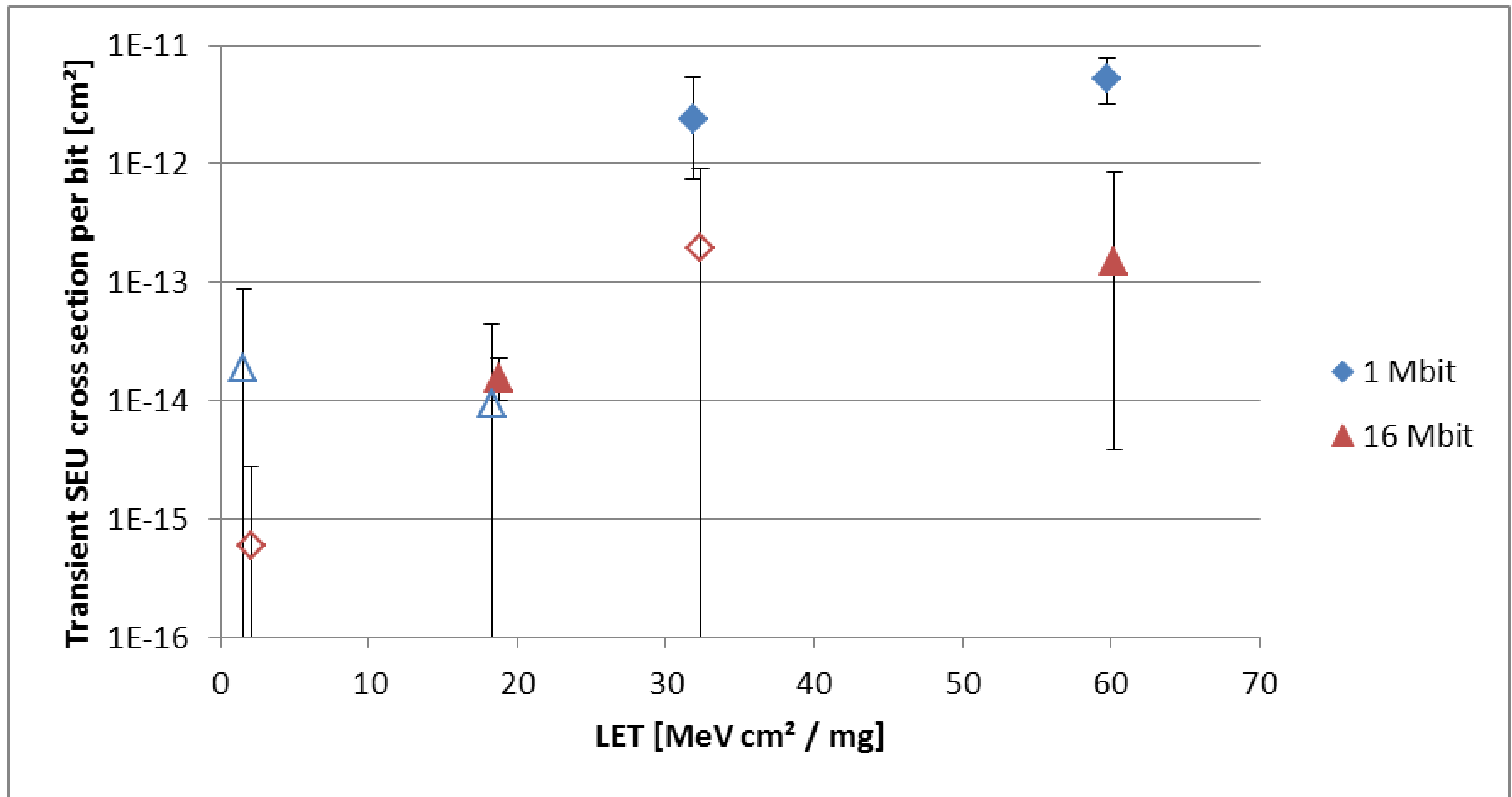
MRAM SEE – Data errors

- SEUs
  - Static and transient
  - Mostly MBUs (multiple errors in one word)
- No stuck bits
- SEFIs
  - Transient only (e.g. address decoder hit)
- No flux dependence
- No data error analysis performed for marching mode due to latch-up

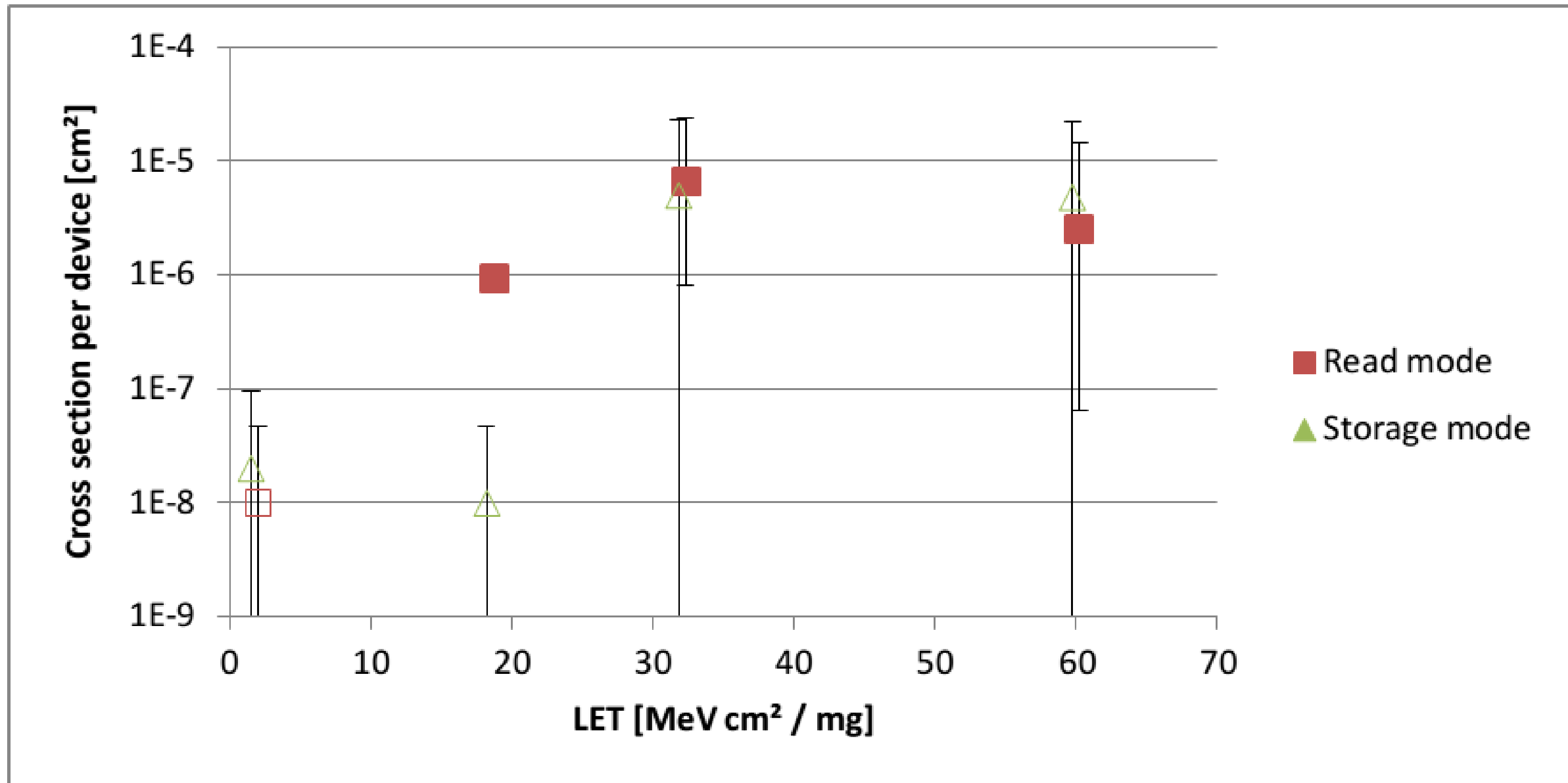
MRAM SEE – Static SEUs in Read Mode



MRAM SEE – Transient SEUs in Read Mode



MRAM SEE – SEFIs (16 Mbit)



- 1-Mbit devices: no useful data, flux too high

MRAM SEE – SEFI patterns

- Often length 256 and start at multiple of 256
- Often multiple SEFIs with related start address
  - E. g., 0x**07**0000, 0x**0a**0000, 0x**17**0000, 0x**a7**0000
- Polarity: sometimes mixed, sometimes all-down

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Test procedures and test results

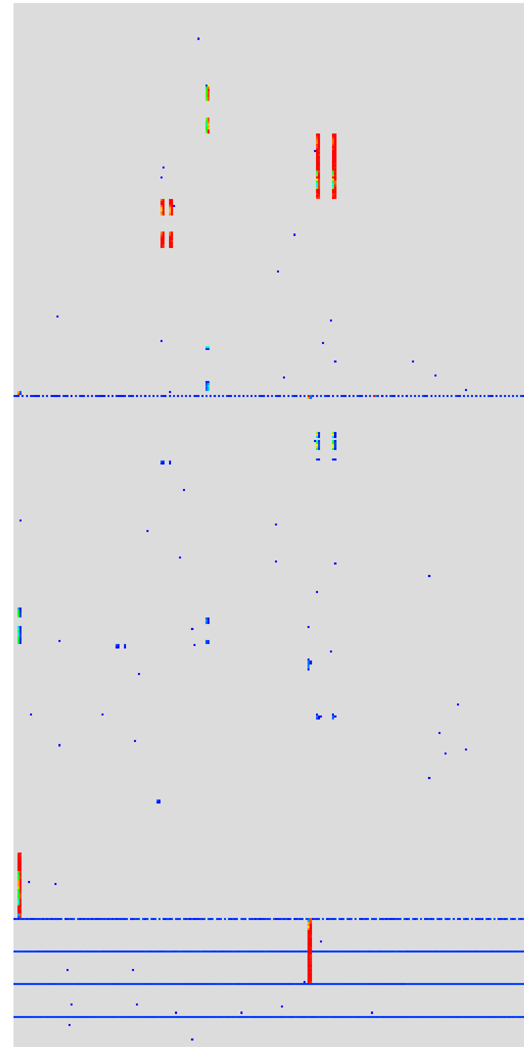
DDR3 heavy-ion SEE

DDR3 SEE – Test procedures

- Test conditions:
  - Test in vacuum without heating/cooling
  - 333 MHz
  - Standard voltage 1.5 V
  - Standard refresh rate 7.8 µs
  - Read mode (continuous read during irradiation)
  - Pseudo-random pattern
- Software conditioning
  - Tests with and without software conditioning
  - Rewrite mode registers, DLL reset, long ZQ calibration

DDR3 SEE – Error classification

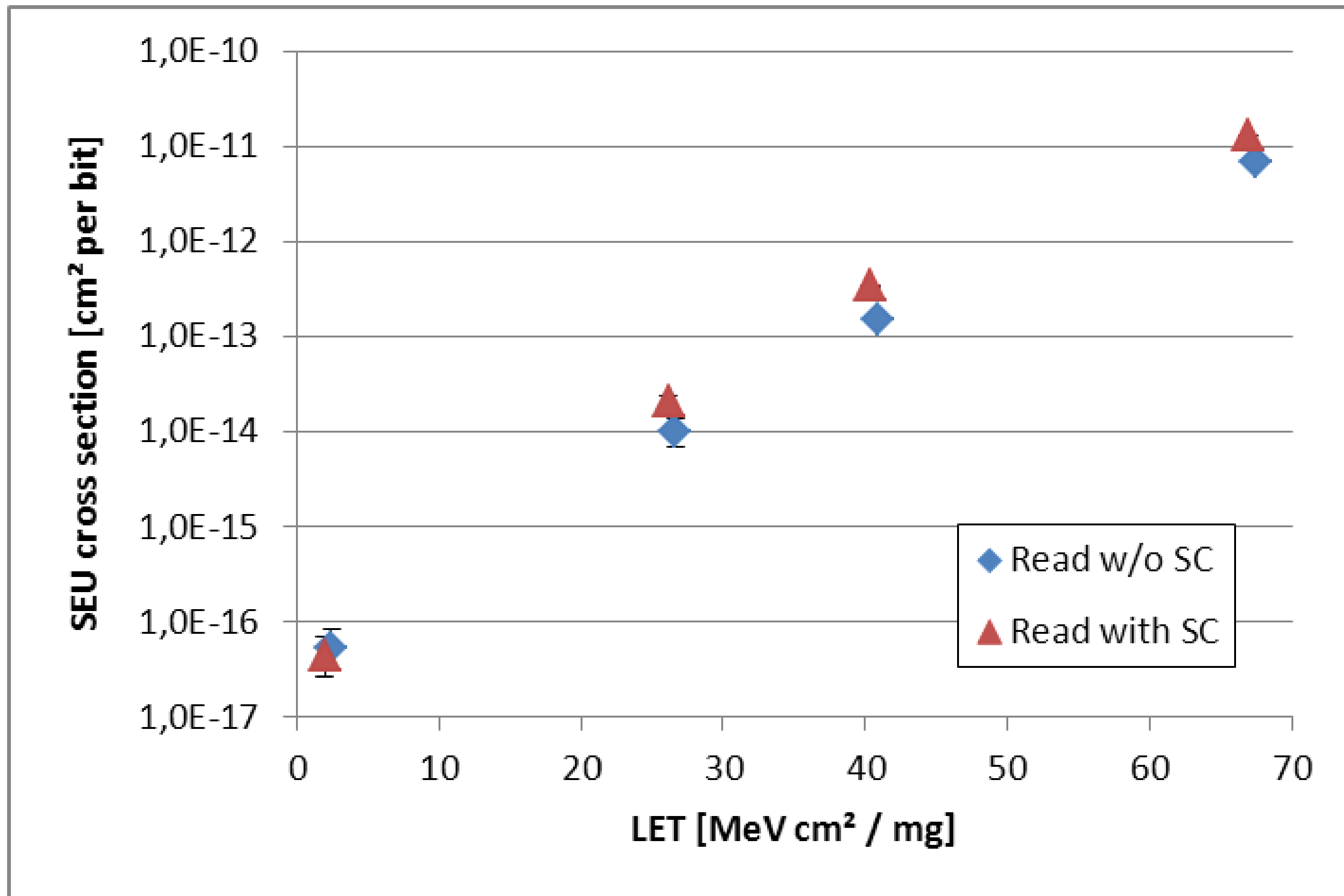
- SEU (SBU or MBU)
- Stuck bit
- SEFI
  - Row SEFI
  - Column SEFI
  - Device SEFI



DDR3 SEE – Results

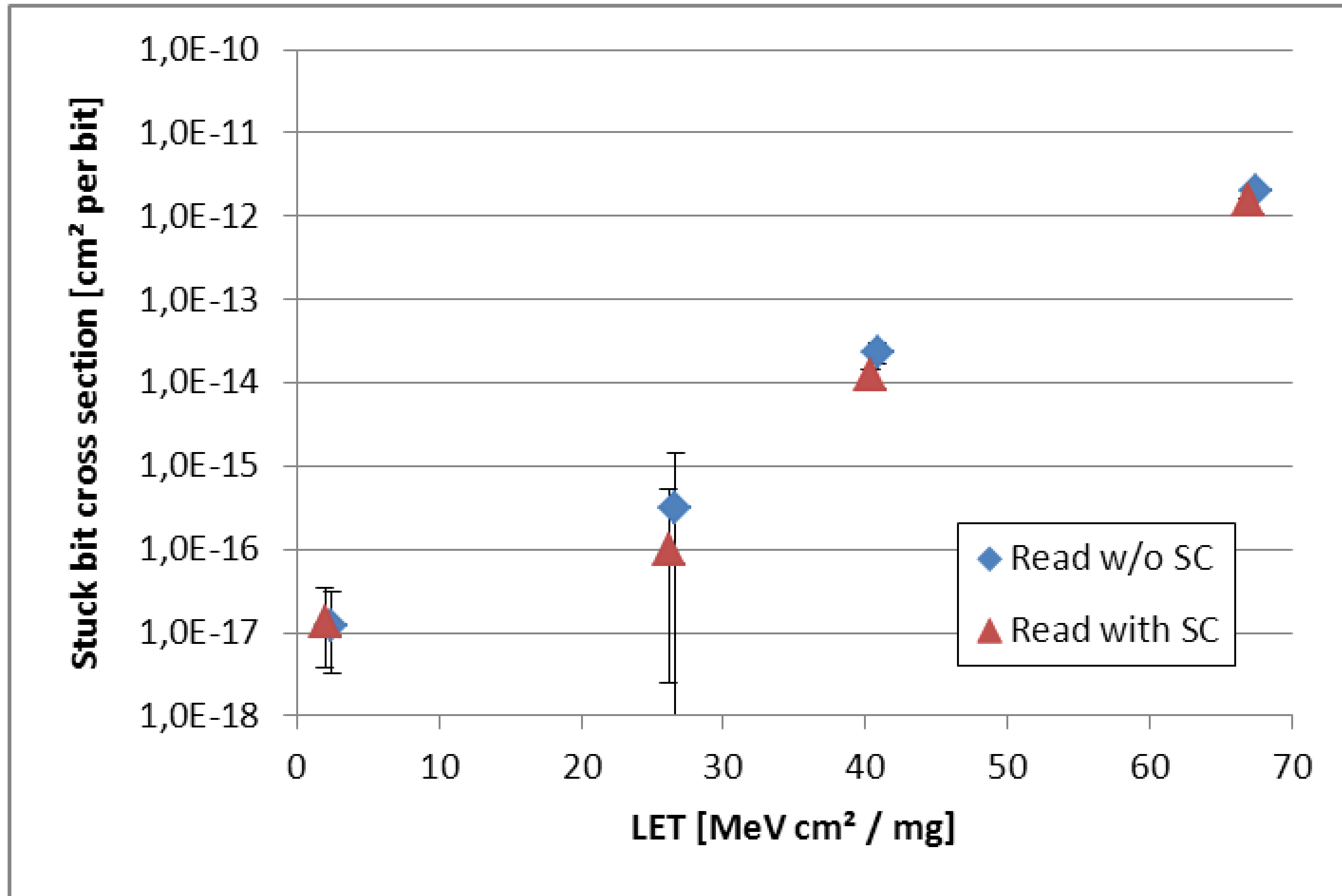
- No latch-up
- No MBUs
- Low threshold LET for SEUs, stuck bits, row SEFIs, column SEFIs, and device SEFIs
- Cross sections comparable to other 4-Gbit device types (Hynix, Micron, Samsung)
  - No column SEFIs for Hynix and Samsung

DDR3 SEE – SEUs



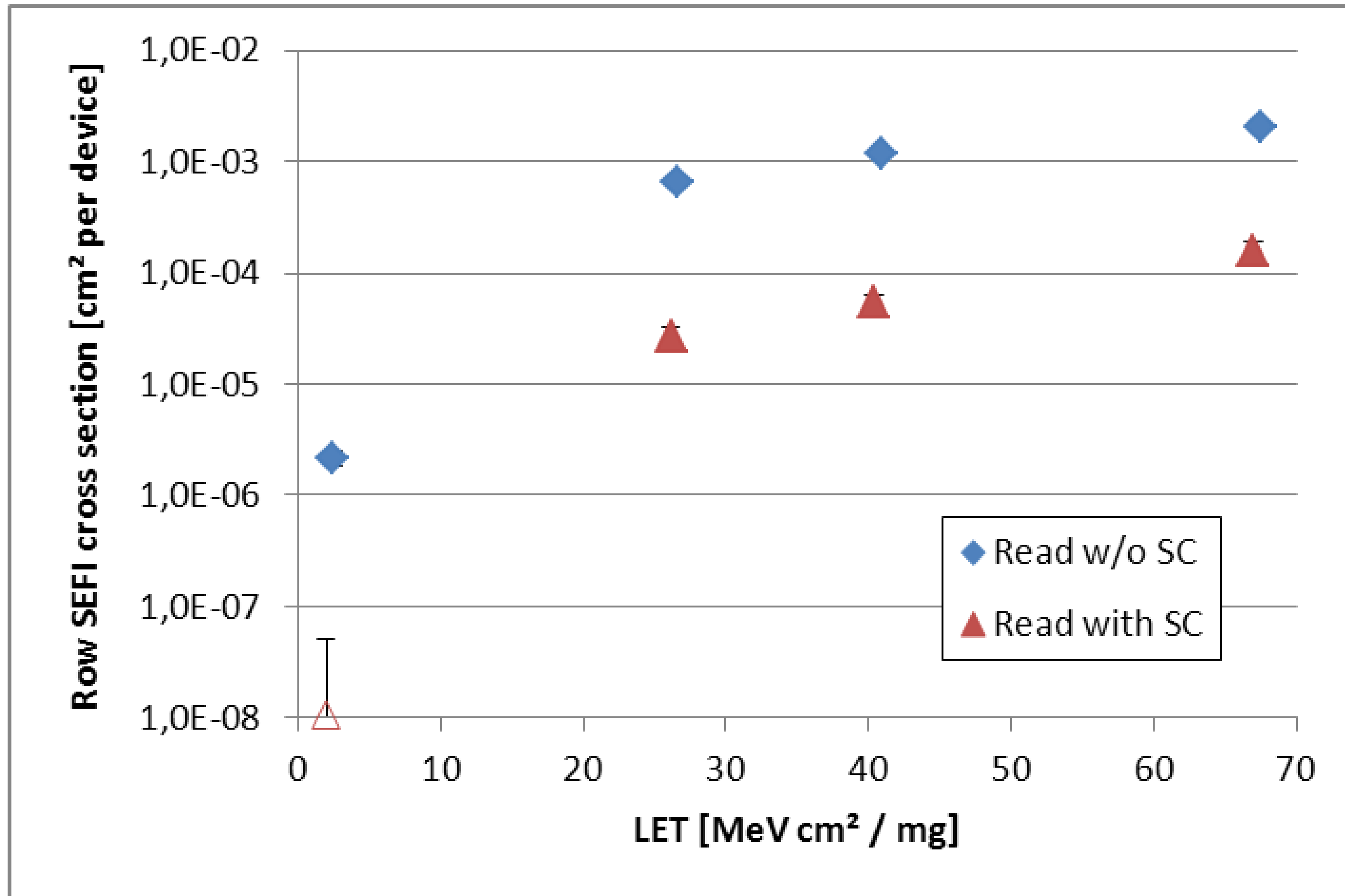
Software conditioning has no effect

DDR3 SEE – Stuck bits



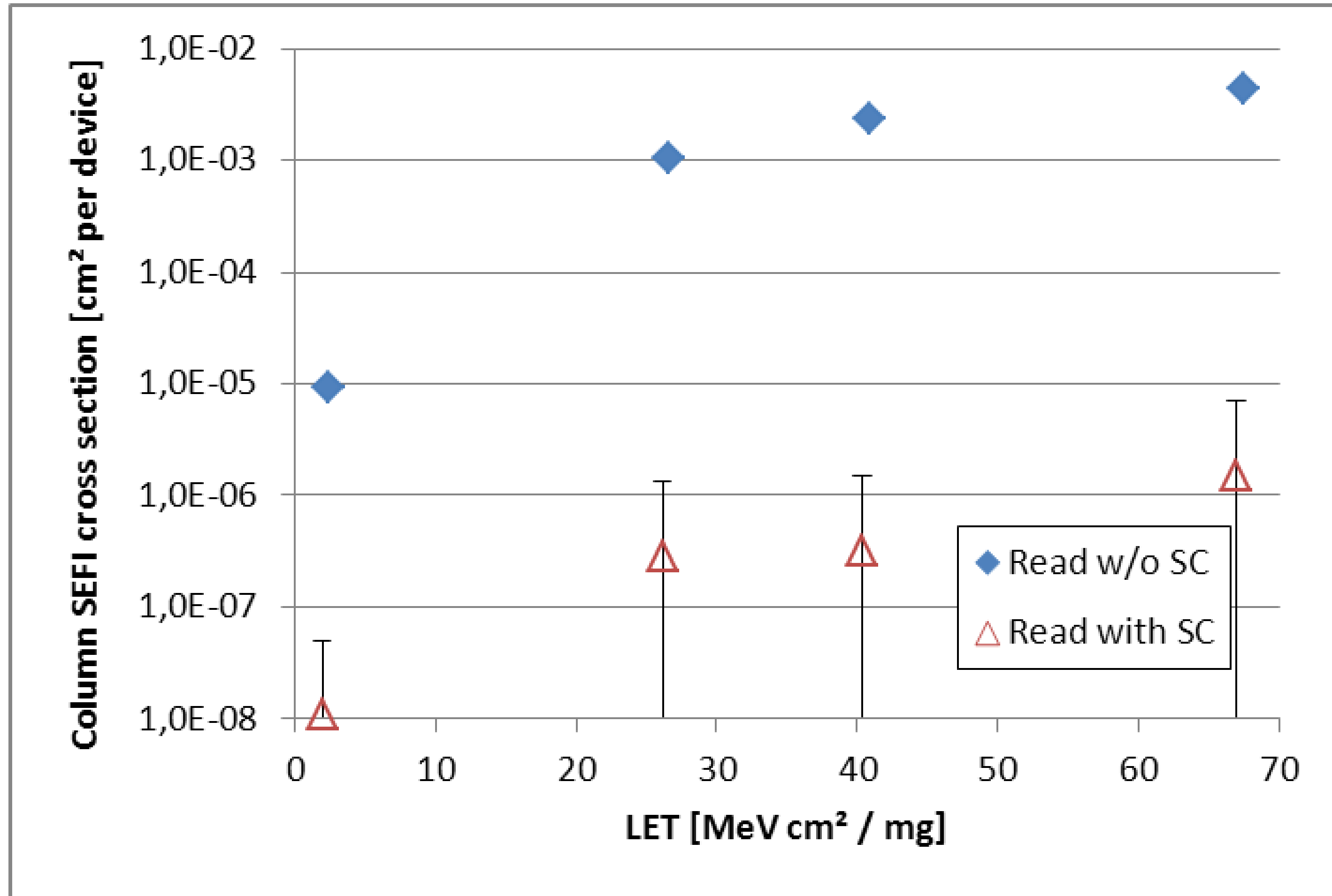
Software conditioning has no effect

DDR3 SEE – Row SEFIs



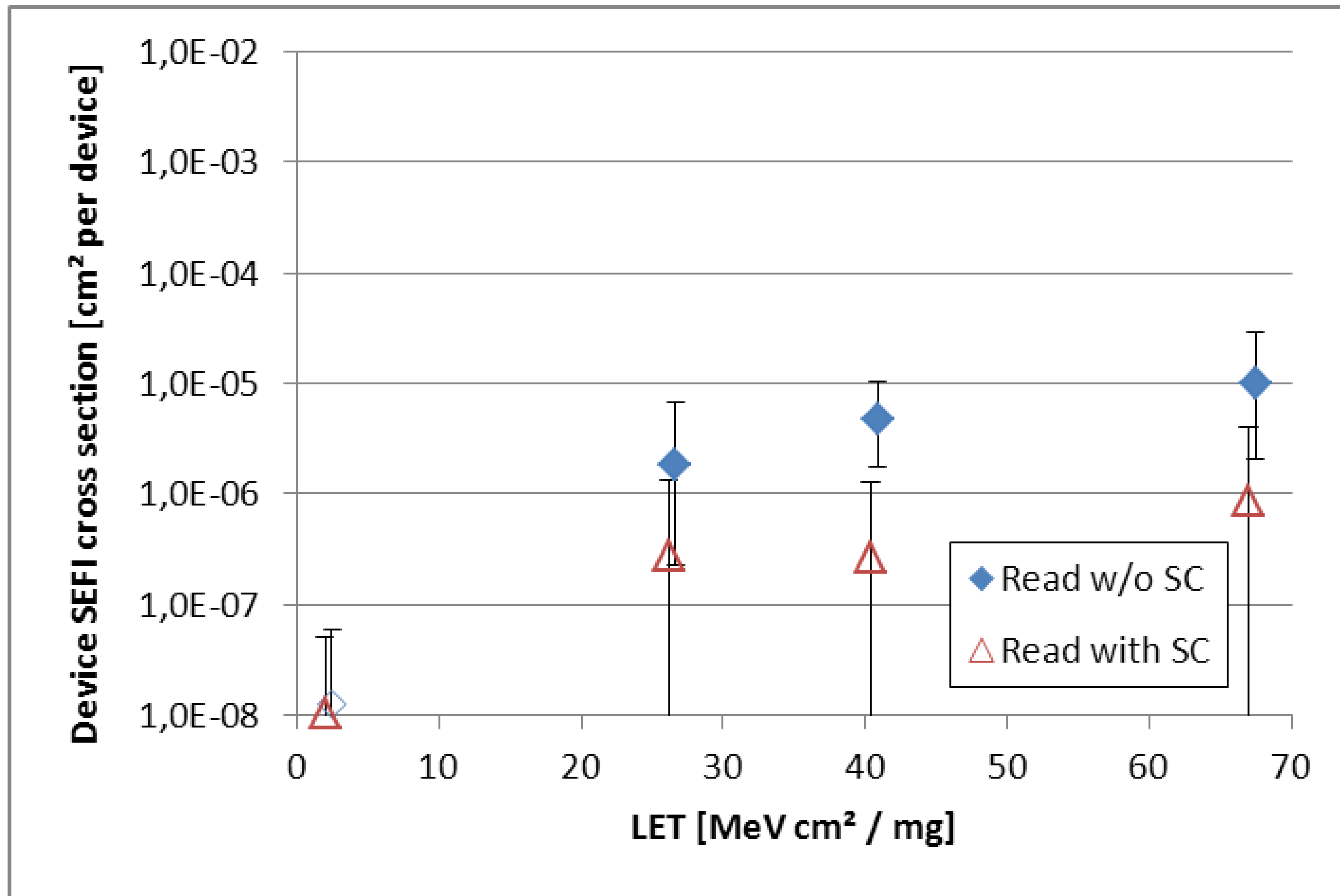
Software conditioning reduces row-SEFI sensitivity
Row SEFIs often appear in groups of 8

DDR3 SEE – Column SEFIs



Software conditioning eliminates column SEFIs
Column SEFIs almost always appear in groups of 8

DDR3 SEE – Device SEFIs



Software conditioning eliminates device SEFIs (but note error bars)

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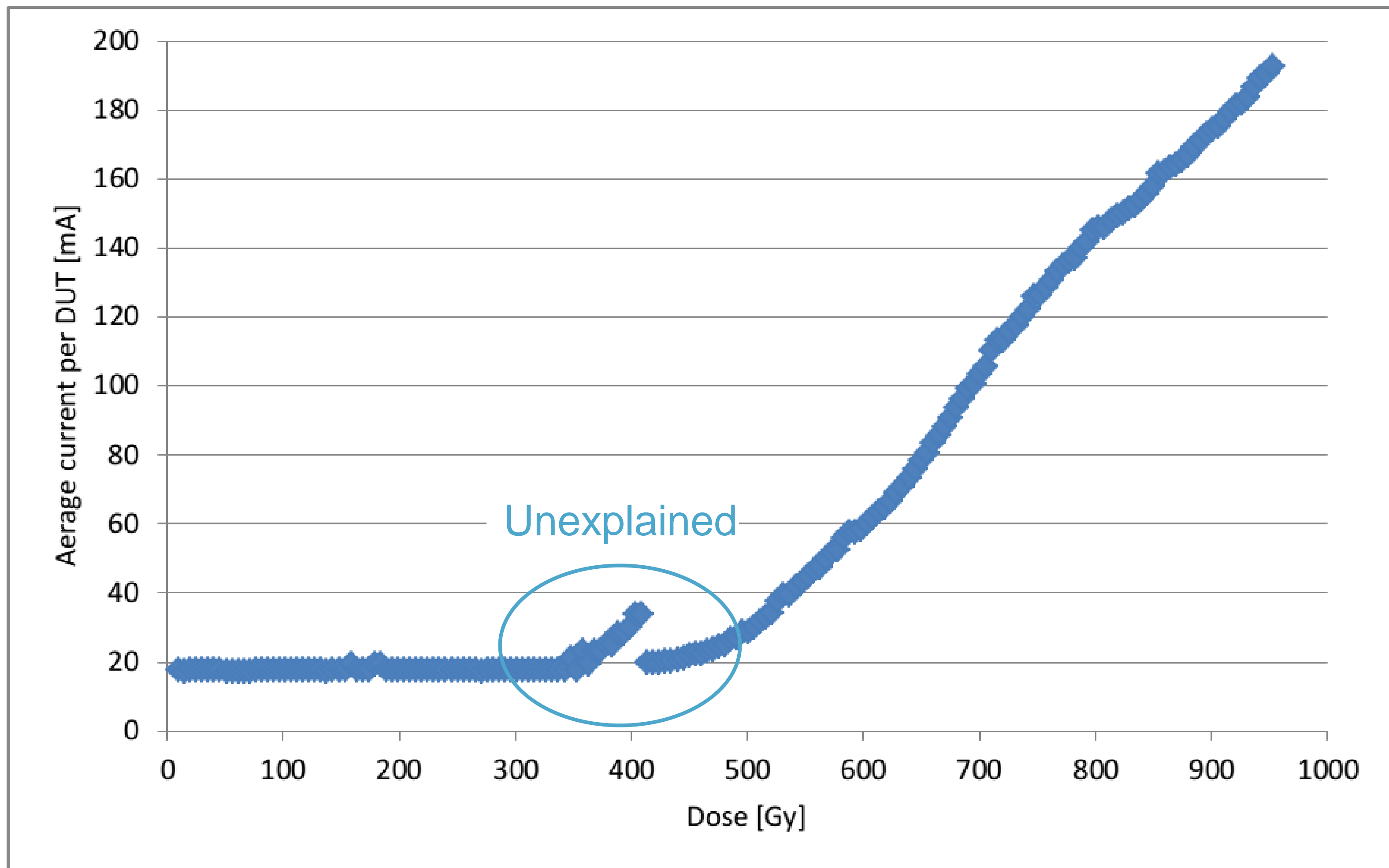
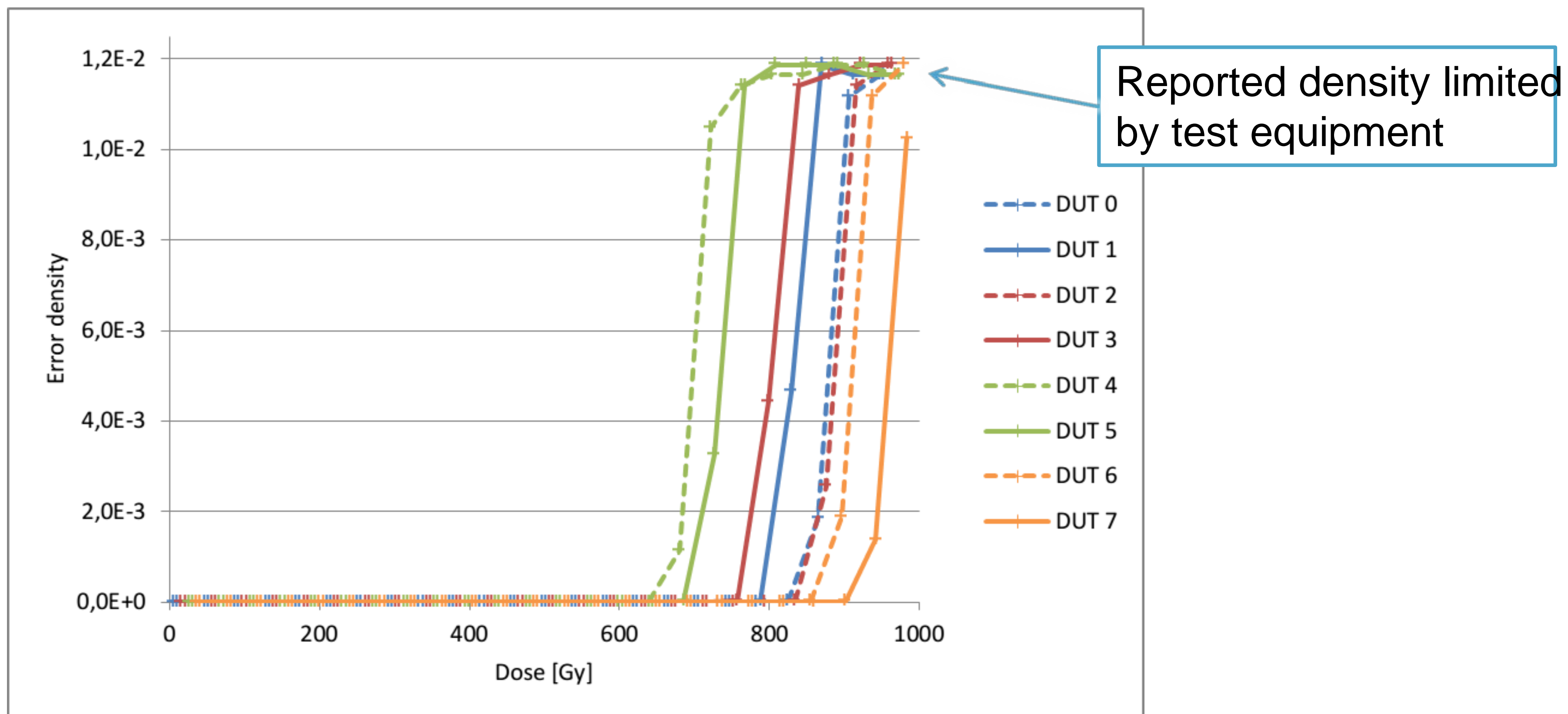
Test procedures and test results

DDR3 in-situ TID

DDR3 TID – Current



DDR3 TID – Data errors



Pseudo-random pattern
Round-robin write/read in 15-minute intervals
333 MHz
Standard refresh interval 7.8 µs

Conclusions

- MRAM:
  - Current increase, latch-up
  - SEUs, SEFIs
- DDR3:
  - TID:
    - ≈ 400 Gy (40 krad), Hynix: > 4 kGy (400 krad)
    - Severe current increase
  - SEE:
    - Comparable with Hynix, Samsung
    - No latch-up, but device SEFIs