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Development of a microcontroller Soft-Core PicoSkyFT

TEC-ED & TEC-SW FPD

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Outline

- PicoSkyFT history
- Architecture
- PicoSkyFT Ecosystem
- PicoSkyFT Validation project
- PicoSkyFT Radiation characterization project
- Use cases
- Next steps

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PicoSkyFT history

- 2010 ESA ESMO mission - responsible for OBDH subsystem
  - Generic CAN Node implementation
    - lack of state-of-the art small processors for space
- 2012: ESMO mission has been concluded after successful PDR
- 2012: PicoSkyFT development initiative took place
- 2014: 6th evolution of PicoSkyFT and SDK (TRL 3)

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PicoSkyFT history

- 2015: First introduction of PicoSkyFT processor core to ESA (TEC-ED)
- 2016: ESA contract awarded for PicoSkyFT verification and validation
  - contract successfully closed in 06/2017 (TRL 4)
- 2017: ESA contract awarded for PicoSkyFT radiation testing characterization under high energy proton beam
  - contract successfully closed in 12/2017 (TRL 5)

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Architecture

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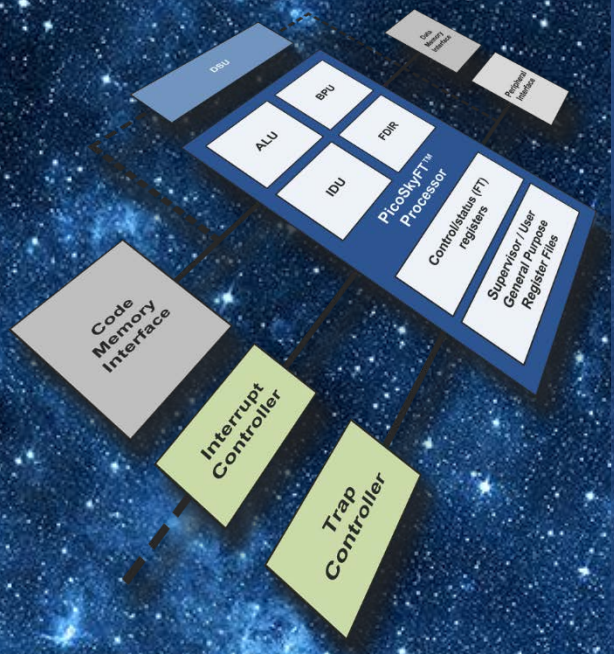
PicoSkyFT soft-core processor

Small footprint, radiation hardened by design processor core



- **Small footprint**, soft-core and **fault tolerant** processor core.
- IP Core building block for true SoC architecture and **EU technology independence**

Architecture

- **RISC** 8/16-bit Harvard architecture
  - Proprietary **PicoSky ISA**
  - Operation in two modes (supervisor – privilege mode / user operation mode)
  - Operation modes
    - Supervisor mode (traps handlers)
    - User mode (reduced instruction set, interrupts handlers)
    - Sleep, Error, Debug mode
- **Single stage pipeline** architecture
  - Highly deterministic operation
  - Hard real time interrupt response capabilities
- **140 instructions** (**97.5%** of 16-bit combinations used) provides extremely **high code density**
  - Low memory footprint of the application code
  - High integration capabilities (minimal number of external components)
  - Hardware accelerated **multiplication instructions**

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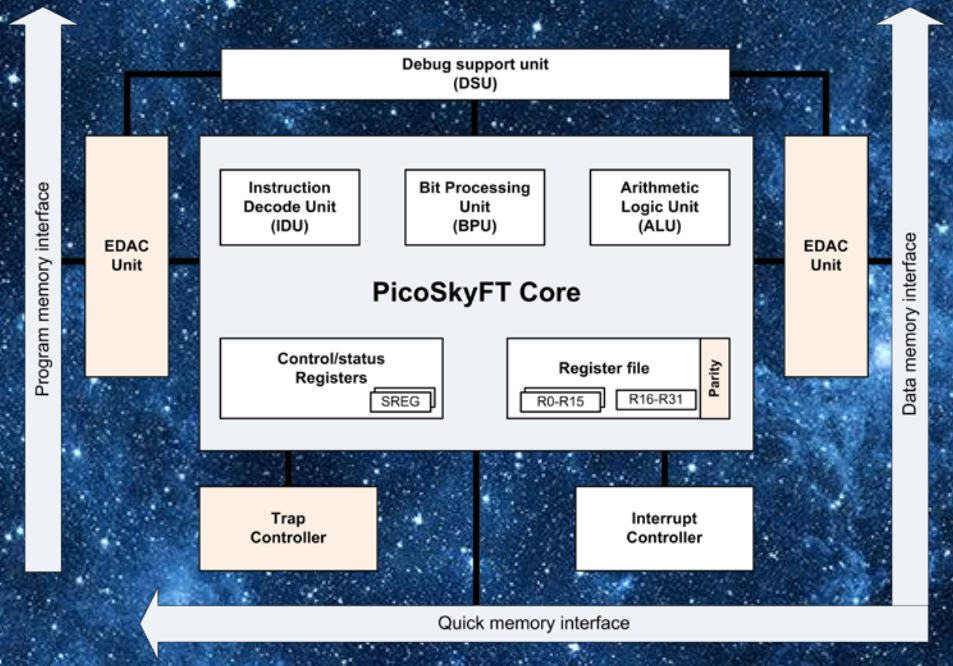
PicoSkyFT soft-core processor

Small footprint, radiation hardened by design processor core



- Configurable **program memory** models **up to 8 MB**
  - Compact (8 kB), Small (64 kB), Medium (128 kB), Large (8 MB)
- Configurable **data memory** models **up to 16 MB**
  - Normal (64kB) or Extended (16MB)
- Register file with **32** general purpose registers
  - R01-R16 are duplicated for Supervisor and User mode, respectively.
- Configurable Interrupt Controller
  - Customizable number of interrupt vectors
  - Prioritized interrupt vectors
- Processor benchmark
  - Mostly single cycle instructions reaching **1 MIPS/MHz**
  - **0.59 CoreMark / MHz** (–O2)

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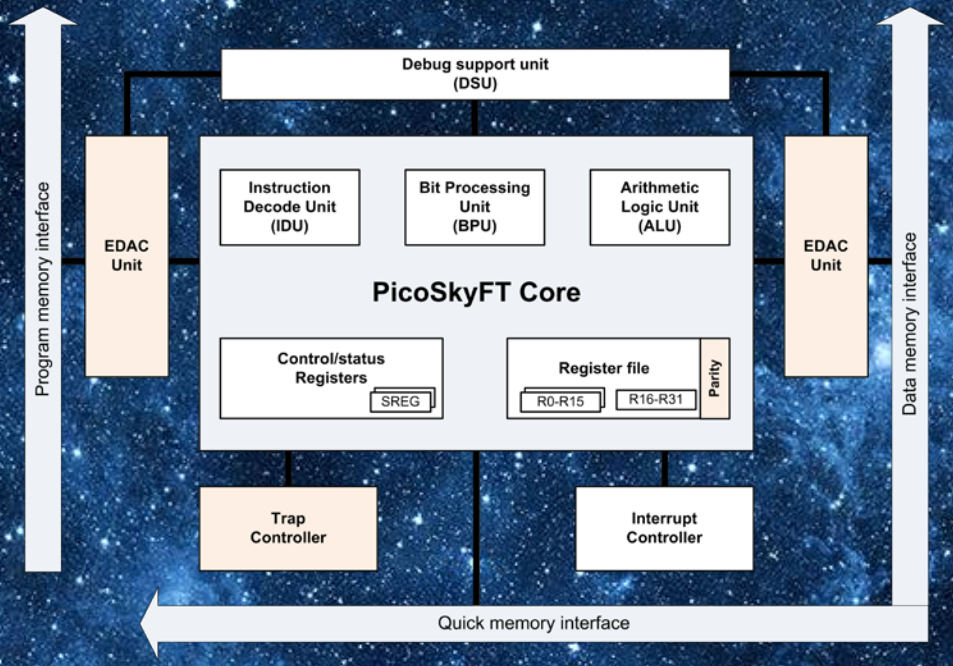
PicoSkyFT soft-core processor

Small footprint, radiation hardened by design processor core



- **Fault tolerant design**
  - All memories EDAC protected by enhanced Hamming
  - Multiple SEC-DED protection
  - **SEC** events **corrected on the fly** with **Zero wait states**
  - Self diagnose EDAC function
  - Register file with dual parity protected
  - Protecting invalid accesses between modes.
  - User mode have a restricted instruction set of instructions.
  - Upon detected faults trap handlers are invoked in single cycle
  - Customisable FDIR policy for each trap respectively

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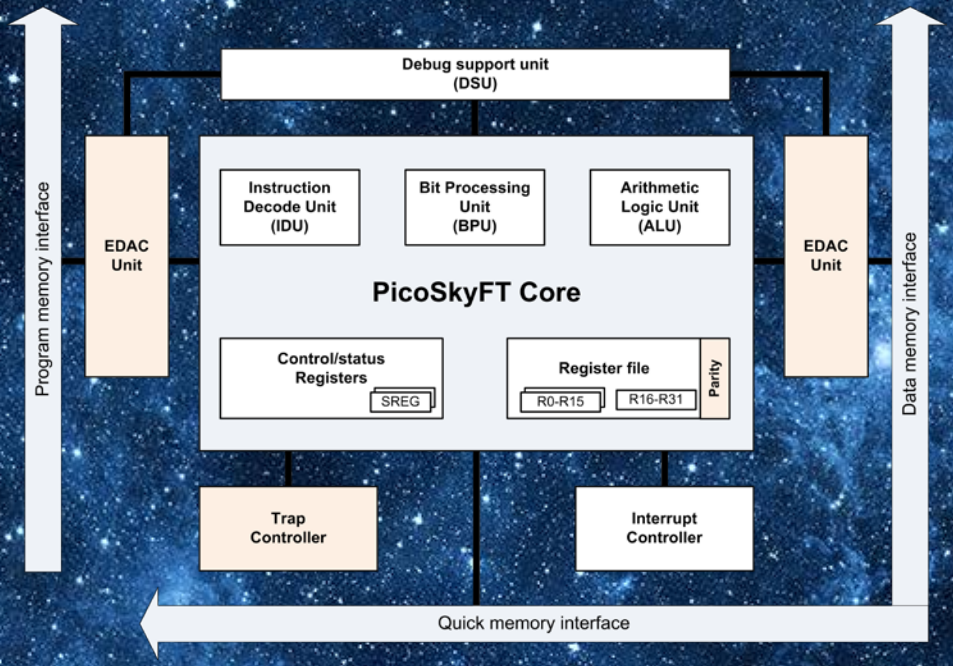
PicoSkyFT soft-core processor

Small footprint, radiation hardened by design processor core



- **Radiation hardened by design approach**
  - Spatial redundancy (TMR) on register level
    - **Full TMR**, or
    - **Partial TMR** for best performance
  - Optional temporal redundancy for improved SET filtering.
  - Proprietary TMRcreator™Tool for ease applying of redundancy on netlist level.
  - Verification of the RHBD techniques by proprietary SEES™Tool
- Build-in **Debug Support Unit** over high-speed **PicoSkyLINK** debugger.
  - DSU physically disabled when PicoSkyLINK detached.

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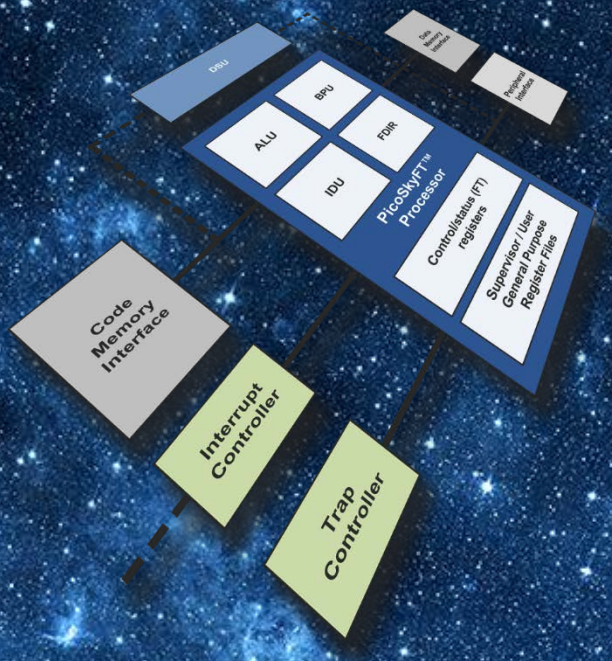
PicoSkyFT soft-core processor

Small footprint, radiation hardened by design processor core



- **PicoSkyFT** makes development **less complex**, thus shortening the development time and verification cycles and ultimately providing **faster time to market**.
- Targeting applications requiring **scaled performance**, reduced peripherals functionality, **hard real-time performance**, and **high reliability requirements**.
- Using PicoSkyFT in application would benefit in terms of **ease of use**, **application performance**, static power consumption and overall production costs.
- PicoSkyFT enables highly customized designs thanks to its availability as IP Core.

Target applications

- That require high reliability, scaled or hard real-time performance and reduced peripherals functionality.
- Replacement for complex FPGA FSMs.
- **Distributed intelligence** as smart sensors/actuators, RTU, payload TM/TC interface, etc.

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PicoSkyFT Ecosystem

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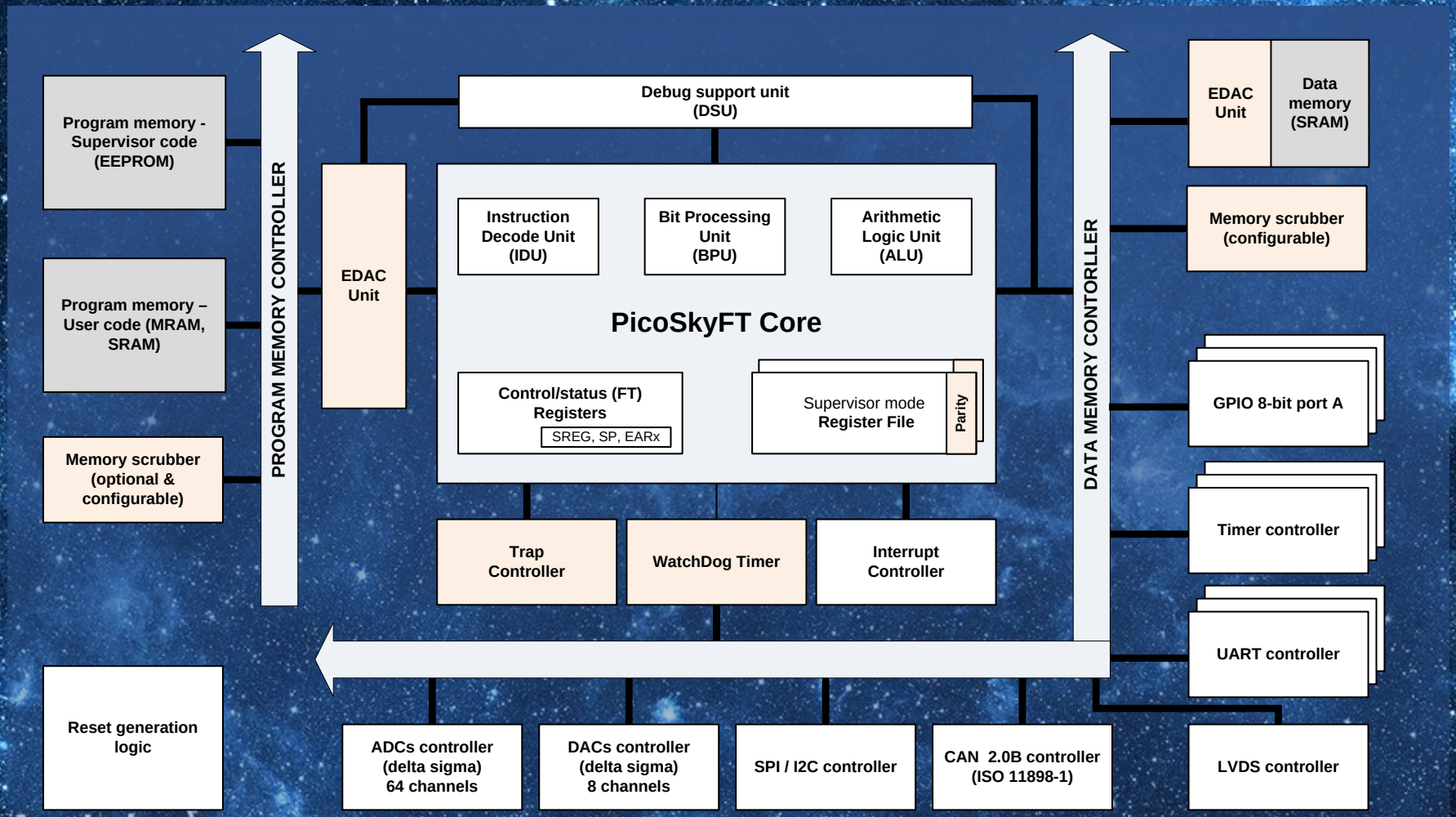
PicoSkyFT system-on-a-chip



*SkyLabs **PicoSkyFT SoC Basic implementation – EXAMPLE!***
(all cores available)

PicoSkyFT Ecosystem

Development environment

PicoSkySIM-Interface
Extenstion board

PicoSkyWARE
PicoSkyWARE is a collection of software development tools to provide the effective development of PicoSkyFT code solutions. PicoSkyWARE is a standalone package compliant with Windows and Linux operating systems.

PicoSkyTEST
PicoSkyTEST is an enhanced test suite platform enabling highly efficient verification of SoC RTL design at each step of the development. The test suite thoroughly examines processor functionality with regrestion testing at RTL simulation level, RTL implementation on FPGA or even in PicoSkySIM.

PicoSkySIM
PicoSkySIM is a cycle exact software based PicoSkyFT processor simulator. PicoSkySIM fastens the development cycle and in addition increases the system's testability as tests can be performed already at the early design stages.

PicoSkyFT processor

ecosystem

PicoSkyLINK *– programmer and debbuger*

PicoSkySIM-Interface
PicoSkySIM Interface board is an extension of the PicoSkySIM providing a bridge between the simulated environment and the real world. Simulated and custom developed peripheral units can be easily interfaced to real physical interfaces.

PicoSkyLINK
*The **PicoSkyLINK** is an **debugger and programmer** for the PicoSkyFT processor. The high speed synchronous debugging interface enabling astonishingly fast programming times and incredibly responsible debugging.*

SEES™
*SEES ™(**Single event effect simulation**) is a comprehensive tool for SEE simulation on the FPGA gate-level (SET, SEU). Technology independent simulator, enables low cost design analysis against soft-errors.*

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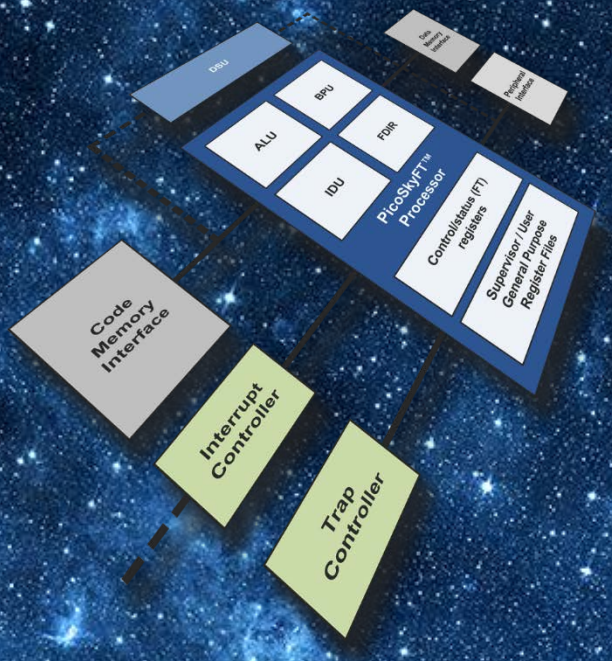
PicoSkyFT soft-core processor

Software development support



Software support

- **FreeRTOS** real-time operating system
- ***C Standard library***
- ***PicoSky Peripherals Drivers*** *library (SPI, TWI, CAN, UART, GPIO, Timers, LVDS, DACs, ADCs...)*
- *Comprehensive* ***code examples*** *for quick hands on experiences*
- *Reference code for errors mitigation in supervisor mode*

Communication stacks

- ***CANopen stack implementation*** *(according to ECSS-E-ST-50-15C)*
- ***CAN-TS*** *(CAN-TinyStack) simple reliable CAN stack*
- ***Light weight TCP/IP*** *Stack*

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PicoSkyFT Ecosystem

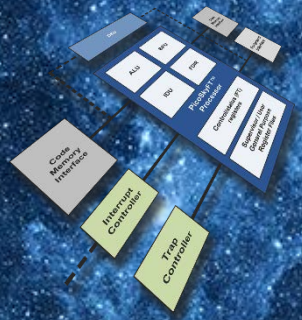
Versatile development boards & satellite subsystems

DEV-BOARD-M2GL050
- MIL-STD-1553B
- SpaceWire
- CAN
- SerDes,...

DEV-BOARD-A3PE3000
- SpaceWire
- MIL-STD-1553B
- CAN
- RS422/232
- SerDes,...

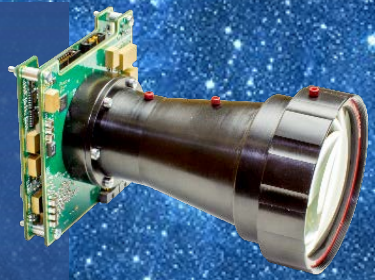
SKY-PICOSKY-EVAL [SKY9213]
- CAN, PIO, USB
- ADCs, DACs
- SPI / I2C

PicoSkyFT processor



ecosystem

MMSI
- SWIR spectral range
- Multispectral
- 20 spectral bands
- 70m GSD @ 350km



NANOobc
- Redundant CAN
- High speed LVDS
- Redundant mass storage
- LCL on-board
- Rich local TM

cpciSDR 1x1 [SKY-9202]
- 3U CPCI® SDR Card
- Xilinx Artix®-7 FPGA (RF)
- RF 1 × 1 transceiver
- Dual CAN, SpW

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PicoSkyFT Validation project

- ESA Project title: Validation of Space Rated Microcontroller Softcore
- Contract number: 4000112637/14/NL/NDe (CCN1)
- Project status: Successfully closed
- KO: 1.6.2016
- Project finished: 1.6.2017

- Objective:

  Prepare a comprehensive regression testing environment to validate and confirm proper operation of the processor itself and companion development tools, as toolchain, debugging software and PicoSkyLINK programmer.

  Perform an assessment of RHBD mitigation techniques available with PicoSkyFT soft-core processor.

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PicoSkyFT Validation project

Background

- Project divided into two sections, with the objectives:
  - Section 1:
    Despite of already high maturity level PicoSkyFT required addition software supporting environment to validate processor in fully systematic manner.
  - Section 2:
    PicoSkyFT supports few RHBD mitigation techniques, however, their assessment should be performed.

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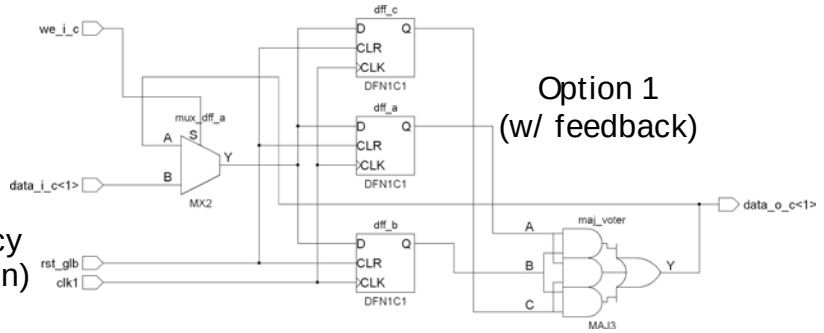
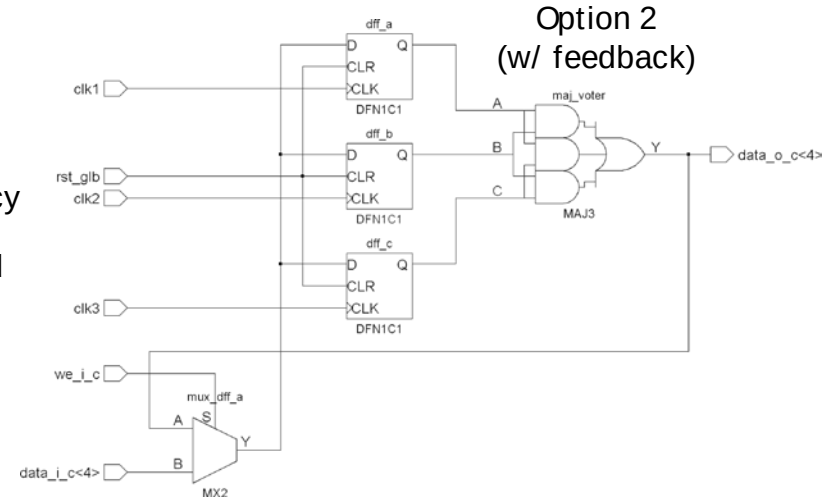
PicoSkyFT Validation project

Assesment RHBD mitigation techniques

- PicoSkyFT design enables hardening against SEU and SET induced events to decrease cross section and improve its fault tolerance.
- PicoSkyFT Local TMR protection assessment
  - Option 1: Spatial triplicated modular redundancy:
    - Local triple modular redundancy on register level (SEU mitigation)



  - Option 2: Spatial triplicated modular redundancy combined with triple temporal redundancy
    - Local triple modular redundancy on register level with tripled temporal redundancy (SEU and SET mitigation)



PicoSkyFT Validation project

Assesment of RHBD mitigation techniques

- Focused on Option 1 mitigation techniques:
  - Full Local TMR – Type 2, and
  - Partial Local TMR – Type 3 (new)
- Full Local TMR (**fTMR**): triplicates all registers
- Partial LTMR (**pTMR**) considers triplication of only crucial registers.
  - By defining protection principles it has been possible to systematically assessed, which registers shall be protected with pTMR (Type 2).
- PicoSkyFT Protection types investigated

Type #	Type description
Type 1	No TMR on flip-flops.
Type 2	Full LTMR – fTMR with refreshing.
Type 2a	Full LTMR – fTMR without refreshing.
Type 3	Partial LTMR – pTMR with refreshing.
Type 3a	Partial LTMR – pTMR without refreshing.

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PicoSkyFT Validation project

Assesment of RHBD mitigation techniques

- PicoSkyFT Protection types resources overhead in FPGA
  - Developed proprietary TMRcreator™Tool to apply spatial redundancy on netlist level.

Protection	type	SEQ count	COMB count	VersaTile cnt	% res utiliz.
Type 1	no TMR	1151	0	1151	0,00%
Type 2	pTMR w/ fb	2141	992	3131	172,37%
Type 3	TMR w/ fb	3453	2302	5755	400,00%
Type 2a	pTMR	2141	496	2636	129,28%
Type 3a	TMR	3453	1151	4604	300,00%

- PicoSkyFT Protection types testing results
  - Developed proprietary SEES ™Tool for SEU and SET injection into PicoSkyFT post layout RTL simulation.
  - SEES™Tool simulation constraints:
    - Only 1 SEU per injection period (injection time is randomized within injection period).
    - Injection period set to 1 us, i.e. one register upset per 20 processor‘s clock cycles.
    - Injection rate not normalized per resources usage (to mimic cross section – more resources – higher probability of SEU)
    - SET events have not been injected (due to 100x lower probability as SEU - HIREX).

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PicoSkyFT Validation project

Assesment of RHBD mitigation techniques

	Type 1	Type 2	Type 3	Type 2a	Type 3a	
Avg. SEU rate [upset / us]	0.78	1,00	0.96	1.01	0.97	
Total testing time [ms]	1.80	50,00	5.18	30.05	7.79	
Total upsets induced	1392	50000	4954	30295	7523	
Number of test runs	164	50	148	147	158	
SEES Tool results						
Expected failures but mitigated by sys. level protection	1 (w/o RFPE*)	0	148 (RF SEU)	16 (w/o RFPE*)	144	e.g. RF parity error, EDAC, IPI, fetch registers
Expected failures and cannot be handled by sys. level protection	163	0	0	131	14	e.g. opcode state machines, accumulated SEU,...
Unexpected failures	0	0	0	0	0	Unhandled faults

* RFPE Register file parity check enable

- SEES™Simulation confirms fTMR and pTMR with feedback (Type 2 and 3) provides the highest protection level for the PicoSkyFT processor.
- pTMR is very promising approach, due to relatively lower resources utilization comparing to fTMR, while upsets in unprotected registers are protected by system level mitigation techniques.
- SEES™Simulation revelad two registers that has been overlooked during systematic definition of the pTMR scheme.

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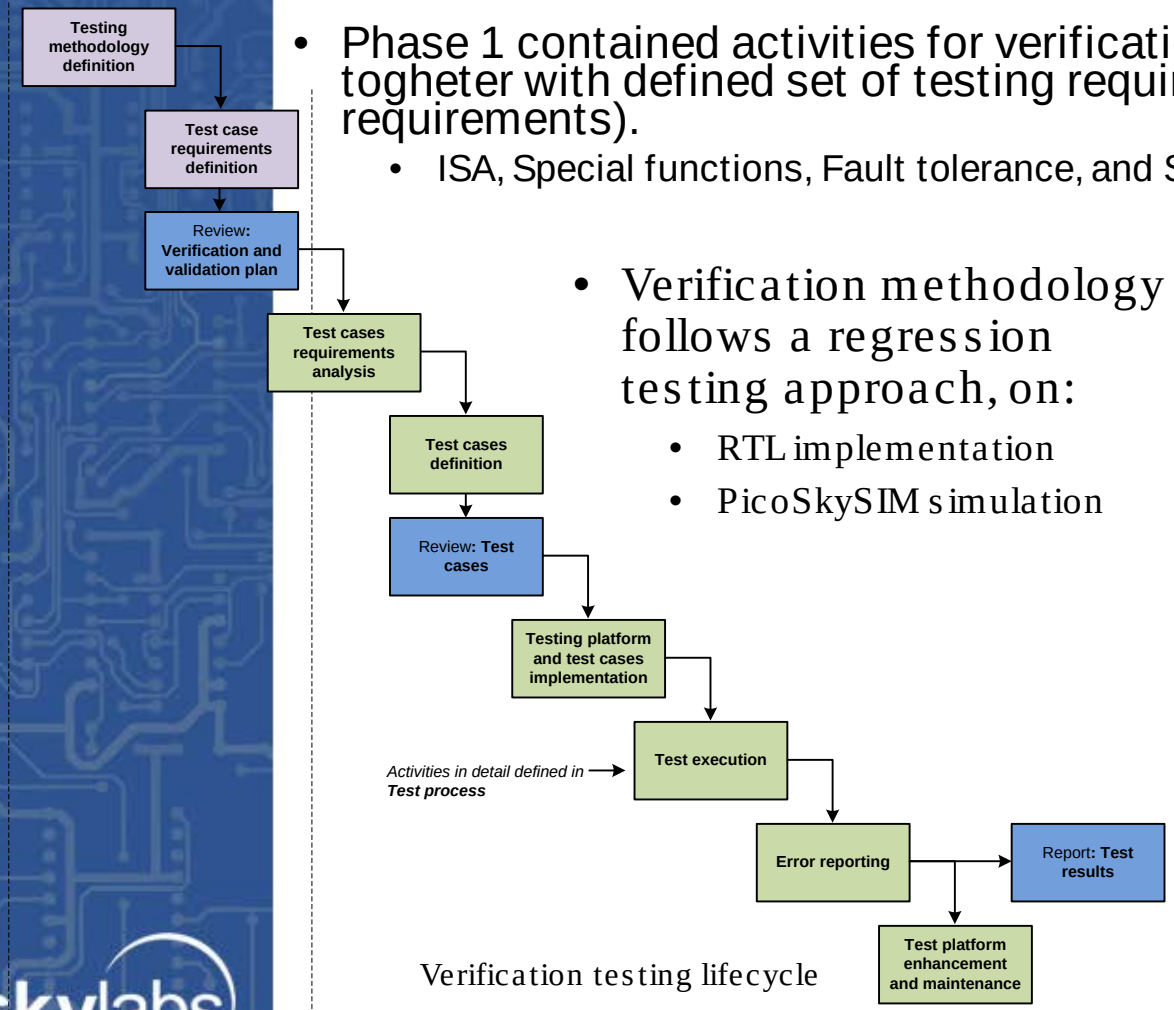
PicoSkyFT Validation project

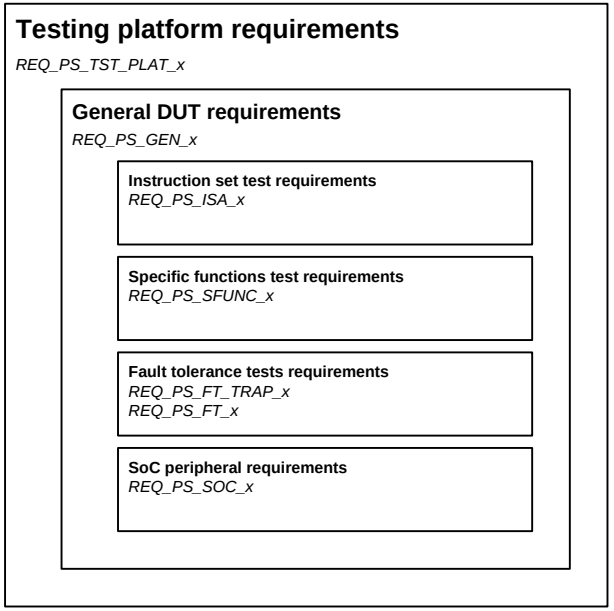
Validation testing platform

- Phase 1 contained activities for verification process definition togheter with defined set of testing requiremtns (98 testing requirements).
  - ISA, Special functions, Fault tolerance, and SoC peripherals test cases



Verification testing lifecycle

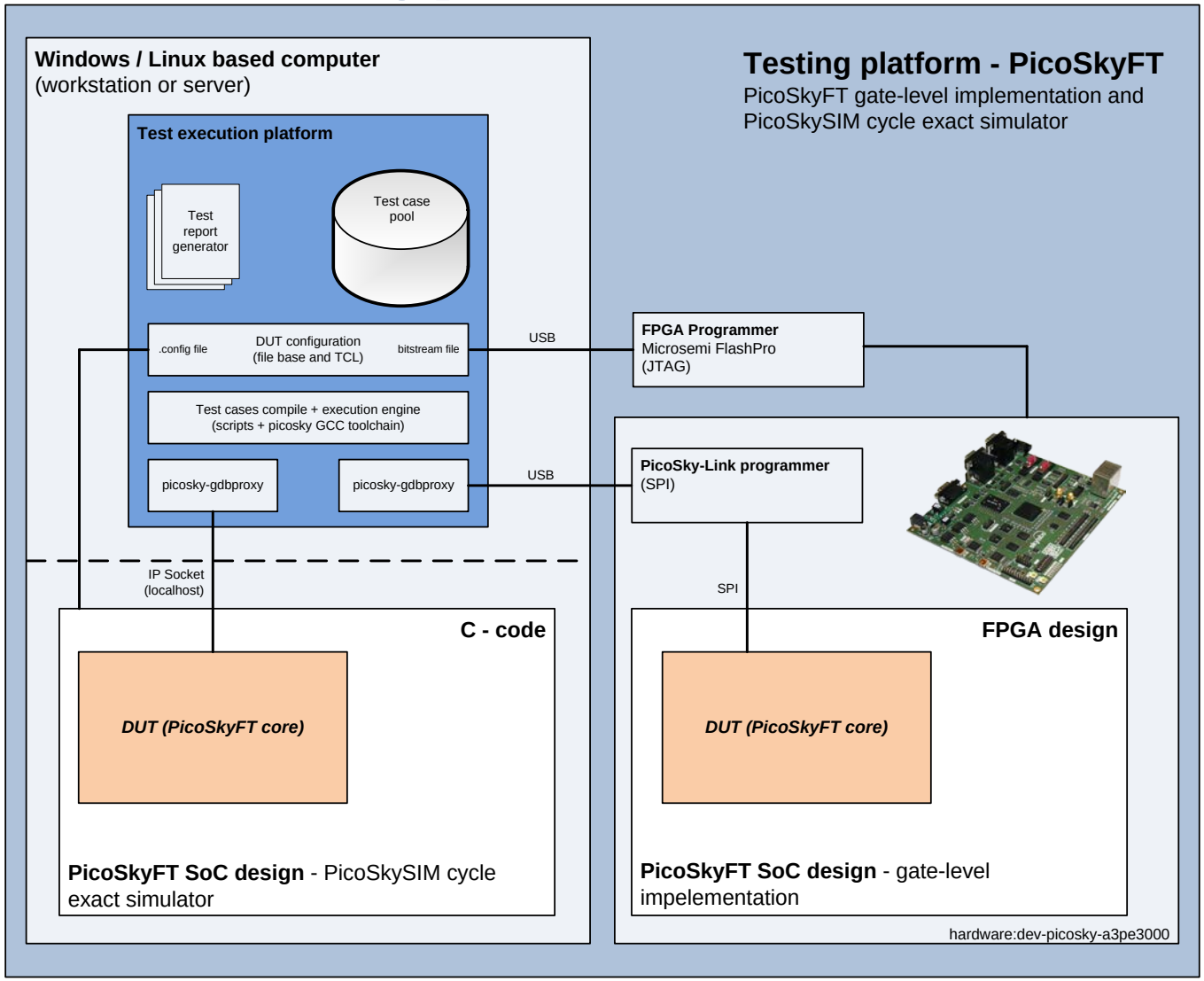
- Verification methodology follows a regression testing approach, on:
  - RTL implementation
  - PicoSkySIM simulation



Hierarchical view of requirements sections

PicoSkyFT Validation project

Validation testing platform



Testing platform architecture

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PicoSkyFT Validation project

Activity results

- More then **4000 test cases** implemented (and still counting) for PicoSkyFT processor and its companion SDK tools.
- Developed automated regression and fuzz testing platform
  - Artificially inducing errors (PM, DM and RF).
- Testing campaign revealed 7 bugs (RTL) and 15 in (PicoSkySIM).
  - Bugs fixed within the 7th evolution of PicoSkyFT and PicoSkySIM.
  - PicoSkySIM bug mostly related to clock exactness issues.
- Identification of partial TMR PicoSkyFT core on a systematic way and develop a TMRCreator tool to apply full TMR or partial TMR on netlist level.
- The validation testing campaign successfully concluded and PicoSkyFT reached **TRL 4.**

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PicoSkyFT Radiation testing

- ESA Project title: Radiation Characterization of Space Rated Microcontroller Softcore with High Energetic Proton Beam
- contract number: 4000112637/14/NL/NDe CCN2
- Project status: TO reviewing final deliverables
- KO: 1.10.2016
- Project finished: planned by the end of 2017

- Objectives:
  - To furthermore extend and rise the TRL level of the PicoSkyFT processor with testing in relevant environment with high energetic proton beam.
  - Verify processor mitigation techniques against single event effects and confirm its suitability for LEO and other proton dominated missions.

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PicoSkyFT Radiation testing

- Radiation testing has taken place at PSI – PIF. Using high energy protons.
  - Selected energies: 75, 150 and 225 MeV.
  - Flux rates: 2.71E+06 up to 1.17E+08 p/cm^2.s
  - Target fluence per test run: 1E+11 p/cm^2.s
- PicoSkyFT testing vehicle was Microsemi ProASIC3 (A3PE3000l-1PQ208) FPGA
  - Known performance under high energy proton beam
  - Safe device operation up to at least 20kRad
  - Known SRAM and FF (flip-flop) cross-sections and SEL immune
- Prepared 6 different PicoSkyFT-SoC-Basic DUT configs
  - Enabling systematic testing approach (first time SkyLabs ever performing such test and in addition on a extremely complex design).

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PicoSkyFT Radiation testing

- Each DUT has be prepared with no TMR (DUT-x1), full TMR (DUT-x2), and partial TMR (DUT-x3).
- All peripherals used fTMR in case of PiocSkyFT with pTRM or fTMR.

DUT	PM	DM	PLL
DUT-A1	Ext. SRAM	Ext. SRAM	No
DUT-B1	Ext. SRAM	Ext. SRAM	Yes
DUT-C1	Ext. SRAM	Int. SRAM [+Ext. SRAM for counter vars]	Yes
DUT-D1	Int SRAM	Int SRAM [+Ext. SRAM for counter vars]	Yes
DUT-E1	Int SRAM	Int SRAM [+Ext. SRAM for counter vars]	Yes

- All *Int SRAM* have capability to use hardware acclerated memory scrubber (with configurable scrubbing period).

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PicoSkyFT Radiation testing

Radiation testing platform

- A radiation testing platform for the PicoSkyFT processor has been developed.
  - Using Microsemi ProASIC3 testing vehicle for PicoSkyFT radiation testing.
  - DUT board + Monitoring board with fully customized logging and monitoring of DUT.

a) High speed DUT Heartbeet interface.

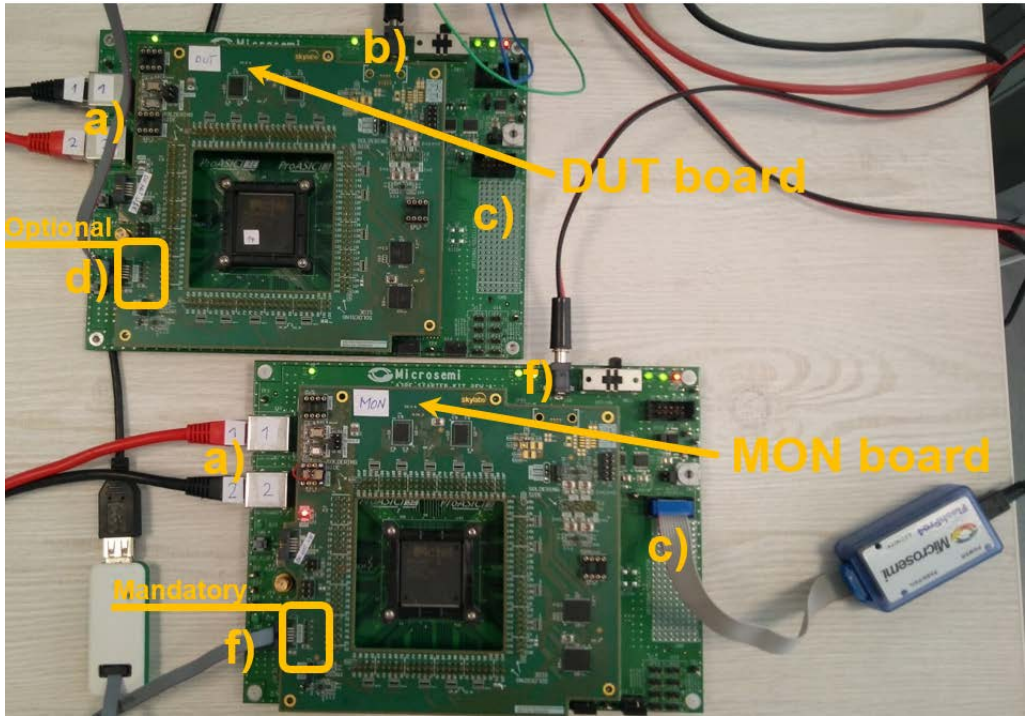
b) DUT board power supply

c) FPGA Programming (optional)

d) DUT board – PicoSkyLINK for uploading DUT firmware.

e) MON board power supply

f) MON board – communication with PC software



Radiation testing platform

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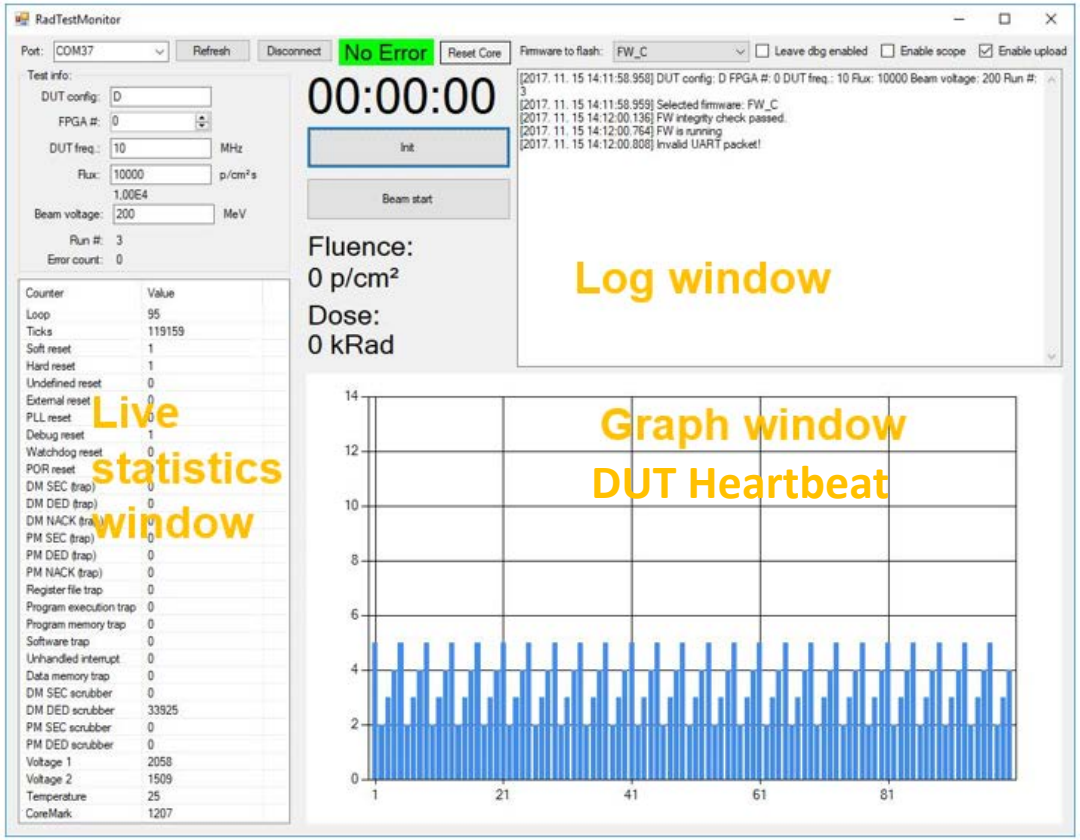
PicoSkyFT Radiation testing

Radiation testing monitor software

- PC software for real time monitoring and logging.
- Possibility to upload different firmware remotely, monitor DUT behaviour via several counters
- Logs are saved to a hard drive
- For easier, visual interpretation of DUT status, the software also contains a graph showing live DUT heartbeat

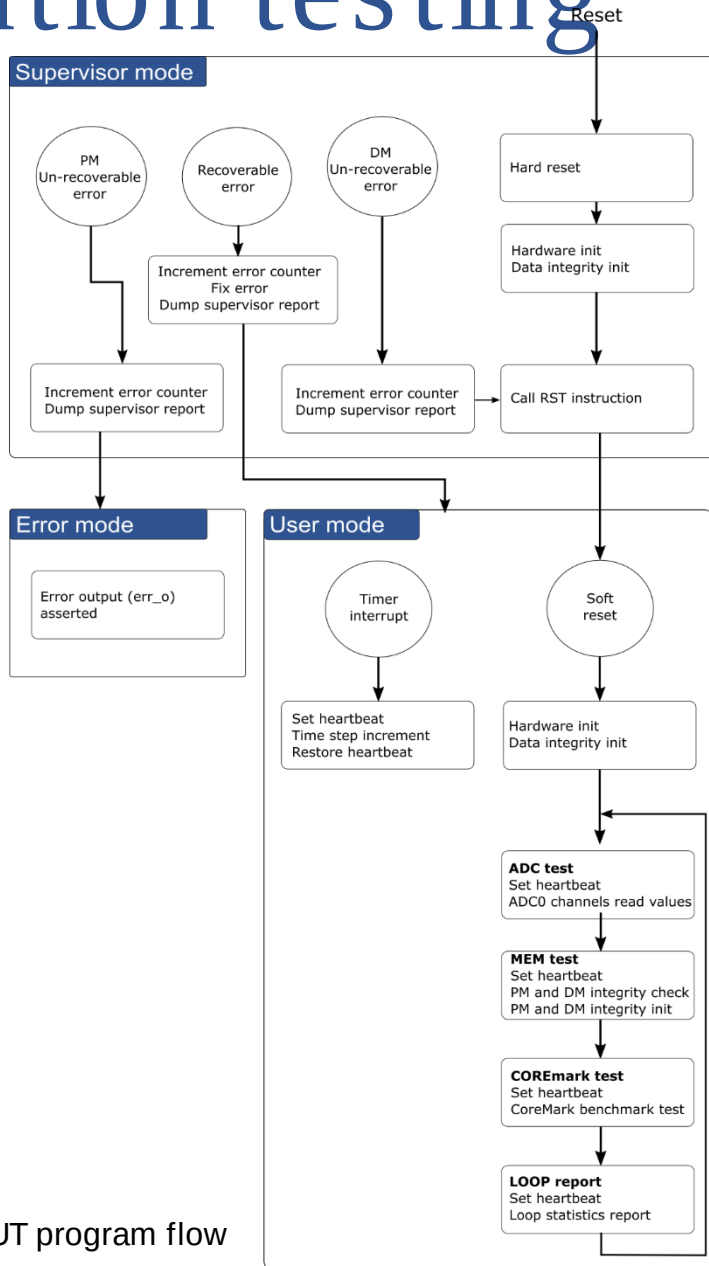


Radiation testing monitoring and logging software

PicoSkyFT Radiation testing

PicoSkyFT Testing firware

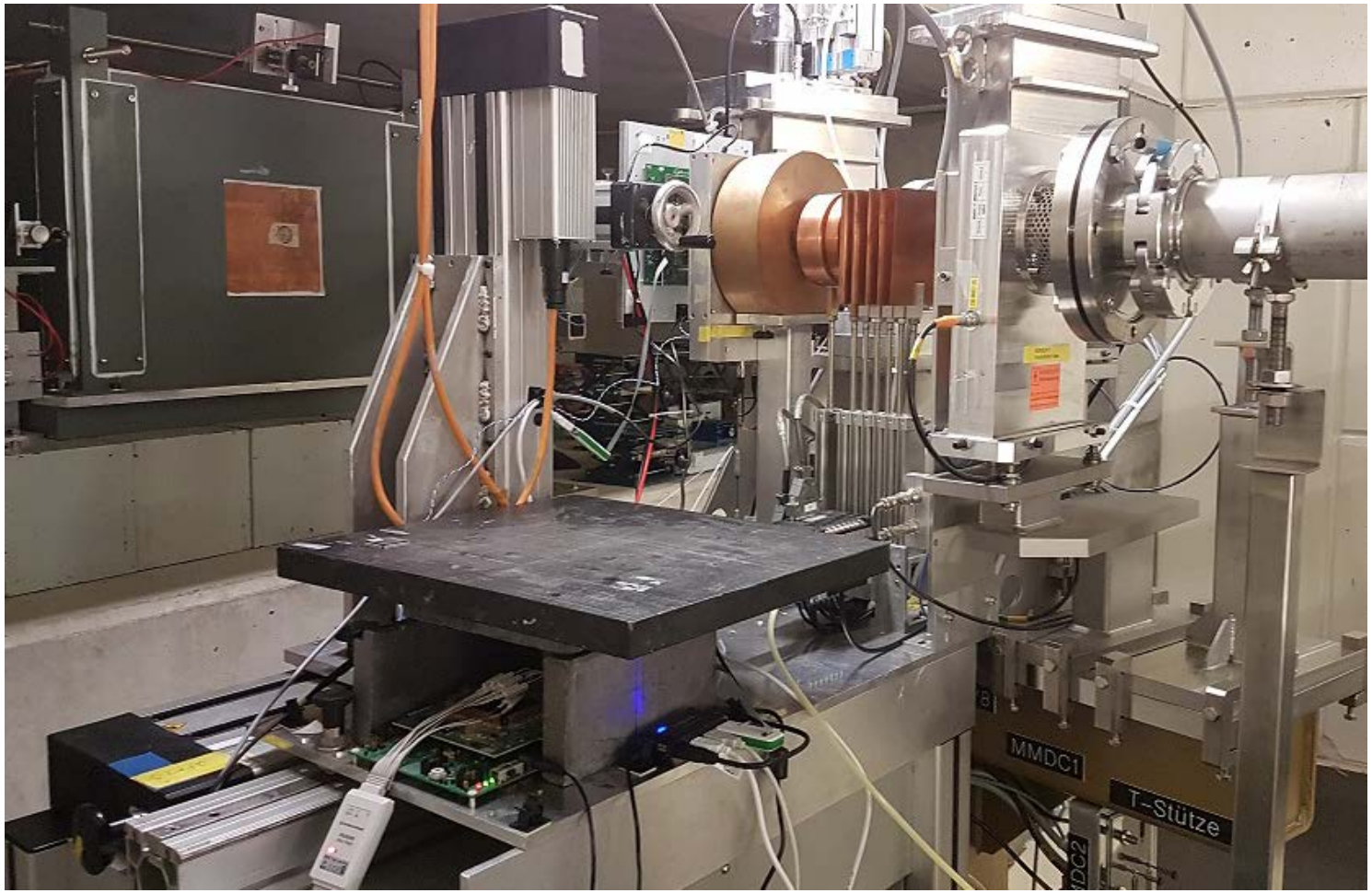
- Running firmware emulates a typical program flow on a mission such:
  - reading and writing to memories,
  - performing arithmetic operations,
  - sending data via to peripherals units (SPI, UART, GPIOs, ADCs).
- Single threaded firmware with the following functions were provided:
  - Heartbeat - 4 GPIOs
  - AD conversion of 3 channels
  - Data integrity check
  - CoreMark benchmark test
  - Fault detection statistics report (to PC)
- Functions were constantly in a loop, each function, trap or interrupt signalled unique sequence of Heartbeat.
- Upon unrecoverable error, processor is reset manually.



DUT program flow

PicoSkyFT Radiation testing

Setup at PSI



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PicoSkyFT Radiation testing

Testing results

- Highly successful radiation testing campaign (10h of testing).
  - Total fluence: 1E+12 p/cm^2
- PicoSkyFT Processor has successfully detected in total 18 events, where processor stopped further code execution, in order to prevent potential erroneous operation.
  - In all cases processor made proper reaction.
  - No SEFIs encountered on PicoSkyFT nor FPGA.
- PicoSkyFT had 3 sporadic resets
  - 1x soft-reset in non TMR'ed configuration (SET/SEU in *idc_rst*)
  - 2x in fTMR configuration -> SET in reset logic
- 27k of SEU in FPGA SRAM has been detected and successfully mitigated.
  - 4 SEU / second - worst case

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PicoSkyFT Radiation testing

Testing results

- Gathered Cross-section comparable with know radiation characteristic of the ProASIC3.

- A1: confirmed proper operation of EDAC on PM and DM with with high statistical confidence level.
- D2: Due to higher resource utilization of fTMR compared to a non-TMR version higher probability of SET has been expected. fTMR logic confirmed due to no observed SEU on the register file.
- D3: pTMR has 38 % lower FF count than full TMR version of PicoSkyFT, thus better CS measured.
- No unsafe SEFI recorded or external reset needed, therefore safety of PicoSkyFT is 100%.

DUT	Freq [MHz]	Energy [MeV]	Fluence [p/cm²]	SRAM - CS / bit	FF - CS / bit (RF)	PicoSkyFT Reset - CS / dev	FF - CS / bit (SOC)	Availability	Safety
A1	16	75	4,20E+09	3,36E-14	-	-	-	100,00%	100,00%
A1	16	151	4,24E+09	2,52E-14	-	-	-	100,00%	100,00%
A1	16	225	5,77E+10	2,44E-14	1,80E-14	1,73E-11	7,03E-15	99,93%	100,00%
D1	10	75	1,15E+09	1,15E-13	-	-	-	100,00%	100,00%
D1	10	151	4,79E+09	1,56E-14	2,17E-13	2,08E-10	8,47E-14	99,93%	100,00%
D1	10	225	4,76E+11	3,49E-14	4,37E-15	1,46E-11	4,26E-15	99,84%	100,00%
D2	10	75	3,60E+10	1,27E-13	-	5,56E-11	-	99,87%	100,00%
D2	10	225	2,66E+11	3,20E-14	1,17E-14	3,37E-11	-	99,67%	100,00%
D3	10	75	2,18E+10	3,93E-14	-	-	-	100,00%	100,00%
D3	10	225	1,06E+11	3,58E-14	-	9,46E-12	-	99,91%	100,00%

PicoSkyFT Radiation testing

Conclusion

- Results on proton beam shows very robust design and confirming the mitigation techniques work properly.
- Only SEC' were observed in SRAM memories and properly mitigated with processor or memory scrubber, depends on PicoSkyFT configuration.
- In comparison to HIREX report (A3PE3000L), cross sections for FPGAs internal SRAM and FF are comparable (within less then two orders of magnitudes)
- Several FPGA devices were tested and irradiated to around 20Krad (Si) before changing the device.
- There were no failed FPGA devices and no observable SEL interrupts were measured
- Further test are planned to be done with ESA at CERN and neutrons testing with University.

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Use cases

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PicoSkyFT use cases

- Small footprint and radiation tolerant by design PicoSkyFT processor is the key enabling technologies to reduce system complexity and increase reusability.

- Enables true distributed intelligent system
  - Parallelized verification on the equipment level will become reality.
  - Faster deployment of system, like RTU, for new satellite (NRE significantly reduced per project base)
  - Reducing harness, power consumption and offloading main OBC.
  - One step closer to fully autonomous system.

- Integration to equipment (sensors, actuators,..) to add certain local intelligence and thus provide to system information instead of data.
  - Enabling data fusion already at sensors/ actuators level.

- Safety module for monitoring and controlling other FPAGs in application, like SDR, high performance processing units,...
  - PicoSkyFT in Flash based technology.
  - Observing high-performance FPGAs (which are usually SRAM based an highly SEE susceptible).

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Next steps

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PicoSkyFT Next steps

- The same radaition testing platform has been tested in CERN CHARM facility (2 week ago).
  - Heavy ions (Argon) 40 GeV
  - Analysis undeway (no PicoSkyFT SEFI detected)
- Q1/2018 planned to used the same testing setup at high energy neutron beam (colaboartion with University of Maribor)
- Preperation for PicoSkyFT IOD (to reach **TRL 7**)
- Several instances deployed on a TRISAT mission (first Slovenian satellite – launch in Q1/2019)

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Thank you

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