Development of a microcontroller Soft-Core

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SkyLabs PicoSkyFT processor represents the next generation of soft-core microcontroller device for operation in the most safety-critical applications. The complete soft-core is designed with Verilog RTL and therefore synthesizable for all major FPGA technologies on the market. Processor PicoSkyFT has integrated several error mitigation techniques to achieve fault free operations in harsh environment. Compact, configurable, scalable and highly flexible 8/16-bit FT core for embedded systems based on SoC design approach is targeting smaller, cost effective and low power FPGAs, where implication of many available 32-bit FT counterparts would present excessiveness in terms of performance and design complexity. It's high reliability, availability and data integrity directly addresses many distributed aerospace applications, like compact payloads and data storages, intelligent remote terminal units, communication nodes, smart sensors, and similar.

PicoSkyFT development environment is equipped with complete Software Development Kit (SDK) based on GNU Compiler Collection (GCC) toolchain, integrated Debug Support Unit (DSU), powerful PicoSky-Link programmer / debugger HW key and cycle exact PicoSkySIM SW simulator with PicoSkySIM-Interface extension board to connect simulated environment with real world.

Core reliability in harsh environment is increased by added on the fly (no time penalty) EDAC (H(8,4) SEC/DED) unit, Parity protection unit and error handling unit (Trap controller). Bit scattering pattern can be selected and enabled at build time for memory devices, susceptible to Multiple Bit Upsets (MBU). Processor operates in five distinguished modes including supervisor mode to mitigate upsets and prevent uncontrolled execution of privileged instructions. Supervisor mode is triggered whenever the core detects unusual behaviour that violates correct execution in user mode. Trap controller in supervisor mode serves different type of errors (traps) to provide more information upon detected fault and thus enables better fault isolation. Traps are handled completely independent from the application state of user mode. The FDIR policy for error handling in supervisor mode can be defined only at design time.

High code efficiency and performance is provided by powerful instruction set (in total having 140 instructions), efficient addressing modes, by comprehensive interface between a register file (32 8-bit registers) and 8-bit or 16-bit independent data paths to and out of ALU (direct addressing of one or two independent registers in a single clock cycle). The instruction set and addressing modes can be optimized during design time to fully adopt compact, small, medium and large program memory models ranging from 8k up to 8M bytes of addressable space and normal or extended memory models from 64k up to 16M bytes for data memories and peripherals. This gives the possibility to optimize the processor core according to the application needs. In such a way, resources utilization can be reduced and consequently the design complexity, which furthermore reduces SEU/SET effects probability. To increase SEE (SEU, SEL) robustness on design level, PicoSkyFT registers can be triplicated with proprietary PicoSky TMRcreator tool to incorporate spatial and temporal redundancy.

Verification methodology of the PicoSkyFT processor followed a regression testing approach. Special testing platform was provided to test PicoSkyFT gate-level implementation and PicoSkySIM cycle exact simulator at the same time. In overall the soft-core verification run through more than 3300 test cases covering: ISA instruction set, special functionality (such as checking protection register, interrupts, program store enable bit, data memory wait signal), EDAC functionality, ERROR state, Supervisor TRAP handling and Special firmware & algorithms (CoreMark, Memory testing, CRC16-CCIT algorithm).

Radiation characterization of PicoSkyFT SoC implementation with proton beam at PSI has confirmed implemented mitigation techniques and high cross section level has been achieved.