

Prototyping of Space Protocol(s) for SPI

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12/12/2017

Budget + Program: TRP (two parallel contracts)

Planned Duration: 12 months

Actual Duration: 28 months

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Technical Support: Carlos Urbina Ortega(TEC-EDD)

SCOPE OF THE WORK:

The objectives of this activity are:

- To perform a detailed definition and **analysis of use cases** for SPI bus in space
- **Build a draft specification** for SPI protocols based on space applications use cases
- To propose and prototype appropriate **signal integrity techniques** that can establish guidelines for its implementation
- To develop a representative **demonstrator** for SPI in space
- To Create general **simulation models** for SPI and validate them on the demonstrator hardware with real measurement correlation.

Prototyping of Space Protocol(s) for SPI



Contractor(s): Cobham (Sweden)
Sub-Contractors : AAC Microtec (Sweden)

ESA Budget:

400 k€

TRP T701-402ED

COBHAM



TRL Initial: 2 Current: 4 YoC: 2015 TO: G. Magistrati (TEC-EDD)

Background and justification: The ECSS-E ST-50-14C defines analogue interfaces, bi-level discrete interface and serial digital interface (16-bit). Considering the most recent sensor acquisition methodologies that are dominating the industrial world the space community should update the standard in order to include the recent and conceivable evolution of sensors acquisition systems. A natural evolution is pushed by the need to increase the signal integrity and resolution of the transmitted signals, maintaining in any case very low power consumption (or even further decreasing it), and by the availability of miniaturised ASIC-sensors able to locally include the sensor biasing and signal conditioning/processing functionalities. Those capabilities make the need for the definition of standards for digital transmission of sensor data in spacecraft, very pressing, and this is the focus of the present activity.

Objective(s): To perform a detailed definition and analysis of use cases for SPI bus in space, build a draft specification and develop a representative demonstrator together with general simulation models validated on it through real measurement correlation.

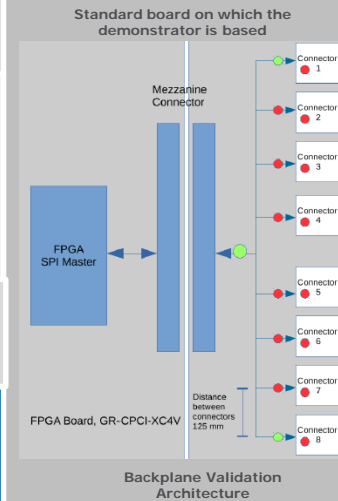
Achievements and status:

This activity has prototyped SPI protocol(s) and physical layers for space applications. A draft specification taking into account existing solutions has been derived and Signal integrity techniques and also differential variants of the physical layer were investigated and prototyped in order to improve the communication quality and integrity. The SPI model(s) and code(s) for the demonstrator were developed (including HDL IP-core).

Benefits: Thanks to the development, the standardization process for SPI can start with real grounds on the different trade-offs to be made, which will guarantee the future interoperability and homogeneity of its use on the space market. Furthermore, a company is now ready to provide a standard SPI IP core, simulation models and a demonstrator test-bed on its portfolio.

Next steps: To complete the same exercise with the parallel contract and start a ECSS working group with the specifications of both activities as input.

Target
TRL: ?
Date:
2018Q1





Prototyping of Space Protocol(s) for SPI

TEC-ED and TEC-SW Final Presentation Days – 12 December 2017

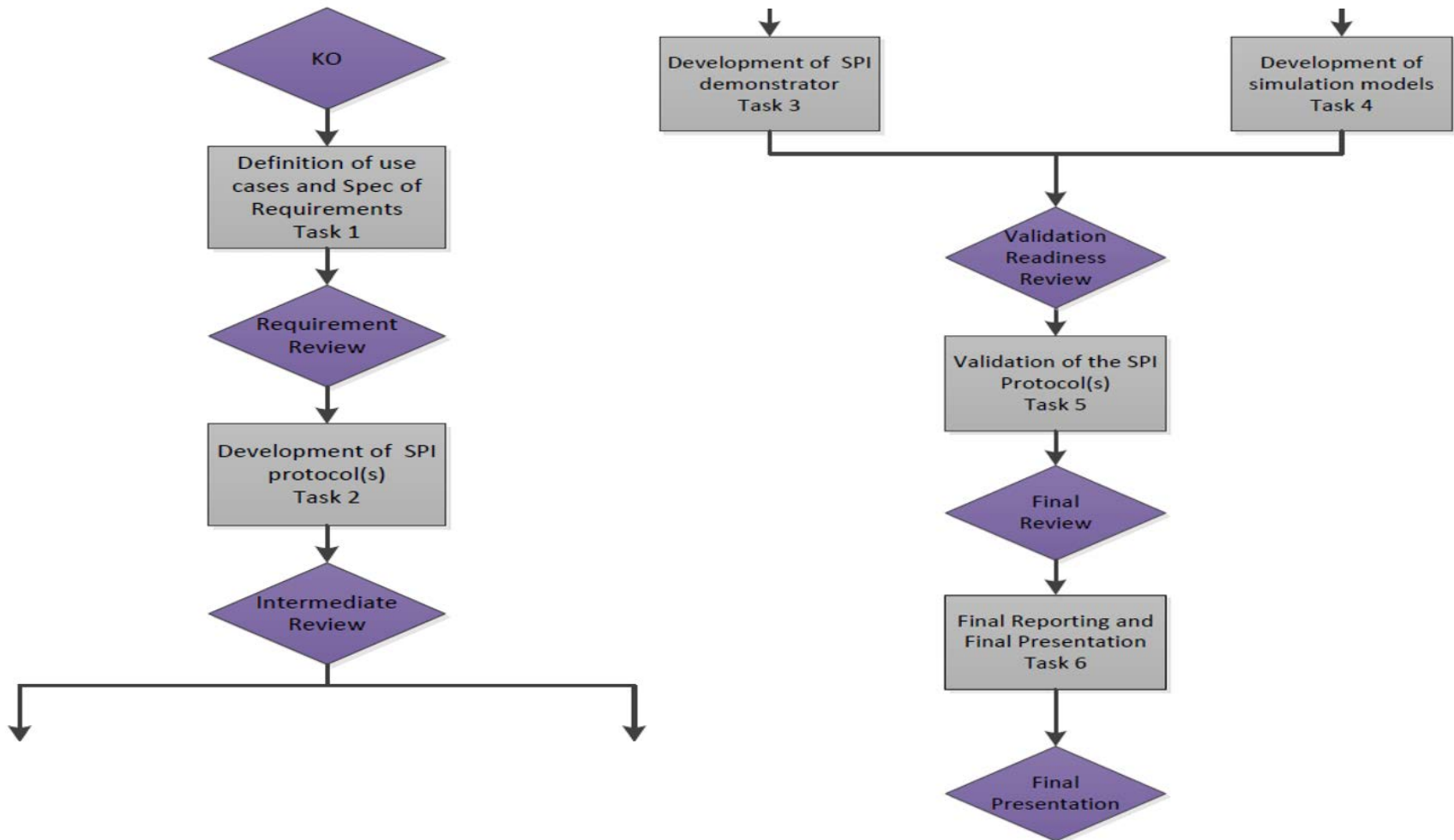
in cooperation with



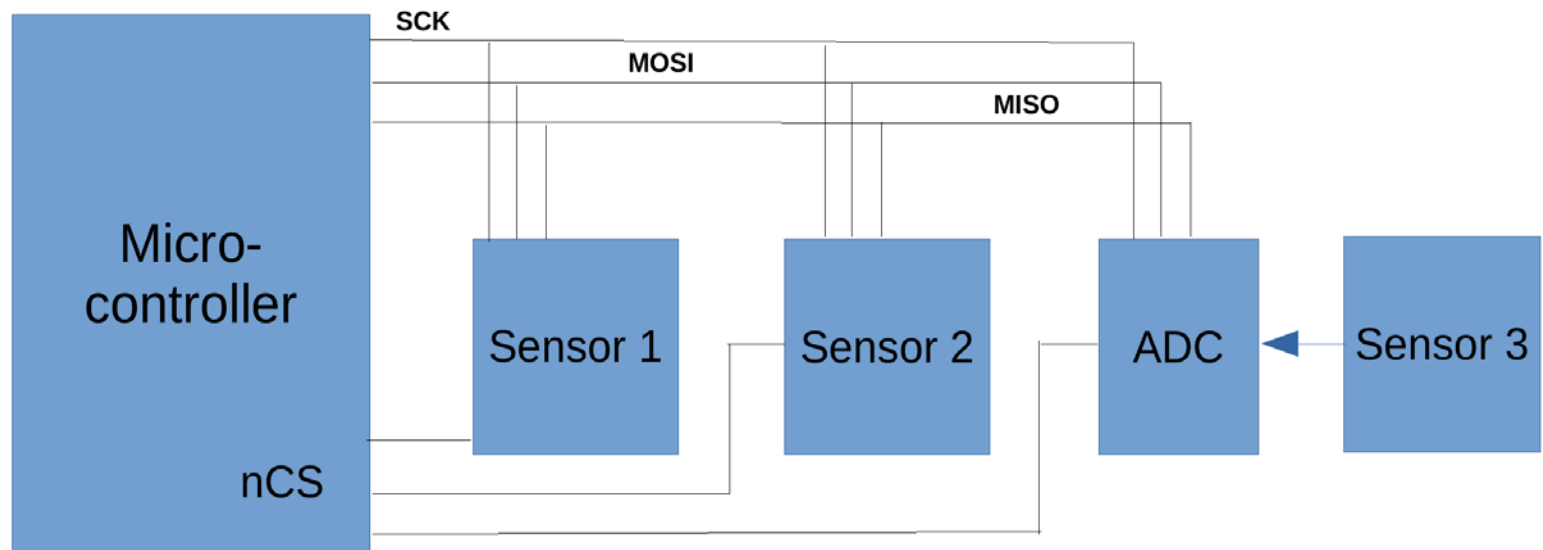
- Prototyping of Space Protocol(s) for SPI: initiated and funded by ESA/ESTEC under contract 4000114112/15/NL/LF
- This activity has proposed and prototyped SPI protocol(s) and physical layers for space applications based on
 - The intermediate results of TEC-EDD activities
 - Modular RTU – GSTP
 - Standardization of Digital interfaces – TRP
 - Also acquiring inputs from companies and entities being module/unit designers or space component manufacturers
- Work performed by
 - Cobham Gaisler, Gothenburg, Sweden (Prime)
 - AAC Microtec, Uppsala, Sweden

- Introduction
- Objectives
- Activity overview
- Work performed
- SPI overview
- Protocol definition
- Redundancy
- System design
- Physical layer definition
- Protocol tests
- Summary of tests and simulations
- Outcome of the activity

- To specify the physical layer, data link layer and network layer for the SPI communication
- To prototype the physical layer, data link layer and network layer for the SPI communication
- To model and simulate layers
- To develop a demonstrator platform
- To analyse and measure performance of the demonstrator



- Detailed definition and analysis of use cases for SPI bus
 - Internal backplane bus inside a unit
 - Serial bus for reprogrammable logic on board interface with sensors
 - Interface with standard IC's
 - Interface using cables



- Questionnaire developed, feedback collected, analyzed and reported
 - 30 questions
 - Responses from 15 different stakeholders within the Industry
 - Majority response
 - Comments from the Industry
 - Simplified redundancy options
 - All Modes (CPOL, CPHA supported)
 - MSB first
 - Mandatory chip select
 - SPI over cable, point to point, LVDS, microD
 - Detailed definition of structured messages
 - CRC checksum

- Specification of layers

- Physical layer

- Connectors, cables, cable assemblies, voltage levels, noise margins, PCB tracks, signal encoding, data transfer rate and redundancy solutions.
 - Three different alternatives for the electrical signals to be transferred, called routing cases, are defined:
 - PCB internal communication
 - PCB to PCB via backplane
 - Cable, using LVDS

- Data link and Network layer

- Different communication protocols are defined to provide a generic solution for existing devices and a separate protocol for high or medium traffic load with detailed data and network layer definition.
 - This layer provides data word formats, message formats defining commands and responses, data integrity and redundancy solutions.

- Development of SPI protocols and layers

- VHDL and Simulation models

- Development of a demonstrator of SPI bus
 - GR-RASTA-SPI
 - Platform GR-CPCI-XC4V
 - Mezzanine Boards
 - GR-CPCI-MEZZ-SPI-PCB (PCB internal communication)
 - GR-CPCI-MEZZ-SPI-ZPACK (PCB to PCB via backplane)
 - GR-CPCI-MEZZ-SPI-LVDS (Cable, using LVDS)
- Development of simulation models
 - Simulation models for routing cases have been developed.
 - Physical layer parameters affecting signal integrity
 - Some simplifications - minimize simulation times.
 - A separate crosstalk model

- Demonstration of the functional and performance features (validation of the SPI protocols)
 - Physical layer tests
 - Correlation of simulation models and hardware demonstrator results
 - Performance analysis using models and demonstrator
 - Functional and logical verification of the protocols

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ESA contract: 4000114112/15/NL/LF
Deliverable: D13

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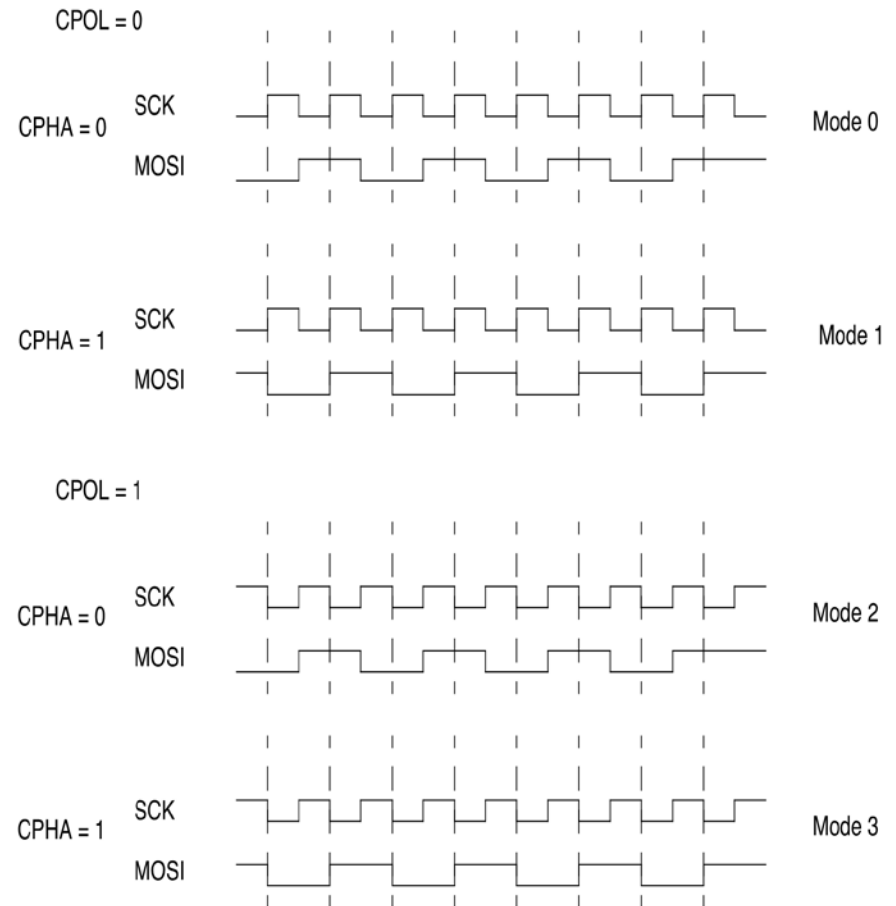
- Full-duplex synchronous serial bus.
 - Transmission starts when a master selects a slave through the slave's chip (or slave) select signal and the clock line (SCK) transitions from its idle state.
- The signals of the SPI protocols are:
 - Serial Clock (SCK) driven by a master: serial clock to all the slave devices
 - Master Out Slave In (MOSI): data from the master to the selected slave.
 - Master In Slave Out (MISO): data from the selected slave the master device.
 - Chip Select(s) (nCS#): independent to each slave, only driven by master

SPI overview

Configurations

- The SCK, MOSI and MISO signals shall be possible to configure in the four different modes (Mode 0, 1, 2, 3)
- CPHA (Clock Phase) controls write or read transition
- CPOL (Clock Polarity) controls idle state of SCK
- The idle state of SCK shall be either high or low.

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1



- The protocol SPI-0 is generic and to be used for interfacing existing devices
- The protocol SPI-1 targets 8, 16 and 24 bit data word communications.
 - To guarantee the quality of data transmission a Parity bit is included at SPI word level.
- The protocol SPI-2 targets 16-bit data word communications.
 - The data and network layer provides data word formats, message formats defining commands and responses, data integrity and redundancy solutions.

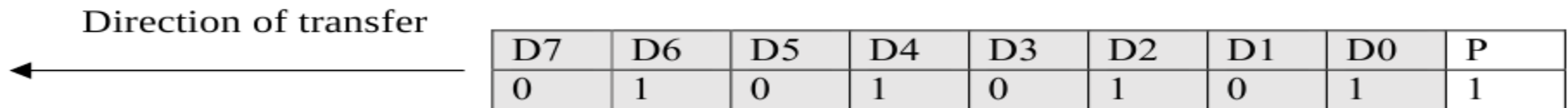
- SPI-0 protocol
 - Word width shall be as per the requirements of the implementers.
 - Recommended word width shall be 8 bits.
 - Word bit ordering (MSB first or LSB first transferred) shall be as per the implementers.
 - Recommended bit ordering: MSB transferred first and LSB last.
 - The contents of the message, type of message, and number of words per message shall be as per the requirements of the implementers.
 - The implementers can choose any data integrity solutions (e.g. parity, CRC)

Protocol definition

Data Link Layer (SPI-1 and SPI-2)

- SPI-1 protocol

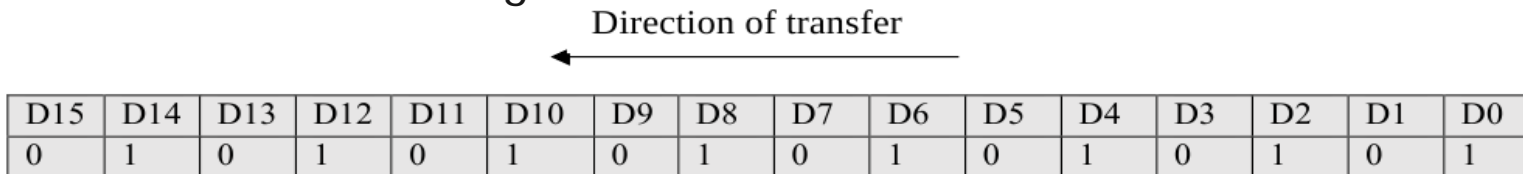
- Word width shall be 8, 16 or 24 bits.
- Word bit ordering shall be MSB transferred first and LSB transferred last.
- Parity bit shall be included at word level. The master device shall have the option to choose odd or even parity.



Example 8 bit data 0x55 transfer, odd parity, MSB first

- SPI-2 protocol

- Word width shall be 16 bits.
- Word bit ordering shall be MSB transferred first and LSB transferred last



Example 16 bit data 0x5555 transfer, MSB first

Protocol definition

Detailed Network layer, SPI-2 protocol

- Message format
 - Message header: Command token for the master and Response token for the slave
 - Optional data words and CRC checksum
 - The CRC is mandatory
 - The received messages shall be processed by the SPI slave device, response and data shall be transferred as per the received command.

Signal	Message Header		Payload	Payload CRC
MOSI	Command #1	Command #2	Data	CRC-16
MISO	Response #1	Response #2	0x0000	0x0000

Example Message format (Write data)

Signal	Message Header		Payload	Payload CRC
MOSI	Command #1	Command #2	0x0000	0x0000
MISO	Response #1	Response #2	Data	CRC-16

Example Message format (Read data)

Protocol definition

Detailed Network layer, SPI-2 protocol

- Command Token

- The master transmits a message header which specifies the action need to be performed in slave.
- The message header sent by master device is called command token which consist of two 16-bit words.

MSB Command Token Word #1															LSB
Prefix		Command Code						Spare		Message Length					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
'0'	'1'	C5	C4	C3	C2	C1	C0	'1'	'1'	L5	L4	L3	L2	L1	L0

Command word #1

MSB Command Token Word #2															LSB
Prefix		Sub-address								Spare		CRC-4			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
'0'	'1'	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	'1'	'1'	CRC3	CRC2	CRC1	CRC0

Command word #2

Protocol definition

Detailed Network layer, SPI-2 protocol, Command overview

Code	Command	Length	Sub-address	Payload
0x00	RESET_SPI	0x00	0x00	None
0x07	SYNCH	0x04	0x00	MOSI: <SYNC1> <SYNC2><SYNC3><SYNC4><CRC-16> MISO: <all zeros>
0x08	TICK	0x00	Used as index for increment.	None
0x0A	READBACK_CMD	0x02	0x00	MOSI: <all zeros> MISO: <CMDTOKEN>< CRC-16>
0x0D	WRITE_SA	Number of words to be written, N	SA	MOSI: <DW1> <DW2> ...<DWN> <CRC-16> MISO: <all zeros>
0x0E	READ_SA	Number of words to be read, N	SA	MOSI: <all zeros> MISO: <DW1> <DW2> ...<DWN> <CRC-16>
0x20	CONFIG-WRITE_ADDR	0x02	0x00	MOSI: <CW1><CW2> <CRC-16> MISO: <all zeros>
0x21	CONFIG READ_ADDR	0x02	0x00	MOSI: <CR1> <CR2> <CRC-16> MISO: <all zeros>
0x24	ACTIVATE	0x00	0x00	None
0x25	DEACTIVATE	0x00	0x00	None
All others	N/A	0x00		

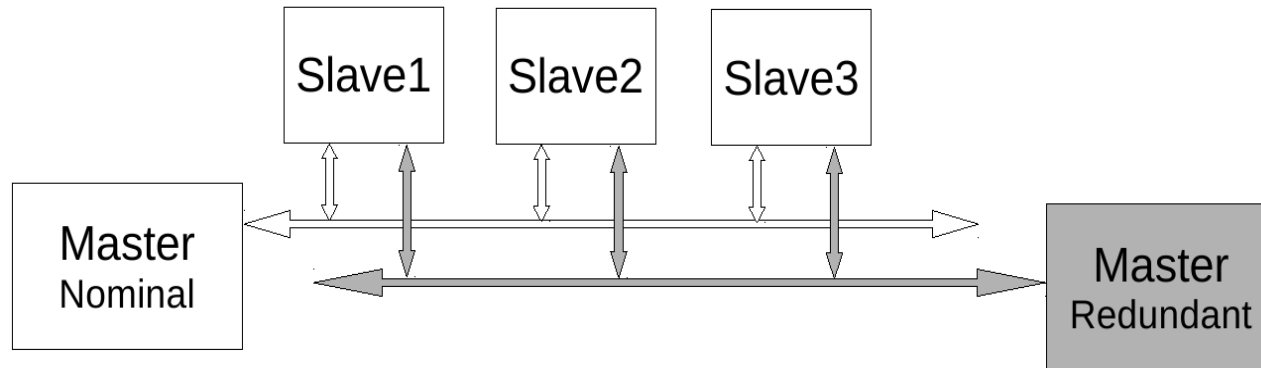
Detailed Network layer, SPI-2 protocol, Response overview

Bit	Identifier	Type	Value	Description	Clear Condition
13	SPI_TERMINAL_FAULT	Error	'0'=no fault '1'=fault	The bit shall flag a SPI terminal fault condition. The SPI master controller reaction to this flag is left to the implementers.	According to the module current state.
12	MESSAGE_ERROR	Error	'0'=no fault '1'=fault	This bit shall be utilized to indicate that the previous message received from the bus master has failed to pass the validity tests.	Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).
11	ADDRESS_ERROR	Error	'0'=no fault '1'=fault	This bit shall flag that a misaligned sub address, which did not match the used block in this module, was used in the previous command.	Always related to the previous command. Reception of a valid command will clear it (with a delay of one command)
10	ILLEGAL_COMMAND	Error	'0'=no fault '1'=fault	This bit shall flag that the previous received command was not compatible with the state of the module at the reception's instant.	Always related to the previous command. Reception of a valid command will clear it (with a delay of one command)

Bit	Identifier	Type	Value	Description	Clear Condition
0 to 3	Module State	Status	Implementation Specific	Optional bits used to express module state/condition. Details left to implementers.	Implementation Specific

- Simple duplication of sensors
 - As per the implementers need only the interfacing slaves can be duplicated.
- Two independent lanes
 - All the components of the system master, slaves and bus structures shall be duplicated. This option tolerant to any single failures.
- Cross-strapped slaves
 - The nominal and redundant masters are connected to each slave device by two serial interfaces.

Cross-strapped slaves (1)



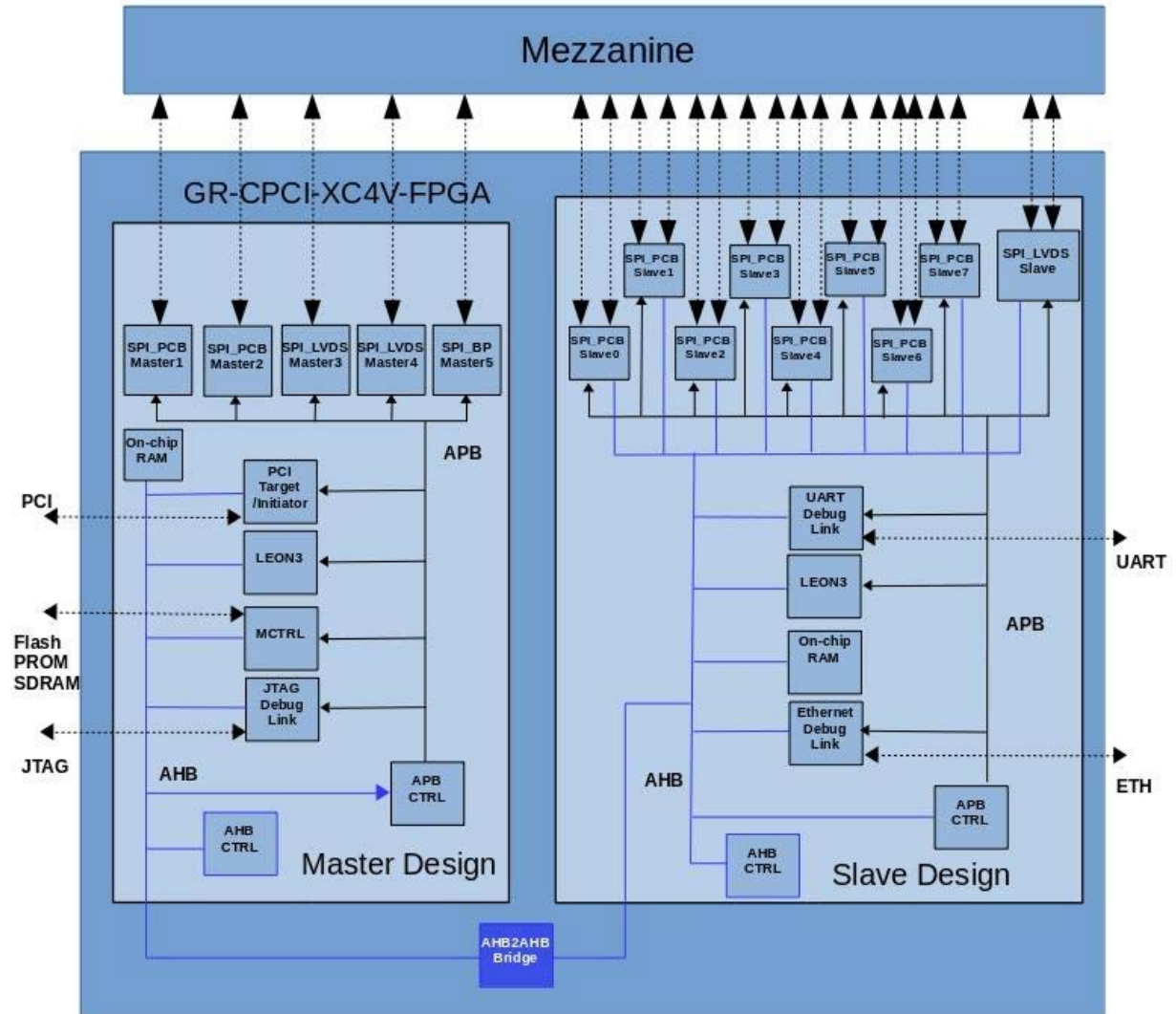
- Cross-strapped slaves

- The nominal and redundant masters are connected to each slave device by two serial interfaces.
- The slaves has two serial interfaces.
- The slave device port selection shall be performed by external configuration or using the command messages from master.
- Dedicated command codes are defined for switch over in SPI-2 protocol.

System design

Demonstrator – FPGA Design, SPI IP Cores

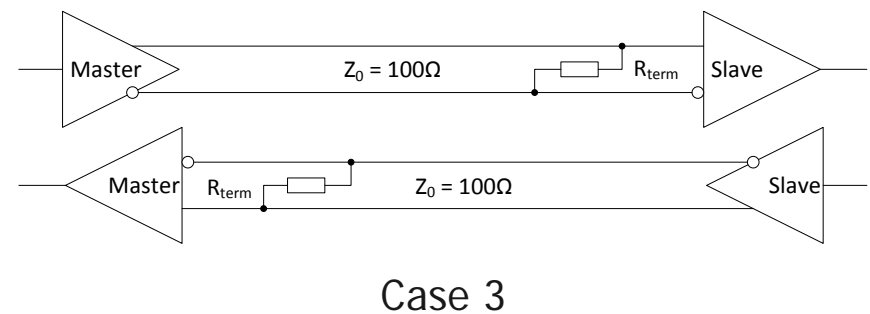
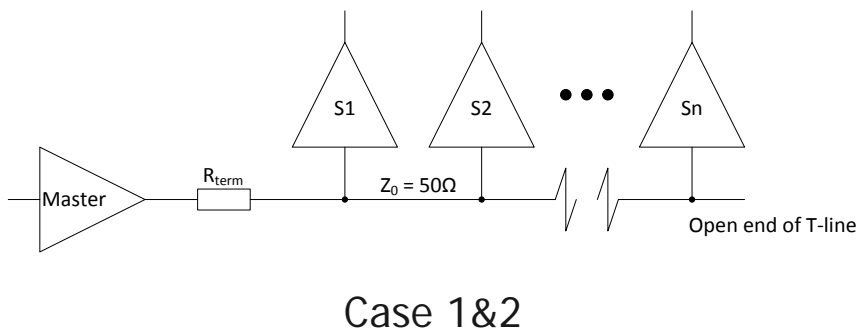
- Master and Slave: two independent SOC with dedicated processor, memory and debug links.
- Realisation of SPI protocols (0, 1 and 2): combination of HW and SW.
- Separate SPI master and SPI slave VHDL IP cores are developed.
- Drivers, Software Libraries for protocols and Test application SW developed



- Development of a hardware specification for general use of SPI in space systems
- Prioritise adherence to established common practice
- Validation of proposed ECSS standard requirements
- Development of simulation models to enable pre-evaluation of signal integrity and SPI frequency selection

Identified routing cases

- 3 cases considered:
 - 1: Multi-drop over single PCB (LVTTTL/3.3V LVCMOS)
 - 2: Multi-drop over backplane (LVTTTL/3.3V LVCMOS)
 - 3: Point-to-point using cable (LVDS)
- Cases 1 & 2 identical electrically even if physical implementation differs



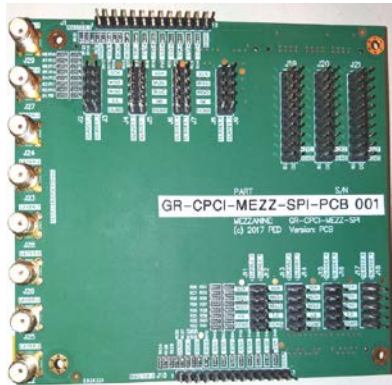
Physical layer specification

Demonstrator –HW platform

- Demonstrator developed based on Cobham Gaisler's existing RASTA avionics test bed
 - The GR-CPCI-XC4V board along with the mezzanine boards constitute the demonstration HW platform GR-RASTA-SPI
 - Purpose developed mezzanine test boards



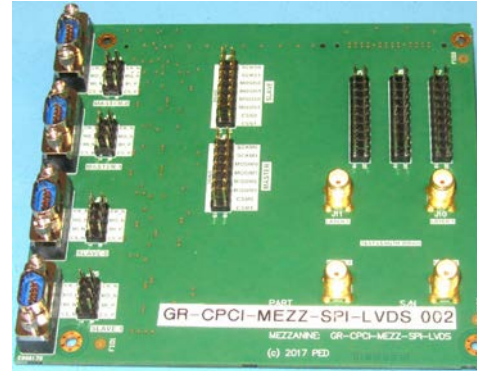
GR-CPCI-XC4V



Routing case 1:
multi-drop PCB



Routing case 2:
multi-drop backplane



Routing case 3:
Point-to-point LVDS

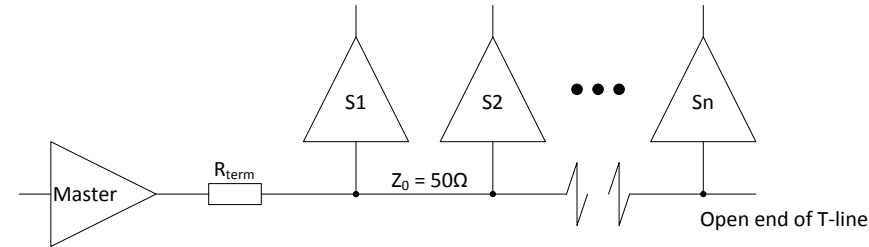


Demonstrator GR-CPCI-XC4V mounted
with GR-CPCI-MEZZ-SPI-ZPACK
mezzanine board

Physical layer specification

Routing case 1 & 2: Single ended multi-drop

- Single ended LVTTTL/LVCMOS signaling
 - Compliant with common practice
- Controlled impedance traces (50Ω)
 - Simplifying analysis of signal behavior
- Series termination only w. open receiver end
 - Allows immediate full-swing at the far end the network
 - Avoids failure propagation due to receiver end short
 - Accurate analysis of networks required to ensure signal integrity
- Slave devices in FPGA or as commercial ICs with space equivalent or of specific interest



General observations:

- Series terminated, open-end, single ended networks frequency limited through a combination of:
 - Turn around delays
 - Reflections at open-end termination
 - Heavy load on driver circuits
- Delay is an inherent limitation in SPI networks as the clock is used for both read and write of slave data
- Reflections are minimized through accurate matching in the driver end (single reflection in open end only)

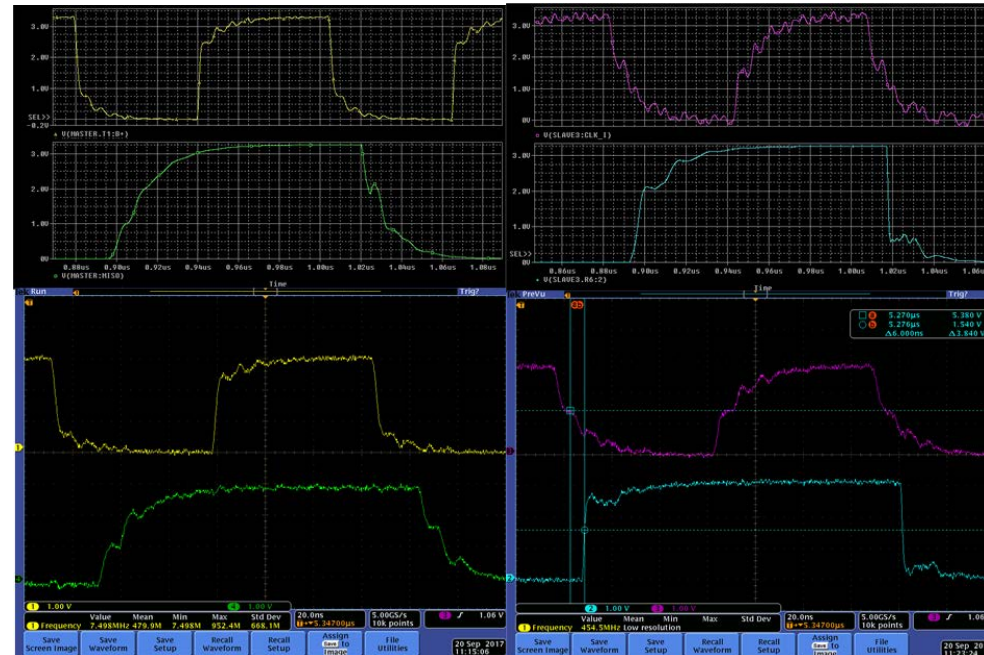
- Simulation models developed for quick evaluation of termination strategy, usable frequency range and signal integrity
- PSpice modelling selected due to familiarity and the simplicity of the modelled networks
- Manufacturer IBIS models used for both master and slave devices

Physical layer specification

Routing case 1&2: Modelling efforts

- Well correlated behaviors between simulation and measurement
- Some limitations in manufacturer IBIS models discovered (workarounds possible)
- Tool for pre-evaluating networks to achieve robust performance

Simulated



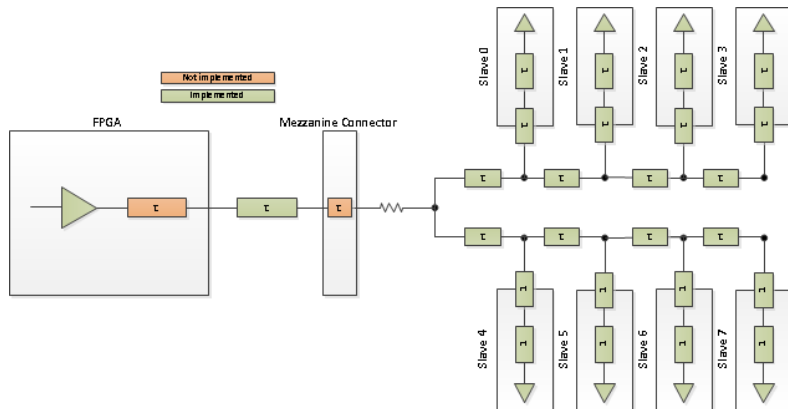
Measured

Physical layer specification

Routing case 1&2: Modelling efforts

Example of studied network configuration:

- 8-slave backplane with master at center node
- 50 cm long arms with 2cm stub length
- Central series termination
- Correlation maintained for reduced test cases



Measured maximum SPI frequency

		SPI frequency [MHz]							
Slave	Slave type	5.33	6.25	8.00	8.33	12.5	15	18	25
0	MRAM MR25					OK	NOK		
1	DAC7552	OK	OK	OK	OK	OK	OK	OK	NOK
2	Flash FL128						OK	NOK	
3	Flash SST080						OK	NOK	
4	FRAM FM25				OK	NOK			
5	ADC128S	OK	OK	OK	OK	OK	OK	OK	NOK
6	Temp AD7814				OK	NOK			
7	Flash SST020						OK	NOK	

Maximum SPI frequency estimated with simulation

		SPI frequency [MHz]							
Slave	Slave type	5.33	6.25	8.00	8.33	12.5	15	18	25
0	MRAM MR25					OK	NOK		
1	DAC7552								
2	Flash FL128								
3	Flash SST080					OK	NOK		
4	FRAM FM25								
5	ADC128S								
6	Temp AD7814				OK	NOK			
7	Flash SST020						OK	NOK	

Physical layer specification

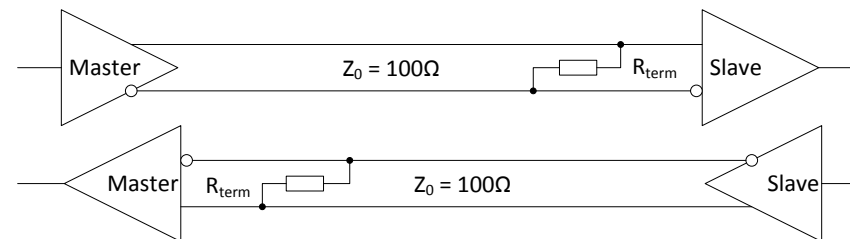
Routing case 3: Differential point-to-point

- Differential point-to-point LVDS signaling
 - High noise rejection, compatible with long distances

- Controlled impedance ($100\ \Omega$)
 - Simplifying analysis of signal behavior

- Parallel termination
 - Compliant with LVDS standard practice
 - Low power due to the low voltage swing of LVDS

- Commercial driver/receiver circuits with space equivalents
 - SN65LVDS31 and SN65LVDS33



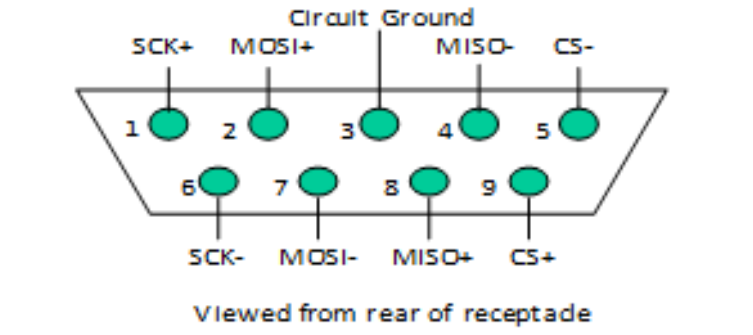
General observations:

- End-to-end matched SPI networks are limited in operational frequency through turn-around delay
- Provided with accurate delay figures:
 - Master end propagation delays
 - Slave end reaction and propagation delays
 - Trace/cable lengths and electrical characteristics
- Worst case delay analysis sufficient for sizing networks
 - Highest estimated functional SPI frequency in agreement with measured results

Physical layer specification

Connectors and cables Routing case 3

- Connector
 - Micro D type
 - Identical pinouts for Master and Slave devices
- Cable
 - Twisted pair cable type with an outer shield for EMC
 - No internal shield is used between signal pairs
 - Separate twist rates for signal pairs minimizes crosstalk



Proposed pinout

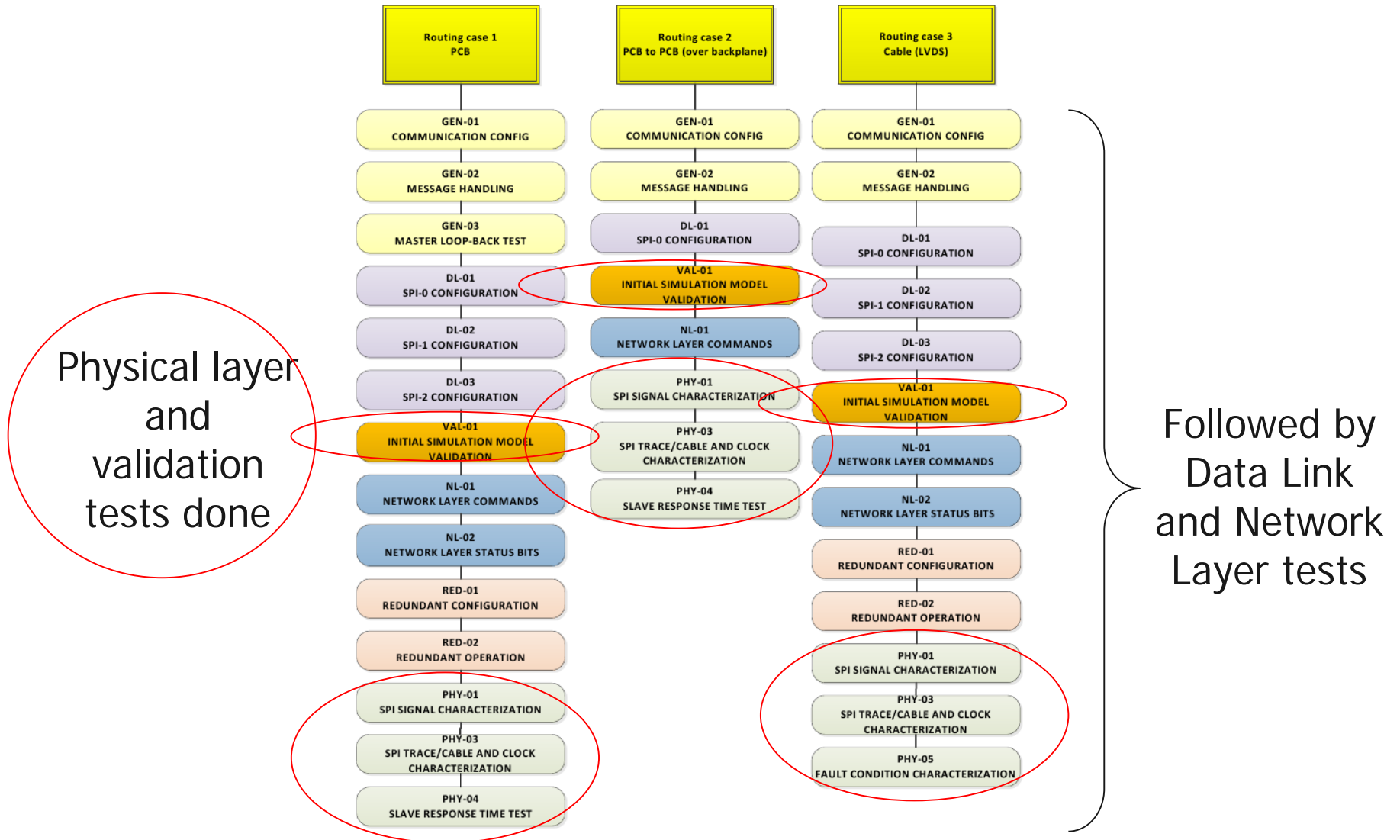
Contact Number	Signal (Master)	Direction (Master)	Direction (Slave)
1	SCK+	Output (Tx)	Input (Rx)
2	MOSI+	Output (Tx)	Input (Rx)
3	Circuit Ground	NA	NA
4	MISO-	Input (Rx)	Output (Tx)
5	CS-	Output (Tx)	Input (Rx)
6	SCK-	Output (Tx)	Input (Rx)
7	MOSI-	Output (Tx)	Input (Rx)
8	MISO+	Input (Rx)	Output (Tx)
9	CS+	Output (Tx)	Input (Rx)

- Recommended requirements for SPI networks broken down into the two identified topologies:
 - Single ended multi-drop
 - Differential point-to-point
- Focused on a achieving analyzable, robust and not overly conservative networks
- Design choices based on common practice

- Inputs to draft ECSS standardization document
- Accurate modelling techniques for single ended SPI networks
- Clock frequency estimation techniques for differential and single ended SPI networks

Protocol tests

Test overview



Protocol tests

Data Link and Network layer tests

- A selection of the configurations tested
- Configured with the maximum measured and simulated frequency from the validation tests
- Covering areas (depending on routing case):
 - Communication configuration (modes (0, 1, 2, 3), word lengths, bit ordering, different slave selections)
 - Chip Select Functionality
 - Master loop back test
 - SPI-0 configuration (word lengths, bit ordering)
 - SPI-1 configuration (word lengths, bit ordering, parity)
 - SPI-2 configuration (word lengths, bit ordering)
 - Network Layer Commands (SPI-2 protocol, all commands)
 - Network Layer Status Bits (SPI-2 protocol, all commands)
 - Redundant Configuration (slave device port selection)
 - Redundant Operation (SPI-2 protocol, all commands)
 - Slave Response Time Test

- A demonstrator and a simulation environment have been developed.
- Validation of both platforms have confirmed equivalent performance.
- The simulation environment can be used for modelling of numerous cases.
- Using the demonstrator hardware SPI protocols (0, 1 and 2) successfully tested and SPI IP cores validated
- Further details are presented in the Final Report from the activity.

- SPI VHDL IP cores – SPI Master and SPI Slave
- Drivers for RTEMS, Software Library, Test application SW
- Demonstrator Test platform (RASTA compatibility)
 - Mezzanine boards
 - PCB case
 - LVDS case
 - Cables for LVDS case (10 cm, 1 m and 10 m)
 - Backplane case
 - Available Slave devices
 - *ADC128S102 – Texas Instruments, 8-Channel, analog to digital converter.*
 - *AD7814ART – Analog Devices, SPI Temperature Sensor 10 bit.*
 - *S25FL128SAGN – Spansion, Flash, 128 Mbit.*
 - *MR25H10 – Everspin, MRAM, 1 Mbit.*
 - *SST25VF080B – Microchip, Flash, 8 Mbit. SST25VF020B – Microchip, Flash, 2 Mbit.*
 - *FM25W256-G – Cypress, FRAM, 256 Kbit.*
 - *DAC7552 – Texas Instruments, DA Converter.*
 - Schematics Board Description and user manual
 - Simulation models
 - Model description and user manual
 - Draft Standard

Thank you for listening!