

Development, Realisation and Validation of a Baseband Equipment Dual-Channel

Final Presentation @ ESTEC, December 12 2017

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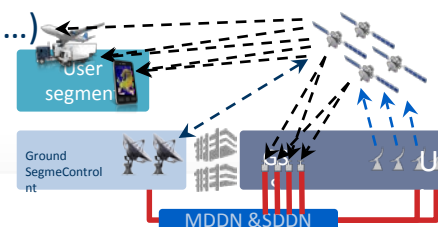
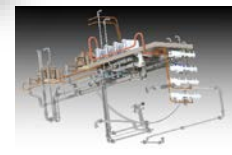
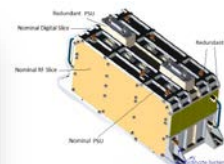
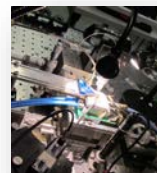
Antwerp Space
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Agenda

- ▶ Antwerp Space
- ▶ Drivers for the development
- ▶ Project structure
- ▶ Key technical challenges and achievements
- ▶ Validation campaign & subco roles
- ▶ Lessons learned
- ▶ Future work

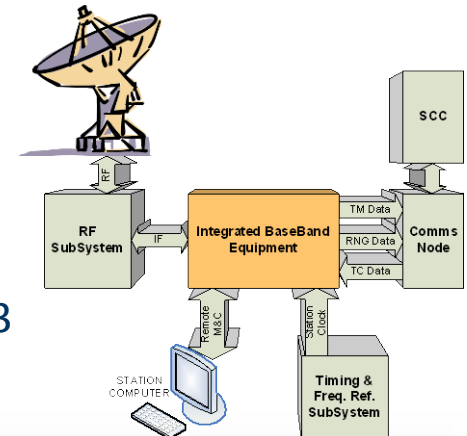
Antwerp Space

- ▶ Satellite communication experts since 1962
- ▶ An OHB company
- ▶ Both onboard and ground solution:
 - On board:
 - components for photonics
 - Modem equipment onboard ISS, RF instrument for Mars
 - Payload integration for scientific satellites (Exomars 2020, JUICE, ...)
 - Ground:
 - Modems for TT&C and high speed telemetry, frequency convertors (EESS and deep space)
 - SCOE for TT&C and payload telemetry, RF suite cases (Solar Orbiter, MTG, Hispasat, Exomars, Columbus Orbital Facility,...)
 - Secure networks (design and implementation of Galileo MDDN and SDDN)

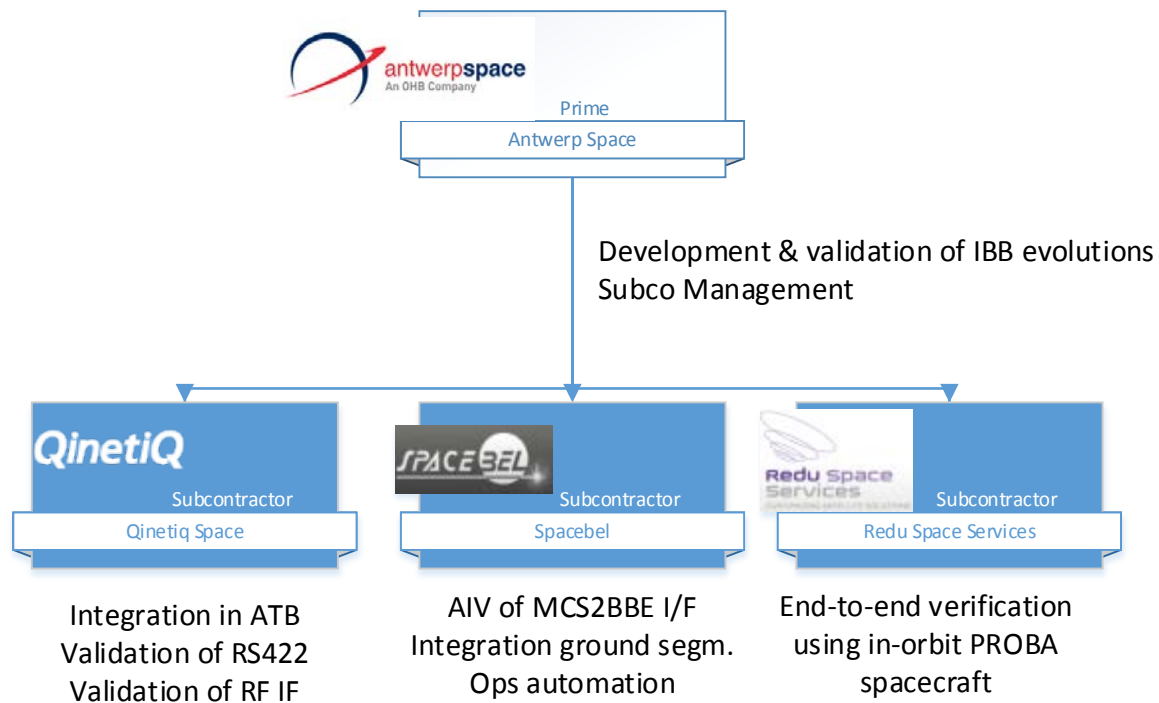


Drivers for the Project

- ▶ History of IBB (Integrated BaseBand)
 - SDR platform for TT&C (physical layer and ECSS/CCSDS stack in SW)
 - Initially designed for House Keeping Telemetry (HKTM) of telecom satellites:
 - => remnant carrier
 - => bitrates up to 64kbps
 - => Tone ranging
 - Used for LEO constellations, SCOEs, etc
 - Enhanced later on with backend protocols like SLE and EDEN
- ▶ Newer satellites require more HKTM (e.g. OBP), and smaller satellites mix payload TM with HKTM
 - ⇒ Need for higher symbol rates and other modulation types
- ▶ Operators require more flexibility in TM processing
 - ⇒ need for better TM replay
 - ⇒ Need for TM archive browsing
- ▶ Opportunity arose to validate new version with PROBA-V and PROBA-3
 - => need for MCS2BBE protocol



Project Structure



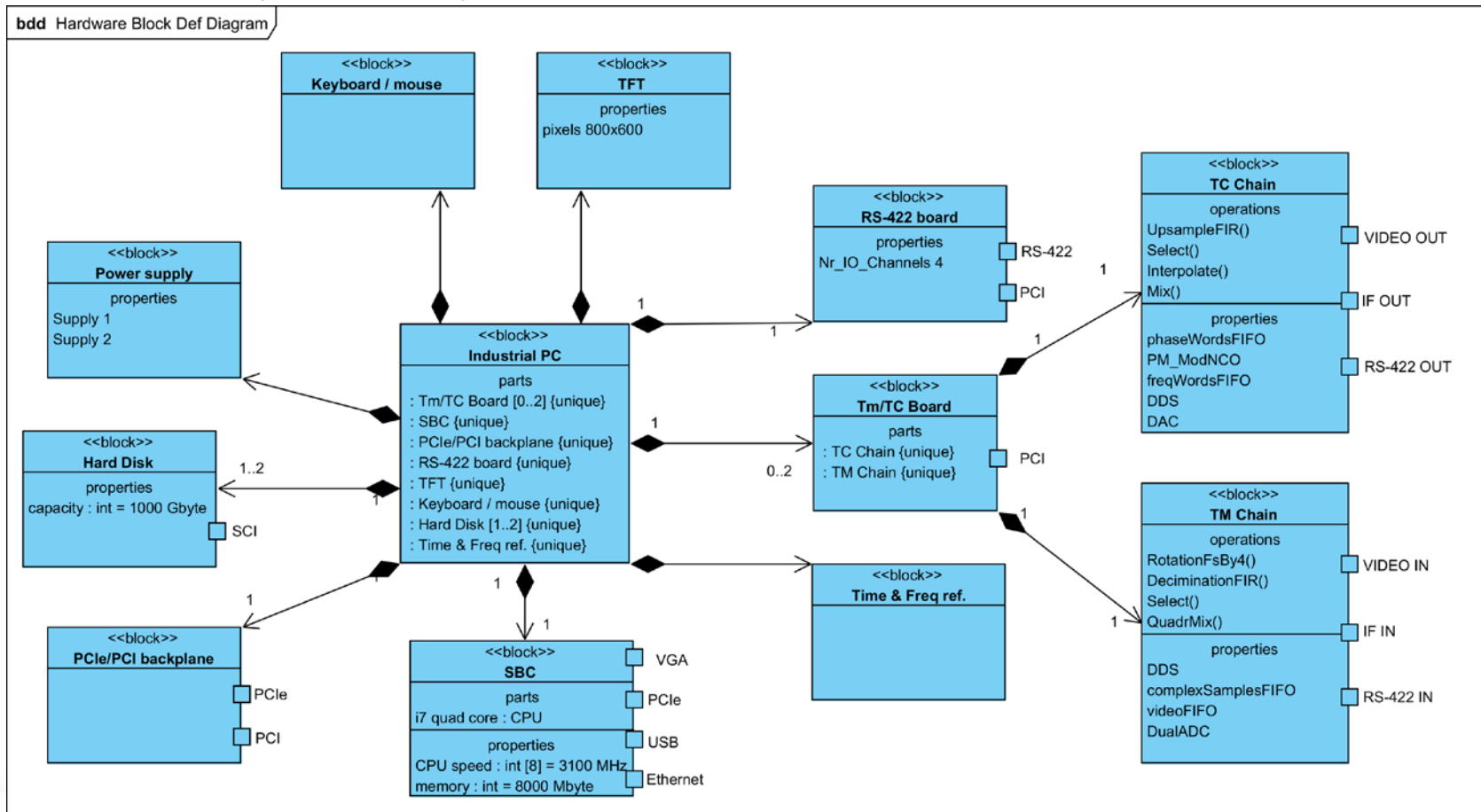
Key Technical Challenges & Achievements

▶ Integrated BaseBand (IBB) Philosophy

- Hardware minimized
 - Industrial computer platform
 - Antwerp Space sampling Board (TMTC board)
- Software maximized
 - DSP software
 - TM handling
 - TC handling
 - Monitoring and Control
 - Graphical User Interface
 - Custom software upon user demand (e.g. interfaces)
- Advantages
 - Flexibility (extra modules at minimal cost, configurability, SW switch matrix)
 - No added noise during mod / demod
- Disadvantages
 - Speed depends on CPU (is also an advantage, with increasing CPU power each year)

Key Technical Challenges & Achievements

► IBB hardware (just a computer ?)



Key Technical Challenges & Achievements

► Hardware challenges

- Previous IBB (3d generation)
 - HW developed in 2008/2009
 - Direct sampling @ 70 MHz, down sampling to 1 MHz
- Changes needed for new IBB
 - PCI or PCIe backplane
 - CPU usage => SBC quad core i7 + hyperthreading
 - Solid State hard Disks (capacity 1TB)
 - Redundant power supply
 - FPGA changes for higher resolution and BW of 4 MHz
- What didn't change
 - TMTTC boards
 - RS422 board
 - Time and Frequency board

Key Technical Challenges & Achievements

▶ Hardware benchmarks

▪ Old IBB:

- 1 Msample / s
- 16384 samples / buffer (FPGA FIFO of 32 kbyte)
- Rx 8 bit I and 8 bit Q – Tx 16 bit real : 64 kbyte per transfer per chain



New buffer is needed every 16.384 ms (1 Msample) in up and in down link
The old PC had 16 ms to handle an IRQ as it appears for 1 chain.

▪ New IBB:

- 4 Msample / s
- 16384 samples / buffer
- Rx 16 bit I and 16 bit Q – Tx 16 bit real or 8 bit I and 8 bit Q: 96 kbyte /chain
- New buffer is needed every 4.096 ms (4 Msample) in up and down link per chain



So 2 chains means only 2 ms available to handle IRQ's and mandatory calculations.

▪ Max transfer speed of data over PCI bus = 264 Mbyte/s (32 bit x 66 MHz)

- Time to transfer 32 kbyte over PCI bus > 0.12 ms
- For 2 chains and 96 kbyte this means $2 \times 3 \times 0.12 = 0.73$ ms **BEST CASE !**

▪ Average time to calculate 4096 point FFT: 110 μ s (carrier acquisition) < 2ms

Key Technical Challenges & Achievements

► Hardware benchmarks 32 Kbyte transfer

▪ Uplink throughput

- Average: 309 μ s
- Max : 346 μ s
- Min: 280 μ s

▪ Downlink throughput

- Average: 276 μ s
- Max : 311 μ s
- Min: 263 μ s

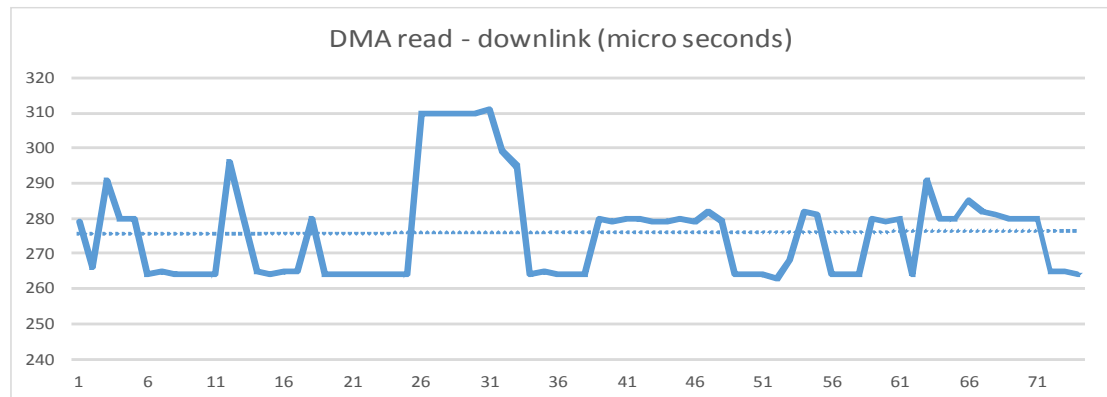
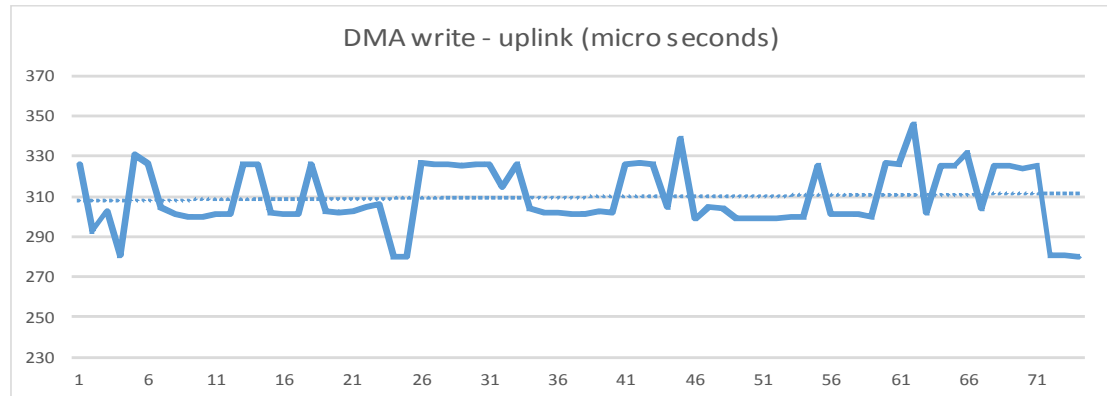
▪ Total (2 DL + 1 UL):

- Average: 861 μ s / chain
- Max: 968 μ s / chain
- Min: 806 μ s / chain

▪ Reason for delay / diff:

- PCIe – PCI bridge chips

▪ Remark: additional transfers for IRIG-B needed !



Key Technical Challenges & Achievements

► Hardware challenges (continued)

▪ Problems encountered

- EMC problems

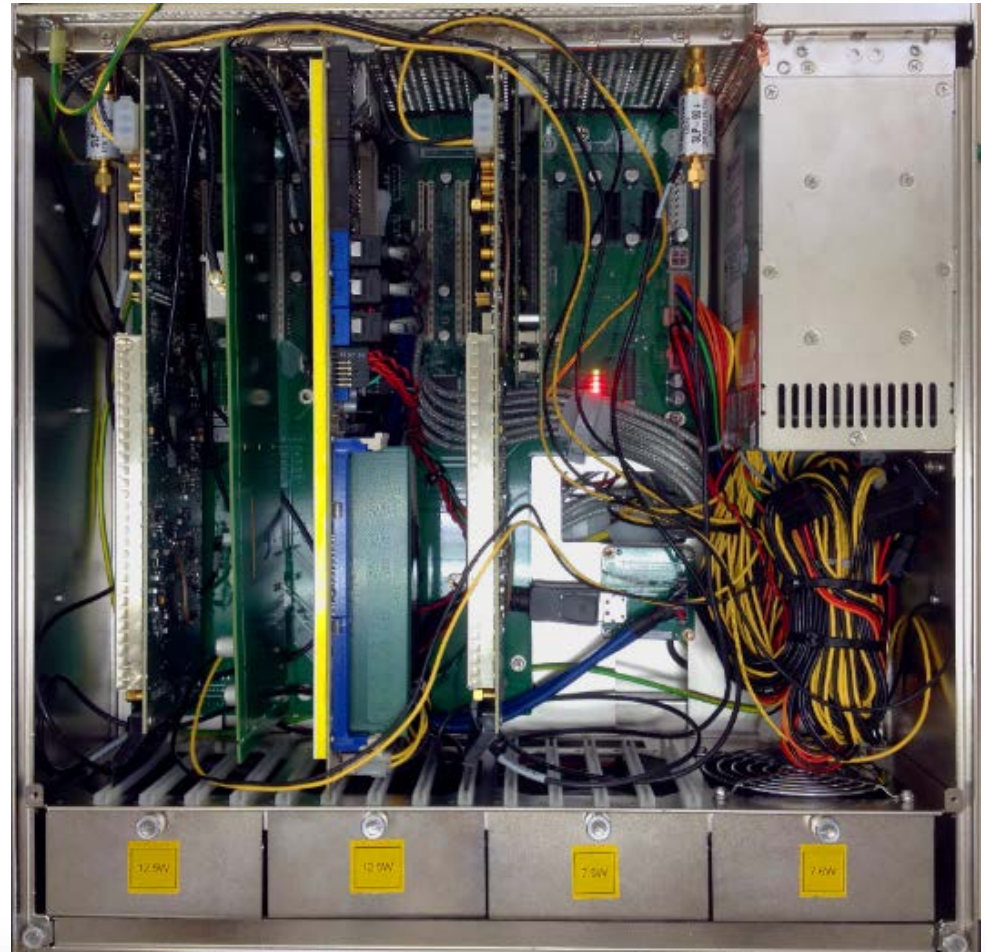


- Backplanes (PCI-PCIe bridge)

- BIOS update

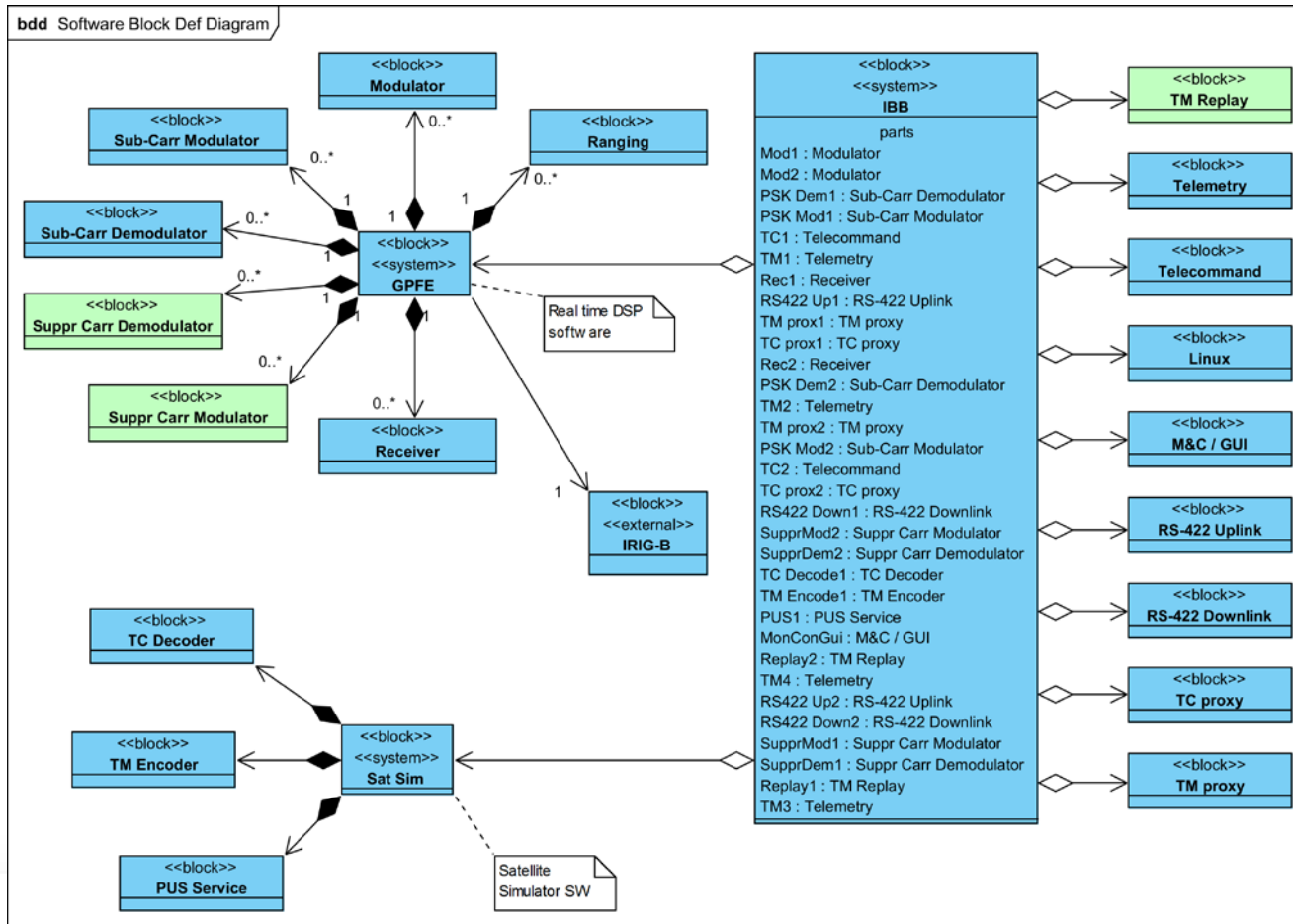


- RS-422



Key Technical Challenges & Achievements

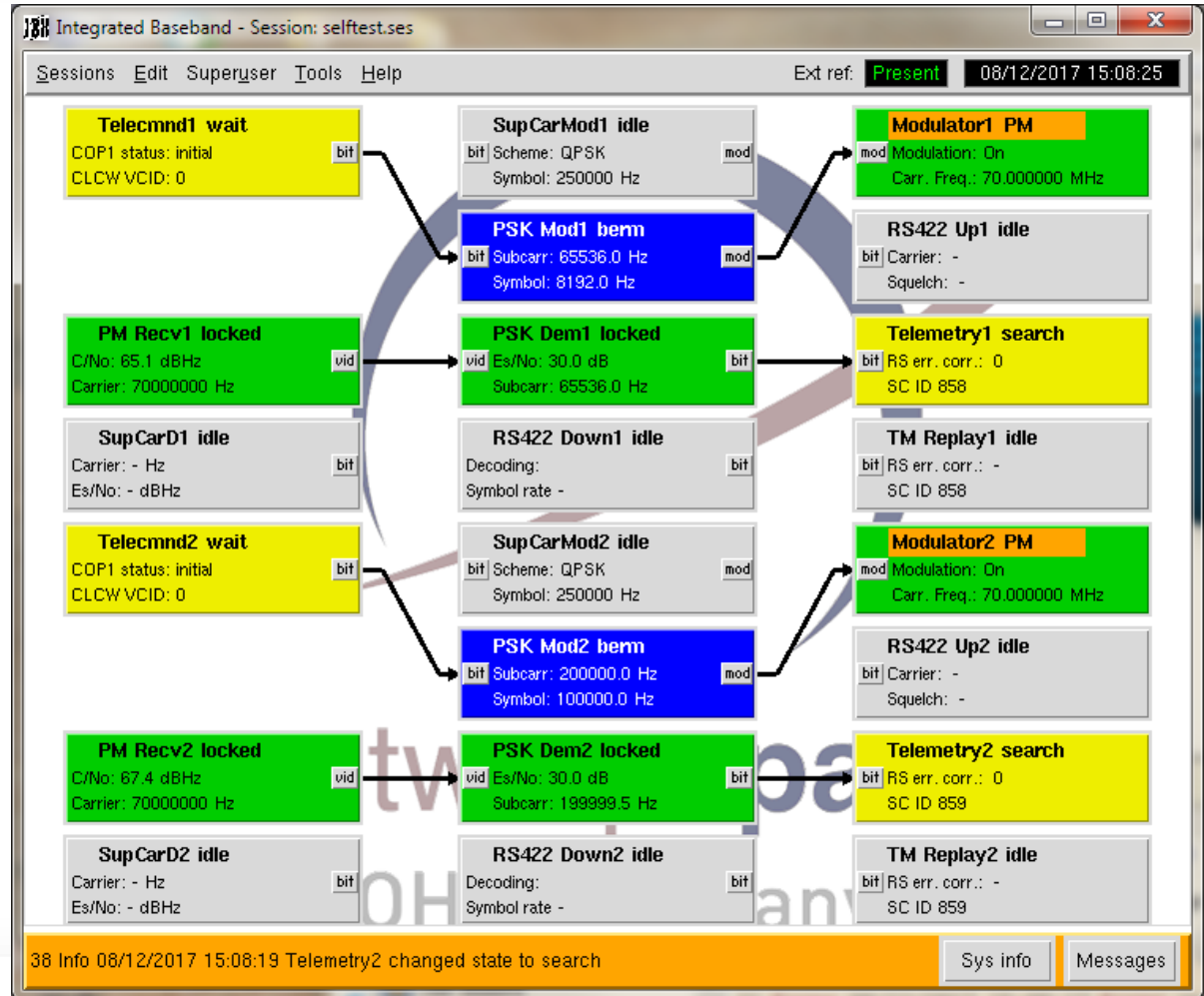
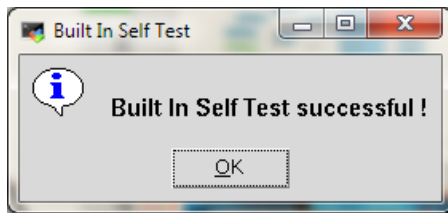
► Software challenges



Key Technical Challenges & Achievements

► IBB Software

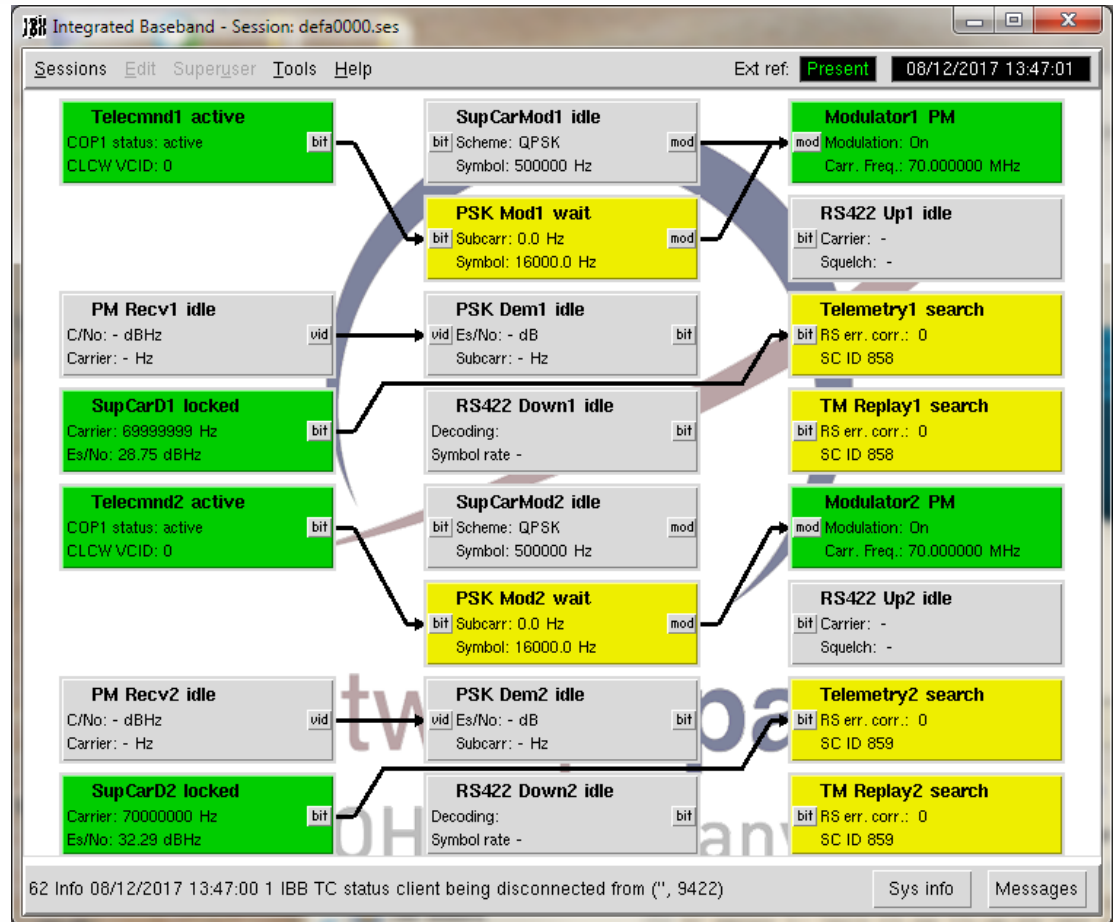
- Quick overview of the IBB User interface
- sessions, configurations, modules, connections, ...



Key Technical Challenges & Achievements

► Software challenges

- Number of modules
- QPSK/BPSK Mod/Demod
- Update TM and TC modules to ECSS standards
- MCS2BBE interface
- Archiving
- TM replay
- Memory and CPU budget
- Verification



Key Technical Challenges & Achievements

► Software challenges (continued)

▪ QPSK Modulator

- Previously phase words (real signal 16 bit)
- Now complex signal (I and Q 8 bit words)

➡ FPGA changes

- Upconverter frequency issues ...

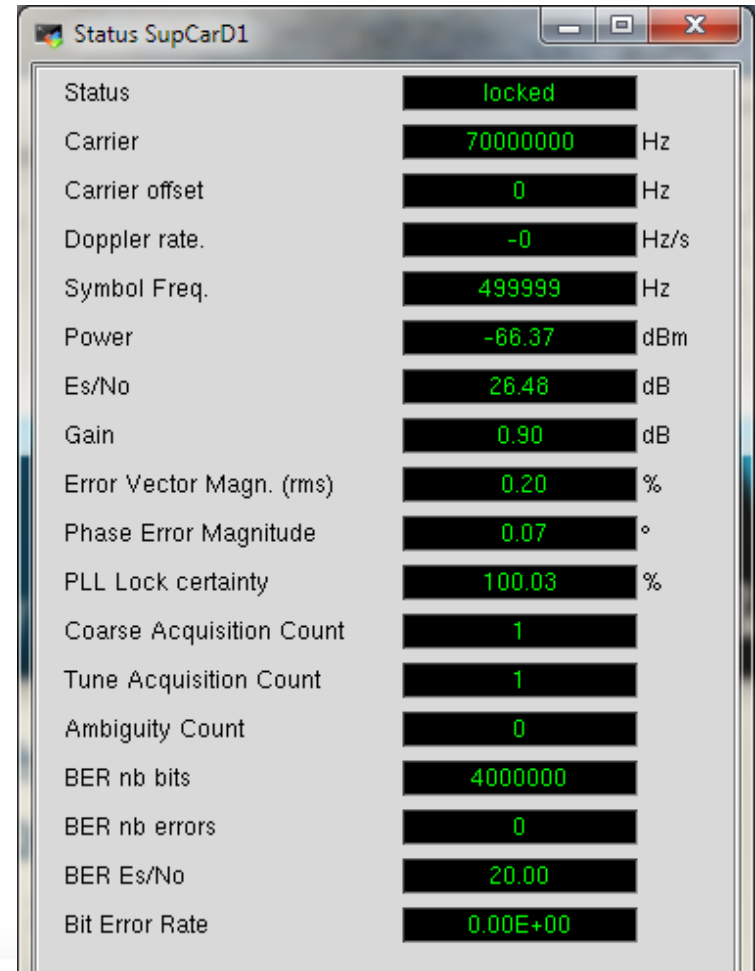
▪ QPSK Demodulator

- Previously complex signal was already used
- Resolution problems 16 bit I and Q needed

➡ FPGA changes

➡ Throughput changes (8 Msam -> 4 Msam)

▪ SRRRC filter (FIR, nb taps & roll-off cfg)



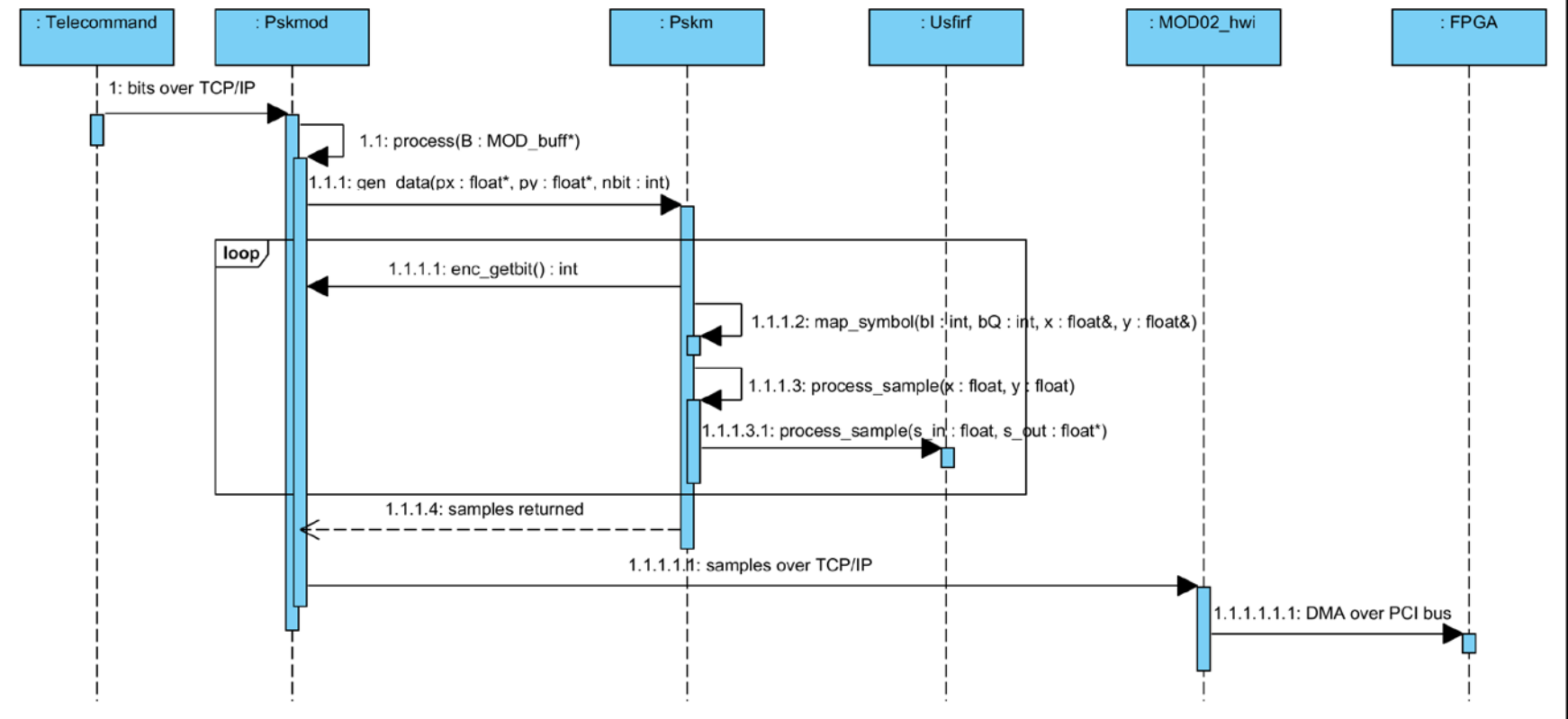
Parameter	Value	Unit
Status	locked	
Carrier	70000000	Hz
Carrier offset	0	Hz
Doppler rate.	-0	Hz/s
Symbol Freq.	499999	Hz
Power	-66.37	dBm
Es/No	26.48	dB
Gain	0.90	dB
Error Vector Magn. (rms)	0.20	%
Phase Error Magnitude	0.07	°
PLL Lock certainty	100.03	%
Coarse Acquisition Count	1	
Tune Acquisition Count	1	
Ambiguity Count	0	
BER nb bits	4000000	
BER nb errors	0	
BER Es/No	20.00	
Bit Error Rate	0.00E+00	

Key Technical Challenges & Achievements

► Software challenges (continued)

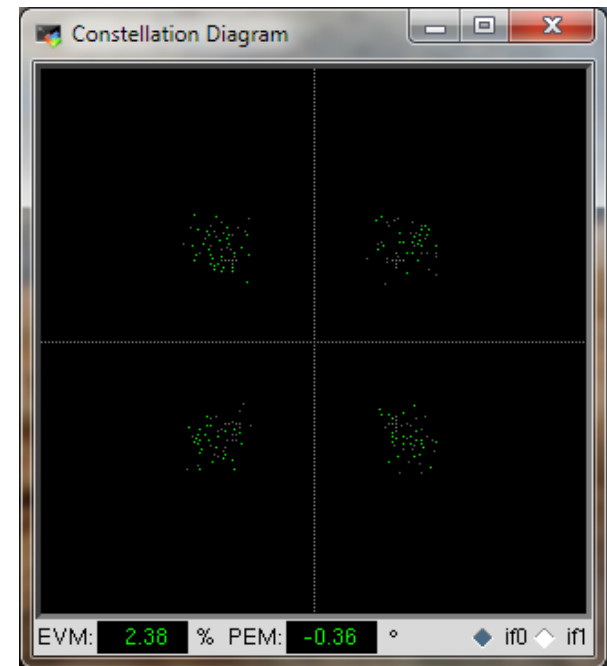
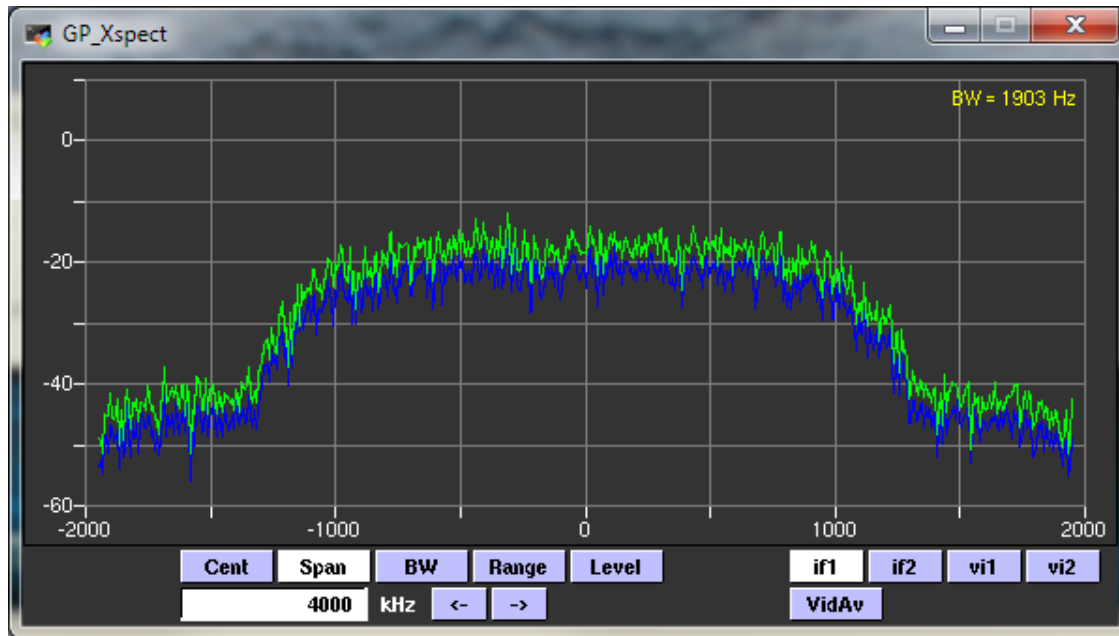
▪ QPSK Modulator context

sd Modulator data path



Key Technical Challenges & Achievements

- ▶ Software challenges (continued)
 - QPSK Demod @ 2Msym/s SRRC roll-off 0.35

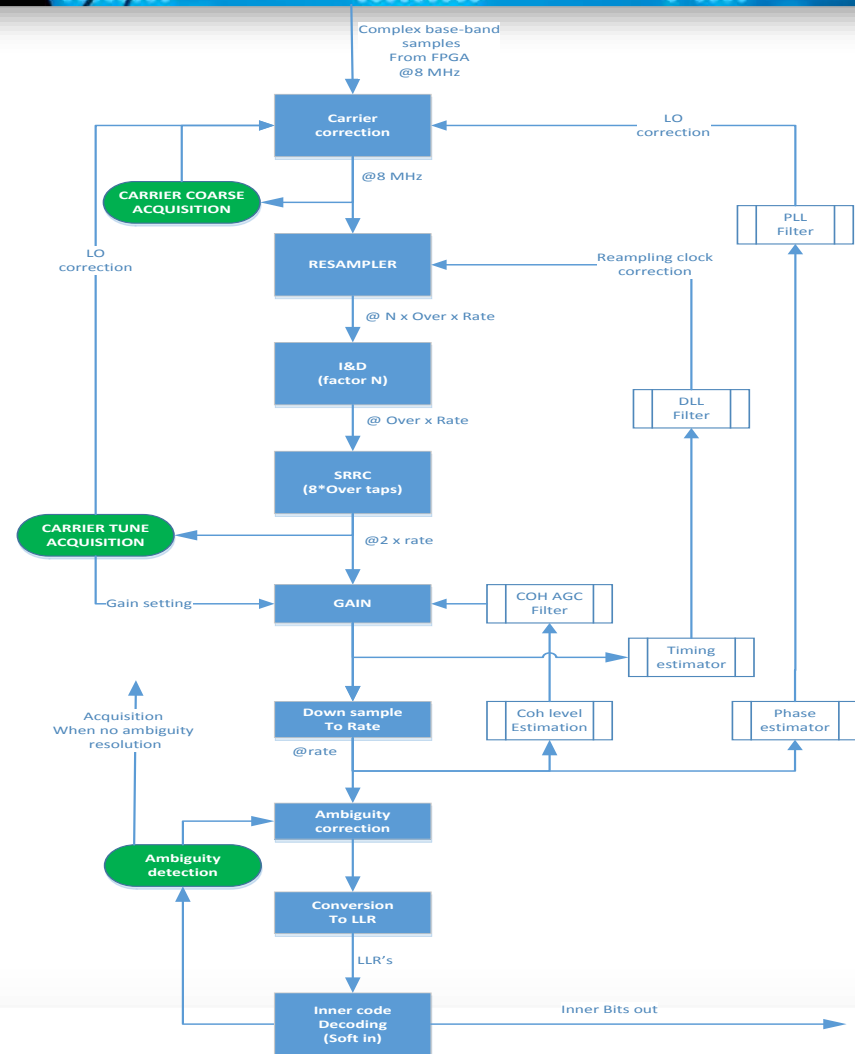


Key Technical Challenges & Achievements

► Software challenges (continued)

▪ QPSK Demod

- Design for highest possible Doppler rate (LEO)
- Acquisition decision dependent on PLL, DLL and Convolutional



Key Technical Challenges & Achievements

► Software challenges

- Update TM and TC modules to match updated ECSS standards
 - Update TC segmentation
 - Improved timestamping of TM (2 bytes => 0,015 ms resolution)
 - Time correlation (onboard – ground time)
 - Provide RS error info in real time (latency)

Key Technical Challenges & Achievements

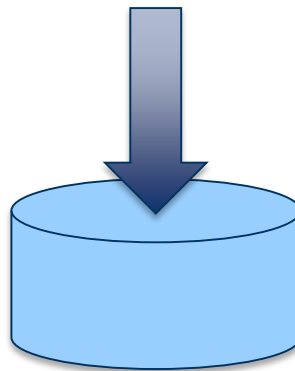
- ▶ Software challenges
 - MCS2BBE interface
 - Addition to existing SLE and EDEN interface
 - Extension of propriety CCCOM interface of IBB for M&C

Key Technical Challenges & Achievements

► Software challenges

▪ Archiving

- Format based on archiving already in use by potential customers
- Adaptation of existing archiving: frames, packets (all of 1 VC or specific ID)
- TC and TM modules (per chain)

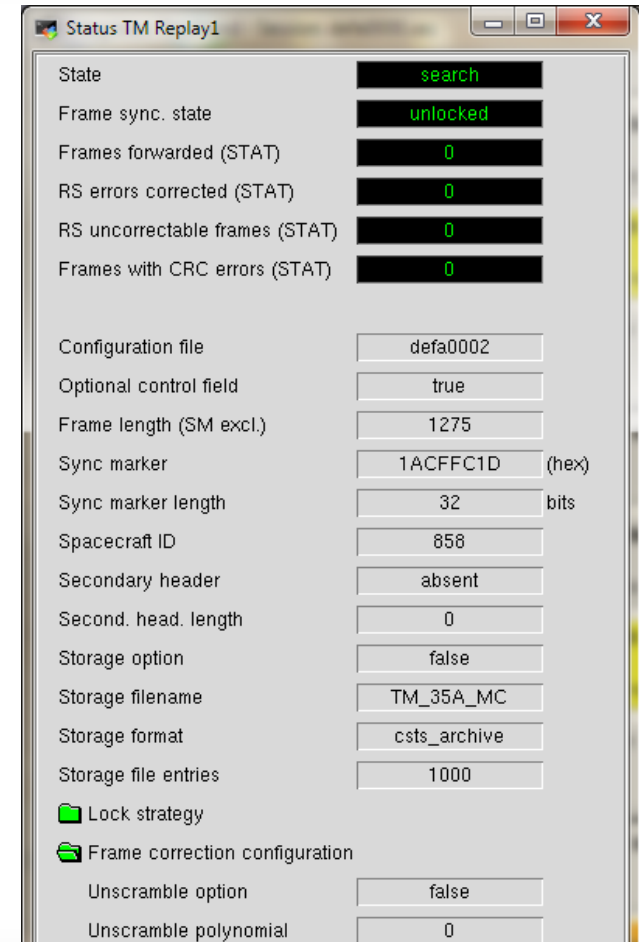


Key Technical Challenges & Achievements

► Software challenges

▪ TM replay

- Simultaneous Real time and Replayed TM
- TM replay proxy – TM archive player – TM module
- Remote start and stop, VC selection
- Usage of archived TM frames
- Generation of timestamped bit blocks
- TM handling identical to real time TM (VC, packets)



Key Technical Challenges & Achievements

- ▶ Software challenges (continued)
 - Memory and CPU budget
 - Memory is not a problem
 - CPU is a problem

Key Technical Challenges & Achievements

► Software challenges

▪ Verification

- Oscilloscope + VSA software (EVM, PEM, constellation diagram)
- Spectrum analyzer (spurious frequencies)
- Omnisat G3 Modulator + Demodulator @ > 1 Msym
- Internal Loopback:
 - Different bitrates
 - BER measurement
 - File replay + TM statistics (frame sync, VC extraction, Reed Solomon, ...)
- Satellite simulator I2B2 (with De Lande Long library) for ECSS TC and TM
- MCS2BBE automated test suite
- EGSE Router simulator (2 chains)
- Celestia Archive browser

Key Technical Challenges & Achievements

- ▶ Remaining software problem areas
 - Demod unlock problem
 - Performance convolutional decoding (Intel instruction set)
- ▶ SW solution for EM issue
 - I/Q swap detection need (QPSK implementation Proba 3 EM)

Test & Validation Campaign - General

► General Approach:



► Tests at Antwerp Space (AS):

- Unit tests of extra code
- Verification tests of complete IBB:
 - Using automated test framework of Antwerp Space
 - Emulator of MCS & EGSERouter for MCS2BBE tests
- 12 test cases, using 21 test procedures (14 automated)
- Some test procedures contain hundreds of scenario's (e.g. MCS2BBE tests)

Test & Validation Campaign - Spacebel

► Tests at Spacebel:

- Main focus was integration and verification of MCS2BBE
- 30 test cases
- Issues:
 - 3 minor, 6 major
 - All resolved (TBC by testing)
 - Main Issues encountered:
 - Minor ICD changes during project
 - TM replay issues

Test & Validation Campaign – QinetiQ Space

► Tests at QinetiQ Space:

▪ Focus:

- RS422 tests
- RF tests
- Integration in ATB of PROBA-3

▪ 36 test cases

▪ Issues:

- 36 minor, 25 major
- Only 2 issues remaining
- Major issues encountered:
 - RS-422 board throughput
 - EM module of PROBA-3 satellite (I/Q swap, wrong bitrate)

Test & Validation Campaign – Redu Space Services

- ▶ Tests at Redu Space Services (RSS):
 - Focus:
 - Validation of integration in operational environment
 - Compatibility test PROBA-V
 - 14 test cases
 - Issues:
 - 3 minor, 3 major
 - 2 issues remaining
 - Major issues encountered:
 - Loss of lock during PROBA-V pass
 - TM replay

Lessons Learned

- ▶ Foresee enough slack in the integration tests at subcontractors
- ▶ Foresee more than 1 platform for testing
 - In order to provide support to subcontractor testing
 - For non-regression testing in parallel by subcontractors
- ▶ Try to obtain (a simulator) of the external components
- ▶ Automated testing platform proved to be invaluable
- ▶ The person who estimates should do the task

Future Work

- ▶ Hardware evolution to increase the symbol rate even more
 - New modulation schemes OQPSK, 8-PSK, ...
 - New sampling HW

- ▶ Software evolutions to increase the number of simultaneous channels

Conclusion

- ▶ Main objectives of the activity:
 - Increase the bandwidth of the IBB baseband SDR platform to 2 x 2Msym/s
 - Enhance IBB with suppressed carrier modulation types (besides remnant carrier)
 - Enhance IBB with MCS2BBE protocol (besides SLE and EDEN)
 - Enhance TM/TC archive browsing and TM replay
- ▶ Main objectives have been achieved:
 - Implementation is validated
 - Demonstrated new capabilities of IBB on PROBA-V and PROBA-3 mission

Thank you !



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