GNC Implementation options: CPUs, busses, networks

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Guidance, Navigation, and Control:
need for high-performance processors

- **Guidance:** establishment of the nominal path to follow
- **Navigation:** establishment of the current position
- **Control:** actions to match the current position with the nominal path

- The various elements above have different computational requirements, among which:
  - Hard real-time for control
  - Intensive image processing for navigation
  - Complex Algorithms requiring floating-point computations
  - High-speed interfaces to receive navigation data
- Having one single solution to cope with all needs is not feasible

Outline

1. Introduction
   - Complementary Solutions High-performance processing
2. General Purpose Processor
   - high-performance, soft real-time processing (e.g. navigation/guidance)
3. Deterministic Floating-Point processor
   - hard real-time actuators control (e.g. control)
4. Digital Signal Processor
   - efficient signal processing (e.g. navigation/guidance)
5. High-speed communication infrastructure
   - Not directly addressed in this presentation

Processing Solutions Under Development
NGMP, CLP, and SSDP

Common Features:

- ✓ High-performance, multi-core architectures
- ✓ System-on-Chip designs: high integration with a wide range of functions and I/Os
- ✓ Efficient floating-point capabilities

Three complementary solutions:

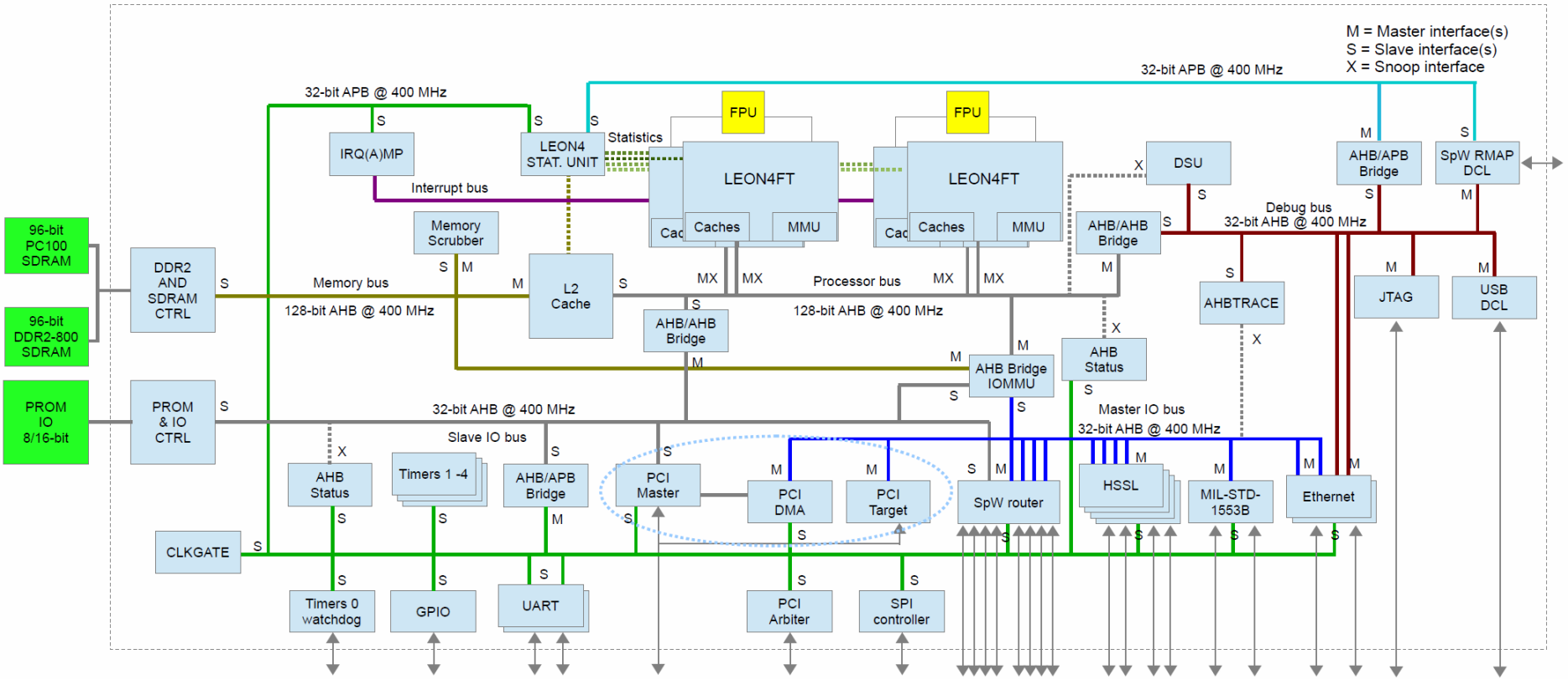
- o *CLP, Control Loop Processor*
  - Real-time highly predictable dual-core processor
  - Targeting closed-loop actuators control
- o *NGMP, Next Generation MicroProcessor*
  - General purpose quad-core processor
  - Targeting a wide range of applications, from OBC to payload processing, etc.
- o *SSDP: Scalable Sensor Data Processor*

NGMP: Next Generation MicroProcessor
Overview

- 4 LEON4FT cores with private L1 cache, 2 double precision FPUs
- Wide (128bit) shared AHB processor bus
- Shared L2 cache (baseline 512KB) and shared DDR2/SDRAM memory
- Wide array of I/Os:
  - SpaceWire router, high-speed inter-chip IF, Ethernet, 1553, etc.
- Hierarchical bus organization to reduce the interference of the I/Os on the processors

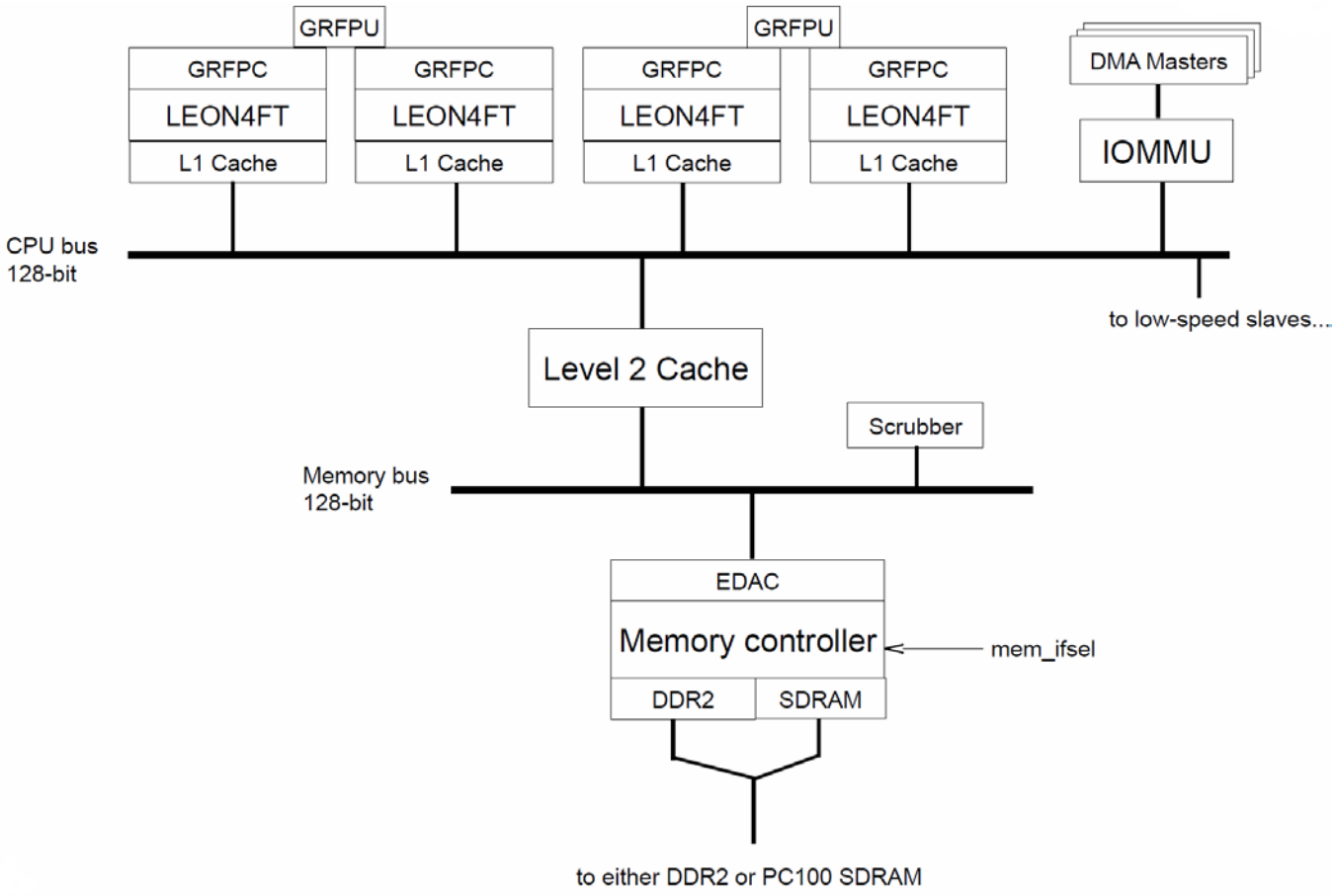
- Support for Symmetric and Asymmetric multi-processing (SMP/AMP)
- Advanced debugging infrastructure
  - Not intrusive debug support unit, performance counters and statistical unit, etc.
- Hardening against upsets in memories and (if necessary) registers
  - EDACs, HW scrubber, triplication, etc.

NGMP: Next Generation MicroProcessor



NGMP: Next Generation MicroProcessor

Details of the processing core



NGMP: Status, Future Evolutions - 1

- ✓ *3 phases planned*
  1) architectural design and functional prototypes
  2) Engineering models design, manufacturing and validation
  3) Flight models design, manufacturing and validation

- ✓ *Phase 1* almost *completed* (with Aeroflex Gaisler)
  - Prototypes on FPGA and commercial ASIC completed
    - ASIC evaluation board (NGMP running at 200MHz) available, http://gaisler.com/index.php/products/boards/gr-cpci-leon4-n2x
  - Functionally equivalent to the current status of the design
    - Specification, preliminary datasheet and performance results available at: http://microelectronics.esa.int/ngmp/
  - Target technology selection in progress
    - 65nm or smaller (28nm) required to meet the target performance (>= 400 MHz clock, large memories on-chip)
    - Technology libraries not accessible until now

NGMP: Status, Future Evolutions - 2

- ✓ *Phase 2 in preparation,* start in Q1 2014
  - Implementation of rad-hard prototypes
  - Target Deep Sub-Micron (DSM) technology, >= 400MHz expected clock frequency
  - Slight architectural modifications envisaged
    - following feedback from users of Phase 1 functional prototypes
    - Also depend on limitations of the target technology
  - Prototypes expected in 2015
  - 1 M€ TRP funding is approved, but very tight to achieve the goals

- ✓ *Phase 3 still to be planned*
  - Subject to funding
  - Depending also on the outcome of phase 2

NGMP: Use Cases

- ✓ On Board Computers, Integrated Modular Avionics (IMA) approach
  - Enabling several applications of mixed criticality on the same computer
- ✓ Payload processing
  - Generally in an SMP configuration
- ✓ Single computer for combined platform and payload processing on small (nano-) satellites
- ✓ GNC, for example processing images for navigation/automatic landing, etc.

Processing Power vs. Predictability

two requirements often conflicting

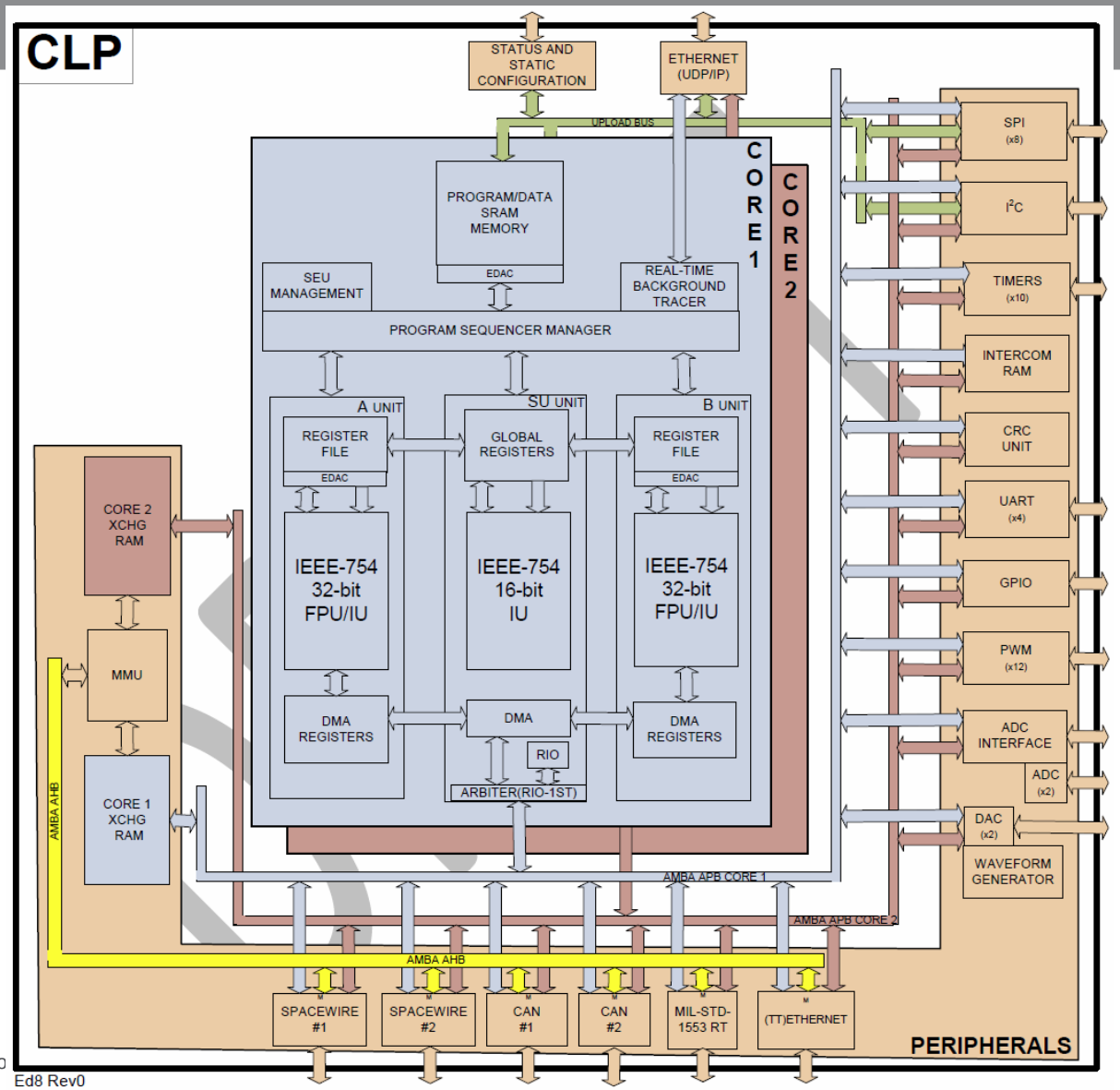
- ✓ The shared architecture of the NGMP complicates deterministic execution of the tasks running on each core
  - Interactions on shared bus, L2 cache, memory
  - Difficult to predict how each processor core will interact with the others
- ✓ Complicated usage for applications with real-time requirements
  - But fairly easy programmability
  - And high raw processing power

- ✓ Control Loop Processor: a fully predictable solution
  - Still high-performance (6 parallel execution units)
  - But more programmability effort
  - Not suitable for every workload

CLP: Control Loop Processor
Details

- Multi-core processor targeting **hard-real time floating-point intensive applications**
  - http://www.clp-space.com/
- Fully deterministic operation, no caches or interrupts
  - No OS, scheduling of tasks in a fixed periodic schedule
  - Servicing of peripheral I/O by polling
- 2 independent processor cores
  - 2 IEEE-754 32-bit floating point units and one 16-bit integer unit per core
- Wide array of I/Os:
  - 2 SpaceWire-RMAPs, (TT)Ethernet, 1553, CAN, etc.
  - Mixed-signal cores (ADCs and DACs)
  - Dedicated peripherals for mechatronic (PWM, AWG)
- Exclusive assignment of I/O peripherals to processor cores

CLP: Control Loop Processor



CLP: Control Loop Processor
Software Development Environment

- ✓ Automatic generation of CLP programs from Matlab/Simulink
  - Motor-control, closed loop algorithms are often designed in Simulink
  - Pre-defined Simulink blocks are provided
- ✓ C compiler
  - Only a subset of C will be supported
  - Processing intensive algorithms are, probably, still better optimized in assembly
- ✓ Manual partitioning of functionalities between the two cores
  - The cores are physically separated
  - No tight interactions foreseen
  - Small intercommunication RAM is the only shared element

CLP: Control Loop Processor
Status

- Target technology
  - UMC 180nm with DARE libraries
  - 50 MHz target frequency, package: QFP 256

3 Phases (development with SABCA, Belgium):

- Phase 1 funding under GSTP, PDR planned for Q4 2014
  - Currently System Requirements Review in progress

- Phase 2: Prototypes in target technology
  - Expected in 2015/2016, subject to funding availability

- Phase 3: flight model qualification

CLP: Use Cases

Hard real-time applications with a predominance of floating-point operations

- ✓ Launchers control of electromechanical actuators (Vega evolution, Ariane 6, ...)
  - *HBRISC2*, predecessor chip, is flying on Vega in the Thrust Vector Control units of the 4 stages and IXV flap control
- ✓ Levitated Reaction sphere (e.g. ELSA project) control
  - http://elsa-project.eu/
- ✓ Rover distributed motor control
  - E.g. lunar or mars rovers
- ✓ Exo-skeleton robotics applications in general

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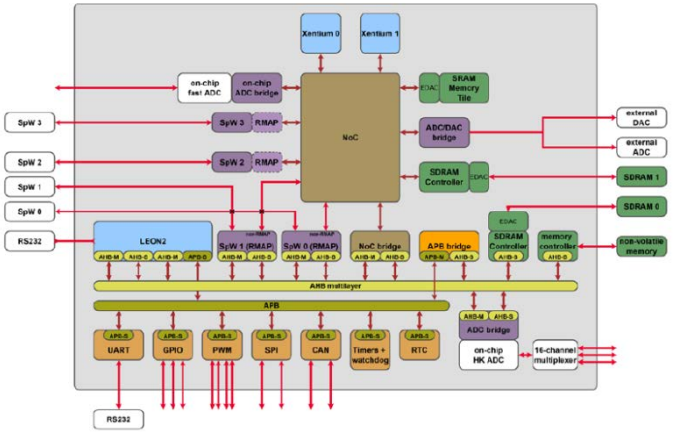
DSP-based Processing Solutions Under Development: *Scalable Sensor Data Processor - 1*

General Features:

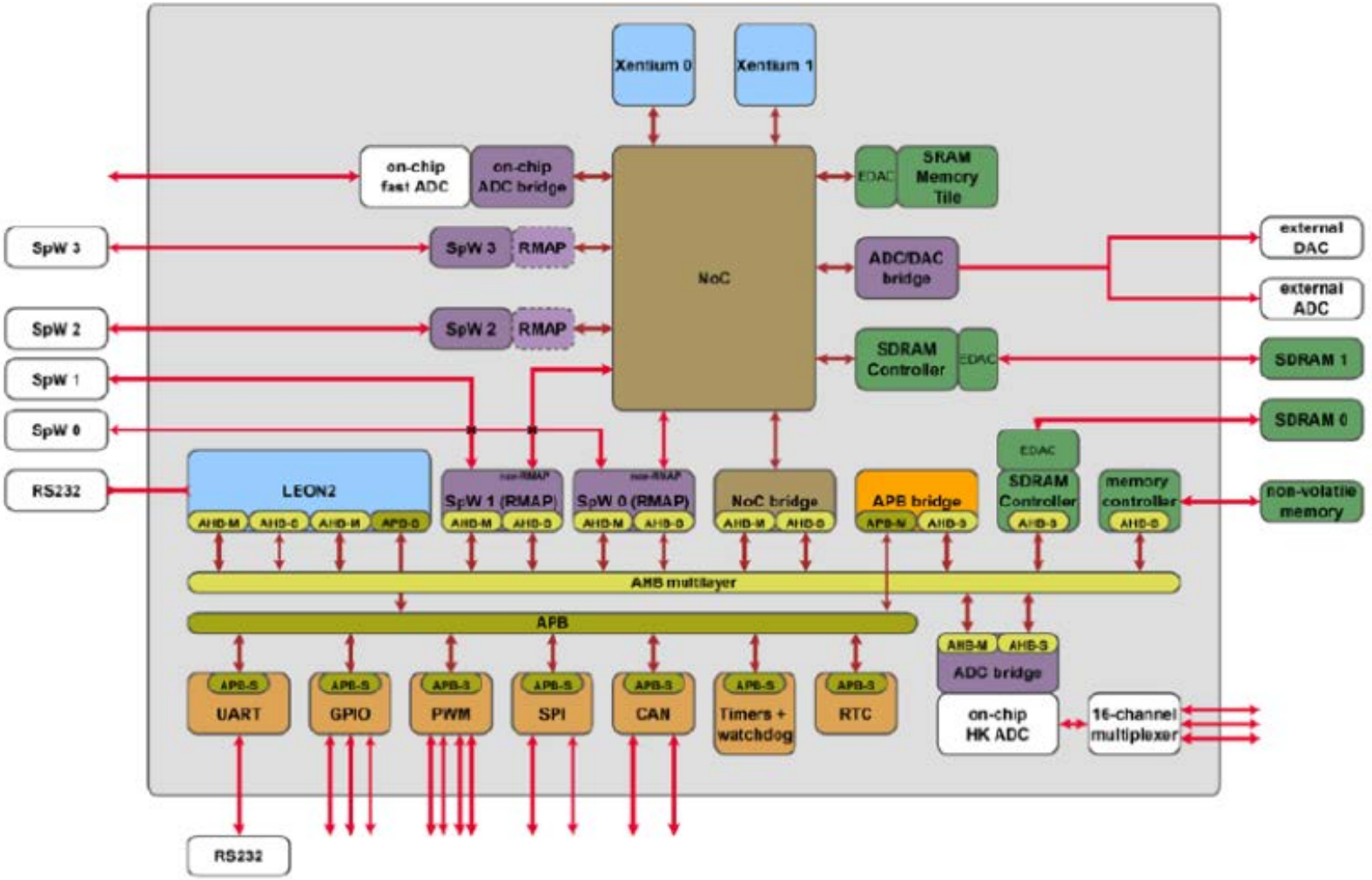
- ✓ Triple core: LEON2 + dual fixed point DSPs
- ✓ LEON FPU, Network on Chip, On-chip memory
- ✓ At 80 MHz, > 1.2 GOPs (16 bit) / 600 MOPs (32 bit) + 50 MFLOPs theor. performance
- ✓ Redundant SpW RMAP, CAN, SPI interfaces; SRAM, SDRAM, PROM



Specific Features:

- ✓ Mixed-signal ASIC based on DARE180 (1 Mrad); On-chip ADCs for sensors (16bit) and HK data acquisition (12 bit)
- ✓ Glueless interfaces to next generation image sensors (STAR3, FAINTSTAR) and popular ADC/DACs (STM1401, AD768 ..)
- ✓ Interface to VASP (TBC)

Scalable Sensor Data Processor
Architectural Details



DSP-based Processing Solutions Under Development: *Scalable Sensor Data Processor -2*

Technology development heritage:

- *RECORE Xentium® VLIW DSP IP and SDE*
- *MPPB & NGDSP tradeoff TRP studies*
- *DARE+ Application ASIC*

Expected use cases:

- ✓ JUICE and other missions, including harsh environments
- ✓ Payload data processing units and Instruments
- ✓ Platform systems (star trackers, other)

Schedule:

- o *Kickoff: October/November 2013*
- o *Prototype samples & evaluation boards expected early 2015*

Conclusions

- Future GNC systems need more processing power than currently available
- Various TEC-ED projects address the issue
  - Covering the whole spectrum of processing requirements for GNC and on-board data systems in general
- Next Generation MicroProcessor:
  - Versatile, general purpose processor
  - Complex to use in hard real-time environment
- Control Loop Processor:
  - High-performance actuators control
  - Fully deterministic
- Scalable Sensor Data Processor :
  - Efficient, programmable solution for signal processing

Thank You for Listening

For more information:

- Luca.Fossati@esa.int
- http://microelectronics.esa.int/ngmp/
- http://clp-space.com/