CAN Bus in Space: supporting developments - IP Cores

L. Fossati
ESA/ESTEC
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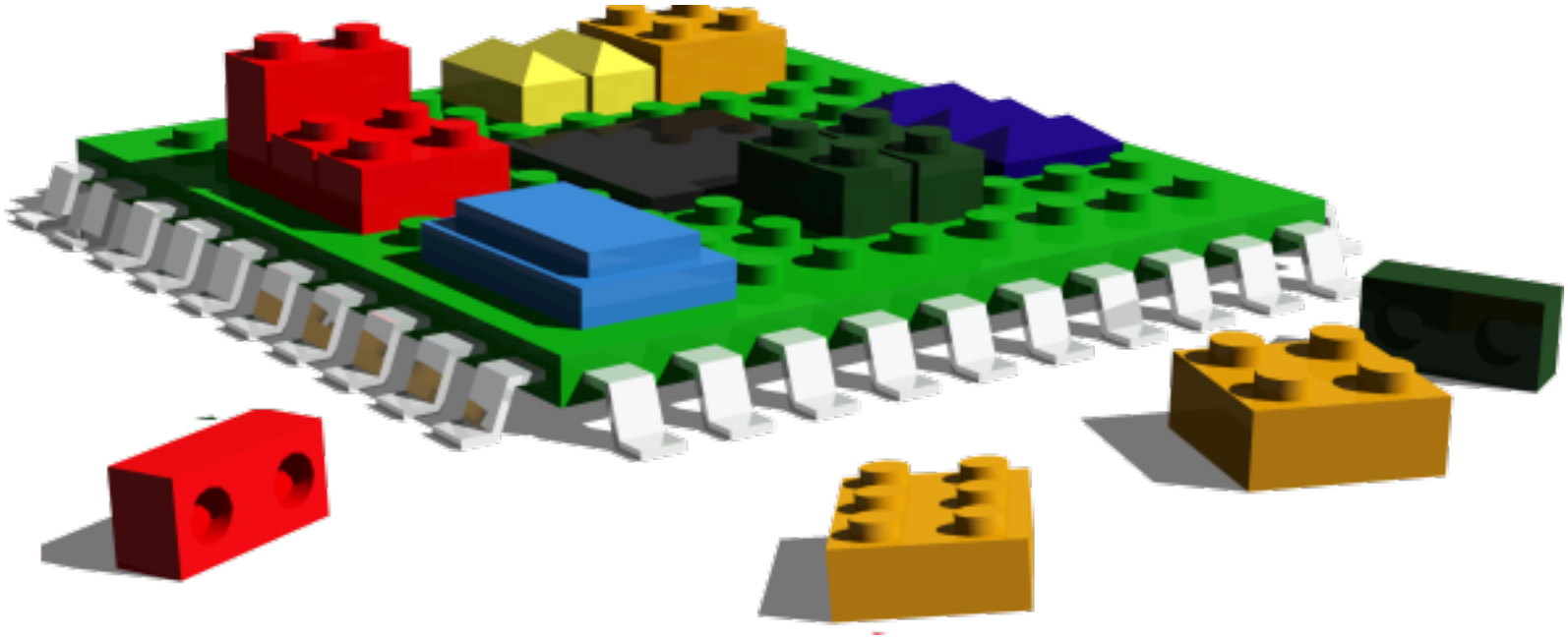
IP-Cores: *overview*

Intellectual Property Core – *definition* *from Wikipedia*:

In electronic design a semiconductor intellectual property core, IP core, or IP block is a **reusable unit of logic**, cell, or chip layout design that is the **intellectual property of one party**.



ESA IP-Cores Service
started in 2002

Roles of ESA:

- ✓ **Promote/Manage** IP-Core development and re-use
  - On-Going new IP-Core developments (TRP/GSTP/ECI …): CCSDS File Delivery Protocol, SpaceFibre, Mass-Memory Controller & File-System …
- ✓ **Licensing** to European (space) Industry
  - Processing requests, producing licenses, solving legal issues …

- ✓ **Providing Support** (in the context of ESA projects)
  - Answering technical questions, problems investigation in the Lab …
- ✓ **Centralize** IP users' **feedback**
- ✓ IP **Maintenance and Updates**
  - Following users' feedback on code bugs, documentation gaps or errors
  - Through contracts with Industry and internally (lab. activities)
- ✓ More information at: **http://tinyurl.com/ESAIPCores**

List of *digital* ESA IPs

HurriCANe	CAN Controller	ESA Member States*
CUC-CTM	CCSDS Unsegmented Code (CUC) & CCSDS Time Manager (CTM)	ESA Member States*
EDAC		ESA Member States*
RT53EUR	MIL-STD-1553B Remote Termina Controller	ESA projects only, netlist
LEON2-FT	Sparc V8 microprocessor	ESA projects only
SpaceWire-AMBA	SpaceWire-b CODEC	ESA Member States*
SpaceWire-b	SpaceWire-b CODEC	ESA projects only
SpaceWire-RMAP	SpaceWire-b CODEC + RMAP	ESA projects only
SpaceWire-RMAP SCOC3	SpaceWire-b CODEC + RMAP	ESA Member States*
AUIP	TC Authentication Unit	ESA projects only
CCIPC	CanOpen Controller	ESA projects only
PDEC	Packet Telecommand Decoder	ESA projects only
PTCD	Packet Telecommand Decoder	ESA projects only
PTME	Packet Telemetry Encoder	ESA Member States*

CAN related IP-Cores

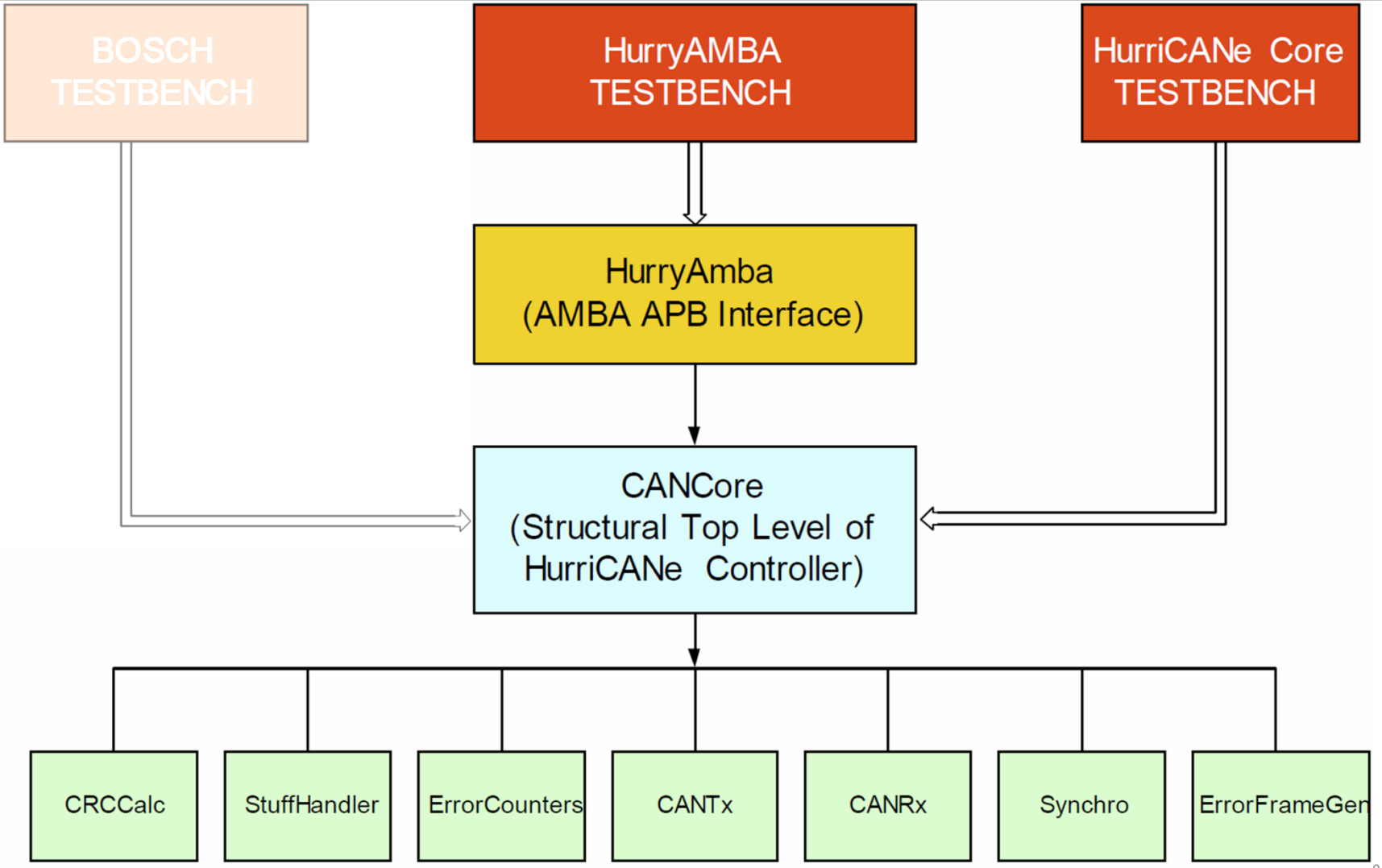
HurriCANe

- CAN bus controller compliant to the ISO 11898-1:2003 standard and the Bosch CAN Specification 2.0 parts A and B

(R)CCIPC

- CANopen Controller IP Core (CCIPC), implementing a large subset of the CANopen services as defined in the CAN in Automation (CiA) Standard "CANopen Application Layer and Communication Profile"
- Two IP-Cores available: 1) CCIPC, fully fledged, 2) RCCIPC, reduced functionality (and reduced silicon area occupation)

HurriCANe: *structure*



HurriCANe: *evolution and characteristics*

- Development started internally at ESA/ESTEC in 1999, later-on followed by evolutions implemented both by ESA and at Sitael (I)
- The IP-Core is now available to the whole Space European Industry
  - A license from Bosch for the use of the CAN Protocol is needed when used outside of ESA projects
- Currently under revision:
  - Improving timing, reset mechanisms, interface refactoring, etc.

- Fully synthesizable core, distributed with testbenches, AMBA APB interfaces, full documentation
- Validation executed against the Bosch Reference VHDL model
  - Model also available for the use in ESA projects

HurriCANe: *details*

- Adjustable SYNC_SEG, TSEG1 and TSEG2 duration
  - Bit Rate (almost) independent from the clock frequency
  - Common clock frequencies: 16, 20, 40 MHz
- Both Standard and Extended frames are supported

- Synthesis results:

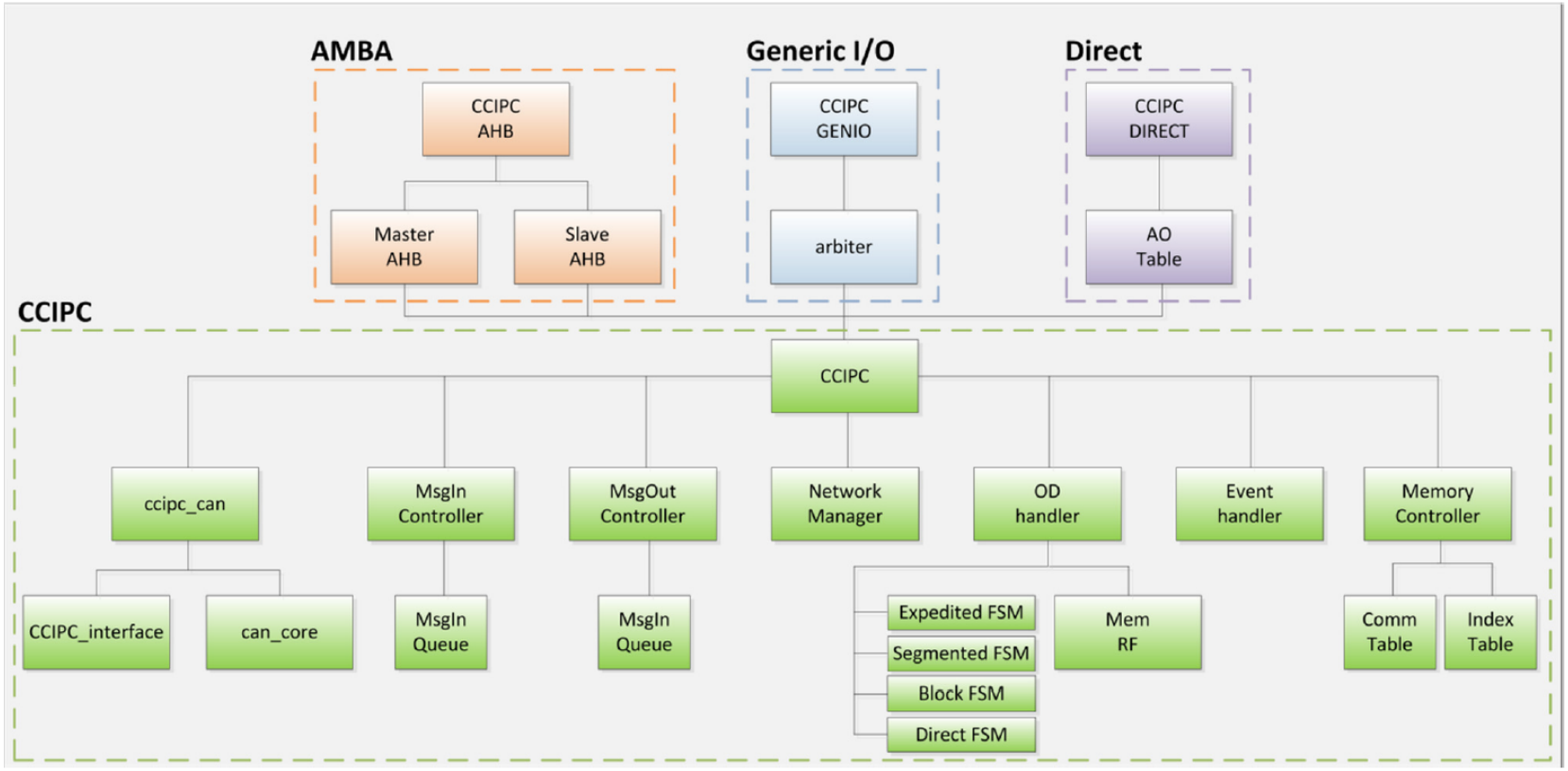
	Microsemi A54SX72A	Xilinx XC2V250FG256-6
Combinatorial – LUTs	1217 (30%)	1047 (34%)
Sequential – regs	530 (26%)	715 (23%)
Clock Buffers	2	1
Max clock frequency	10.4MHz	88MHz

HurriCANe: *usage at ESA*

Over the years the IP-Core has been integrated in various standard components and is flying/will fly in a number of ESA missions

- Components: SCOC3, MDPA, Essential Telemetry ASIC, SpW-RTC
- Missions Examples: ExoMars, Sentinel-1, BepiColombo, Galileo, Columbus, Alphasat, etc.
  - These missions either integrate the standard components above or they integrate it in ad-hoc ASIC/FPGA designs

(R)CCIPC: *structure*



Testbenches are also provided

(R)CCIPC: *evolution and characteristics*

- ✓ Development completed in 2012 in the frame of the ExoMars project by Sitael (I)
- ✓ The IP-Core is available for the use only in ESA projects
- ✓ Follow-up developments on-going

- ✓ Fully synthesizable core, distributed with testbenches, various interfaces (Direct I/O Interface, AMBA AHB, generic), full documentation
- ✓ Seamless integration with HurriCANe
  - potential interoperability with any CAN bus controller
- ✓ Full and reduced flavors of the IP-Core available, enabling to fit the smallest version on an RTAX250S FPGA
- ✓ Being used in ExoMars at the moment
- ✓ Investigations for the use in telecommunication satellites (together with HurriCANe)

(R)CCIPC : *relationship to CiA standard*

- Basic functionality: *Slave node in Network Manager Service*
- Supports the following protocols:
  - Network Management: Start/stop/reset/reset-communication, bus redundancy if heartbeat is missing
  - Boot-up
  - Service Data Object (SDO): accessing object dictionaries of remote devices
  - Process Data Object (PDO): process real-time data among nodes
  - Synchronization Object: consumer of SYNCH messages to carry out synchronous tasks

- Main differences between CCIPC and its reduced version:

	CCIPC	RCCIPC
Process Data Object (PDO)	Synchronous and Asynchronous transmit and receive	Asynchronous transmit and receive, transmit only on event trigger
Service Data Object (SDO)	Block, segmented, expedited	SDO block service only
Configurability	Full Object Dictionary configurability	Limited Object Dictionary configurability

(R)CCIPC: *performance*

RCCIPC	**Microsemi RTAX250S**	**Xilinx XC4VLX25**
Combinatorial – LUTs	2730	2250
Sequential – regs	976	924
Embedded RAMs	5	5
Max clock frequency	16.6MHz	27.7MHz

CCIPC AMBA, Block SDO	**Microsemi RTAX1000S**	**Xilinx XC4VLX25**
Combinatorial – LUTs	8182	7273
Sequential – regs	2174	1686
Clock Buffers	17	17
Max clock frequency	17.9MHz	29.8MHz

Thank You for Listening

For more information:

- Luca.Fossati@esa.int
- http://microelectronics.esa.int