Proceedings

AMICSA 2018

Analogue and Mixed Signal Integrated Circuits for Space Applications

AMICSA 2018 is sponsored by

COBHAM ARQUIMEA ICsense THE IC DESIGN COMPANY

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7th AMICSA
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Imec, Leuven, Belgium

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Overview

AMICSA stands for Analogue and Mixed-Signal Integrated Circuits for Space Applications. It is an international forum for the presentation and discussion of recent advances in analogue and mixed-signal VLSI design techniques and technologies for space applications in the domain of:

- Radiation Effects on analogue and mixed-signal ICs
- Methodologies for Radiation Hardening on analogue circuits at cell-, circuit-, and system design level
- Radiation-hardened technologies for analogue ICs
- Radiation tests of analogue and mixed-signal ICs
- Qualifying and quantifying radiation-hardness of analogue circuits
- Space Applications for analogue and mixed-Signal ICs
- Analogue intellectual property and re-usability of analogue circuits in space
- Needs and Requirements for analogue and mixed-signal ICs in future space missions
- In-orbit Experiences and flight heritage of analogue and mixed-signal Ics

Participants of AMICSA 2016 in Gothenburg, Sweden.

The 7th AMICSA is organized in collaboration with ESA, IMEC and our Sponsors, in Leuven, Belgium, June 17-20, 2018.

Organizers

IMEC

Imec offers both R&D solutions to create new technologies as well as innovation services for products and digital services.
Working with imec reduces your risk and leads to the greatest ROI in terms of time, resources, and investment. Find out more at: www.imec-int.com.

Imec R&D Solutions

Imec is the world-leading R&D and innovation hub in nanoelectronics and digital technologies. As a trusted partner for companies, startups and academia, imec brings together brilliant minds from all over the world in a creative and stimulating environment. By leveraging its world-class infrastructure and local and global ecosystem of diverse partners across a multitude of industries, imec is accelerating progress towards a connected, sustainable world.
Imec research combines its longstanding leadership in semiconductor technology with in-depth expertise in software and ICT to lay the foundation of a more personalized healthcare, smarter cities, cleaner energy and more efficient mobility, logistics and manufacturing solutions.
Imec is a single point of contact for innovators and entrepreneurs who want to explore the potential of advanced technologies.

Imec Innovation Services

Imec helps with the development of technological solutions for products and services. Imec's expertise spans throughout the entire lifecycle of the innovation process: from idea to product realization and solution validation.

Early product/solution validation

Imec offers researchers and entrepreneurs the chance to co-create and test their innovative ideas (product and/or service) thoroughly vis-a-vis their target audience and stakeholders. The involvement of the end users at an early stage of the development process makes it possible to tailor the innovation from the outset. This way one can take into account real needs, habits, attitudes and contextual factors. This gives new products and services every chance to market success..
Whether the innovations are still in a conceptual phase or whether the first building blocks are already available, imec can help you shape your product with both hardware and software services into something your future customers can start using today.

Product prototyping and Solutions

Imec offers prototype- and product engineering with a particular focus on IoT solutions and smart imaging. Imec provides access to customized solutions and services that are hard to find anywhere else; especially considering the low volumes required in the prototyping or initial ramp-up phase.

Imec's assets herein are its unique engineering skills, broad IP portfolio, 30 years expertise of R&D in semiconductor-based systems and access to a global network of partners in the entire semiconductor and system integration value chain.

Imec.IC-link

Imec.IC-link helps realize ideas in application-specific silicon (ASICs). IC-link helps with technical support, design, production (Multi-Project Wafer prototyping as well as Multi-Layer Mask or Full Mask based volume wafer production), packaging, testing, qualification and supply chain management.
To provide this service, Imec co-operates with a network of specialized subcontractors. These include leading-edge foundries for technologies ranging 0.5µm to 16nm feature sizes, IP providers, test and packaging houses etc.

Imec DARE (dare.imec-int.com)

Since the turn of the century imec IC-link has been building DARE (Design Against Radiation Effects) platforms using its radiation-hardening-by-design expertise; using layout and circuit design techniques applied to commercial foundry technology.
The DARE methodology allows for the integration of existing and custom-designed digital and analog blocks on one single chip.
The DARE offer synergizes with the other IC-link activities on ASIC design, manufacturing, packaging, testing and qualification up to Flight Model.

European Space Agency

The European Space Agency (ESA) is Europe’s gateway to space. Its mission is to shape the development of Europe’s space capability and ensure that investment in space continues to deliver benefits to the citizens of Europe and the world. ESA is an international organisation with 22 Member States. By coordinating the financial and intellectual resources of its members, it can undertake programmes and activities far beyond the scope of any single European country.

ESA’s Microelectonics section – TEC-EDM – is responsible for the microelectronics design, technology, and methodology needed by on-board control, data and signal processing systems for spacecraft platform and payloads. Responsibilities include

- using microsystems technology and techniques that permit partial or full system integration on a single chip
- establishing VLSI design methods and techniques to achieve miniaturised low-power high-speed IC design including mitigation techniques against radiation effects, ensuring good levels of testability, reusability, and reliability
- evaluating new technologies and CAD tools, assembly, and packaging techniques from an application perspective
- investigating the usage of deep submicron commercial technologies for space applications by improving radiation performance purely by design

The section provides technical support and expertise in integrated circuits design and technology for spacecraft platform and payloads and for space-related ground applications. This technical support extends to all programme directorates including Navigation and Telecommunications, Earth Observation, Science and Manned Space flight, and Microgravity.

It defines and launches internal and external activities to ensure the short, medium-, and long-term availability of key components that are qualified for use in space. Examples of suchcomponents are application-specific integrated circuits (ASICs), field programmable gate array devices (FPGAs), reusable soft building blocks (synthesisable IP cores or macro cells), multi-chip modules (MCM) and chip-sets, and other specialised and highly integrated semiconductor devices (for example, active pixel sensors).

The applications, the nature of the technology (digital, analogue, and mixed) and the functions that are of interest to the section cover a very broad range. Examples include such diverse fields as data handling and control, microprocessors and microcontrollers (for example, ERC32, LEON-based devices), for platform on-board computers and instrument control, bus nodes and routers (AMBA, PCI, 1553, CAN, and SpaceWire), CCSDS communication protocols (telecommand and telemetry), DSP for image processing, navigation and telecommunication receivers, radiation detectors front-ends, and image sensors.

Some of the section's activities also aim at ensuring the availability, accessibility, and reliability of semiconductor technology and manufacturing processes that are suitable to produce space components (EQML and MIL Silicon technologies of different geometries, Multi-Project Wafer Programmes, Assembly, Packaging and Test resources).

The Microelectronics section is heavily involved with ASIC/FPGA/System-on-Chip design methodologies, including emerging hardware-software co-design techniques.

Another significant responsibility is for preventive and mitigation techniques against radiation effects in integrated circuits. Examples of this are radiation hardened by design libraries, single-event upset (SEU) hardening at register transfer level or gate-level netlist topology, safe use of reprogrammable FPGAs in space, SEU emulation, and effects analysis.

Sponsors

ARQUIMEA (www.arquimea.com) is an engineering company with Headquarters in Madrid (Spain) and a subsidiary in Frankfurt Oder (Germany), specialized in the development and commercialization of electronic, microelectronic and electromechanical parts and systems for space and hi-rel applications, including actuators and mechanisms, sensing and monitoring systems, integrated circuits and robotic parts.
In microelectronics, ARQUIMEA is a Fabless Design House, supplier of rad-hard analog, digital and mixed-signal ICs, ASICs and IP cores in many technologies. The company also provides space FPGA coding and verification.
In mechanisms, ARQUIMEA commercializes space-qualified devices based on Shape Memory Alloys (SMA), including linear actuators, hold-down and release mechanisms (HDRMs), valves and deployment systems.
In electronics, ARQUIMEA develops readout electronic systems to implement different types of detectors, sensors and sensor networks for space and industrial applications.
ARQUIMEA relies on an intensive R&D activity to produce the most innovative products and technologies that are commercialized worldwide.
ARQUIMEA's products and technologies are fully European and ITAR/EAR free. The company is a reliable certified aerospace supplier (ISO 9100:2015, ISO 9001:2008).

Cobham Semiconductor Solutions provides HiRel standard products, ASICs, and radiation testing services. Our Cobham Gaisler site in Goteborg, Sweden provides IP cores and supporting development tools for embedded processors based on the SPARC architecture along with SpaceWire Routers and boards.

The key product is the LEON synthesizable processor model together with a full development environment and a library of IP cores (GRLIB). Our personnel have extended design experience, and have been involved in establishing European standards for ASIC and FPGA development. Cobham Gaisler has extensive experience in the management of ASIC development projects, and in the design of flight quality microelectronic devices. The company specializes in digital hardware design (ASIC/FPGA) for both commercial and aerospace applications.

Easics was founded in 1991 as a spin-off company of KU Leuven - ESAT and imec and has more than twenty five years of experience in building future-proof First Time Right embedded systems.

Easics is active in imaging / image sensors, medical / healthcare, industrial, space / aerospace, wireless & wired connectivity, broadcast and measurement equipment markets.

Easics has an impeccable track record designing Systems-on-Chip for leading product companies worldwide: OEMs (electronics, optics, mechanics), semiconductor companies and analog / mixed-signal IC design houses.

Easics has a strong focus on design and verification methodology, enabling us to deliver First Time Right designs in a world of complex constraints and changing requirements.

ICsense is Europe's premier IC design company. ICsense's core business is ASIC development and supply and custom IC design services. ICsense has the largest fab-independent European design group with world-class expertise in analog, digital, mixed-signal and high-voltage IC design. The company develops and supplies customer exclusive ASIC solutions for the automotive, aerospace, medical, industrial and consumer market compliant with ISO9001, ISO13485, IEC61508-ISO26262.

ICsense is an expert design partner for radiation-hardened ICs and developed ICs for Thales Alenia Space, RUAG Space, ESA, imec, ... In addition, ICsense provides rad hard analog IP blocks as part of imec's DARE library.

Microtest, combining innovation, continuous improvement, and sustainability, is a reliable global supplier and partner for companies seeking advanced electronic and microelectronic solutions for various applications.

After its foundation in 1998 as a test house, today the Microtest portfolio of products and services includes:

- ATE manufacturing
- Test house & test program development
- Microelectronic design house
- Application board turn-key solutions

Integrated Systems Development S.A. (ISD) is an independent Greek SME
active in the domain of Integrated Systems of guaranteed quality and performance. ISD acts as an original electronic equipment developer and integrator, providing services ranging from software development for embedded and general purpose platforms, to digital and analog/RF integrated circuit design, memory design, to digital signal processing for embedded/stand-alone applications and PCB design. ISD is a turn-key
solution provider handling all aspects of product definition, design, development, documentation, production and support.

ISD's key space activities include:

- Design, development and validation of hardened ASICs (ADC, DAC, clock generator, systolic array processor, etc.).
- Design, development and validation of hardened IPs (DDR2/3 PHY for the ST 65nm CMOS platform, parts of a high speed serializer, etc.).
- PCBs for space applications, evaluation kits and test campaigns (hardened RF module driving a laser for data com, evaluation kits for the 8032-based µC, the space-fiber demonstrator and the AGGA4 processor, etc.).
- Hardening strategy definition and demonstration of hardened systems using SRAM FPGAs
- Space software validation (part of the Exomars Rover software, etc).
- AIV activities providing system level, electrical and mechanical integration and testing as well as QC support services for missions such as Solar Orbiter, Euclid, etc.

SERMA GROUP offers a wide range of services related to electronics. Physical analyses, electrical test, environmental qualification, reliability study, microelectronics assembly, thick films screen printing, ASIC & FPGA design and validation. SERMA GROUP provides various services to the space industry (agencies, primes, OEM, EEE parts manufacturers) to help them manufacture and use hi-reliability electronics systems that withstand harsh environments.

Exhibitors

1 Microchip

Microchip's Continued Commitment to the Aerospace and Defense Industry

Microchip uses the latest innovative commercial technologies such as 8-bit AVR® MCUs, Arm® and dsPIC®-based MCUs, adapting these to rad-hard, rad-tolerant and high-reliability application requirements in order to provide proven solutions, volumes and long-term reliability. With more than 20,000 flight models per year delivered in a wide range of aerospace and defense applications (space, avionics, military and harsh environments), our offering affords extended temperature, radiation tolerant or hardened devices issued from our widely deployed Microchip products portfolio to reduce your costs, to boost your time to market and to improve performances of your critical system.

Microchip offers long term supply commitment, full traceability, the most demanding qualification flows, and a rich ecosystem: reference hardware, software environment and transversal system solutions with a dedicated support team for Aerospace and Defense.

Within the aerospace and defense portfolio, Microchip is proud to include the entire Atmel rad-hard product line: Rad Hard ASICS.

2 Alter Technology

ALTER TECHNOLOGY is a global provider of electronic components and related services and solutions to the high tech industry, with special focus on high reliability.

Our services ranges from the procurement of the right product at the right price, to a wide variety of testing services and package design and assembly. On top of that our group provides also engineering support and testing services (EMC, environmental, mechanical, vibration) of special industrial equipment.

We have worked and currently work in a large number of space missions developed world wide as well as in other huge number of international technological projects.

3 - 4 Cobham

Cobham Semiconductor Solutions provides HiRel standard products, ASICs, and radiation testing services. Our Cobham Gaisler site in Goteborg, Sweden provides IP cores and supporting development tools for embedded processors based on the SPARC architecture along with SpaceWire Routers and boards.

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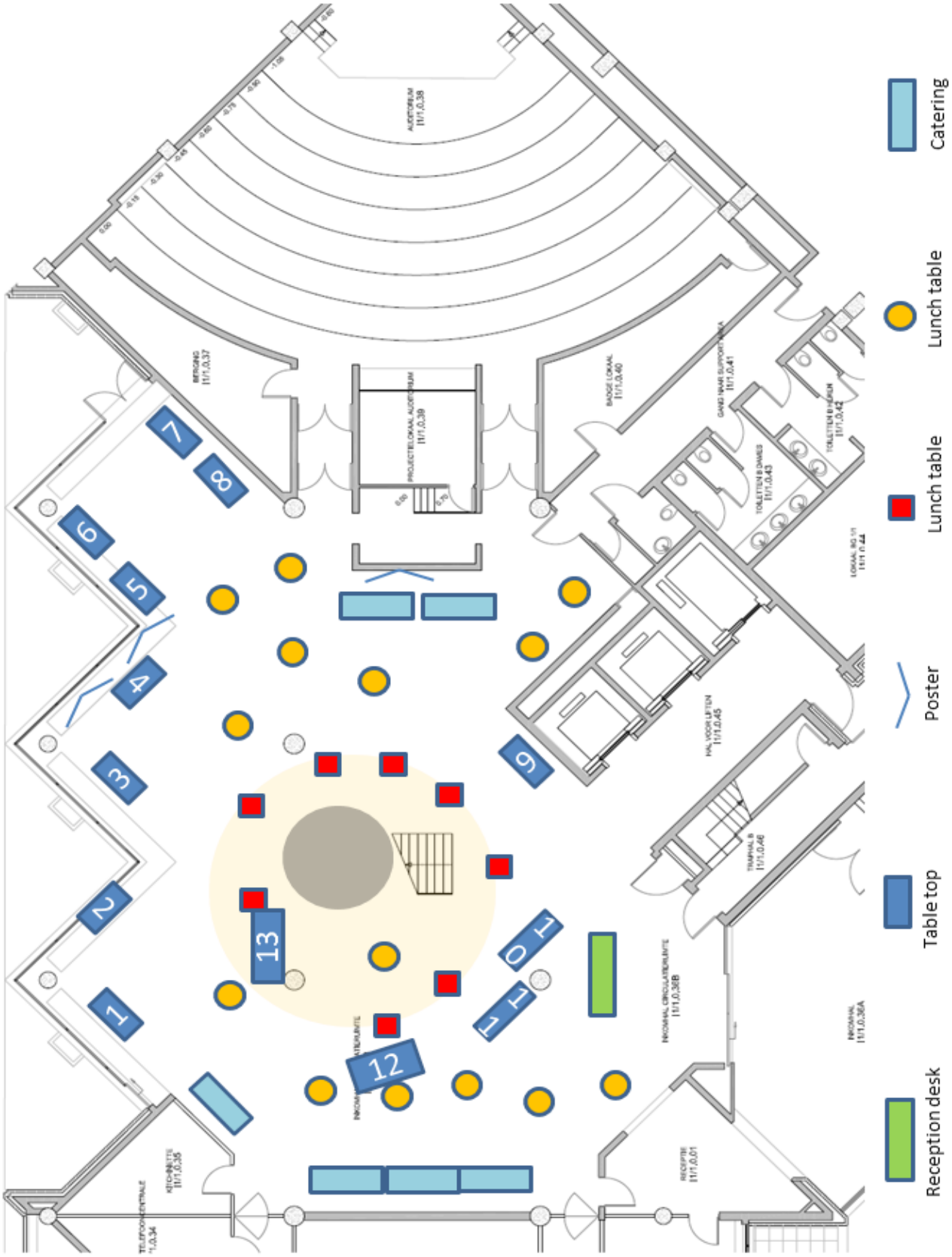

Exhibition floor plan. Stand numbers correspond to the company numbering. 14, 15 and 16 are located in the lounge, 1st floor.

5 Microsemi

Microsemi Corporation, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

6 Micross

Micross Components, a single-source global supplier of advanced high-reliability electronics, manufactures and distributes a wide range of products including discrete bare die and wafers, standard and custom packaged devices and passive components. Our value-added capabilities include a comprehensive list of services spanning assembly, environmental & electrical test, and mechanical component modifications.

For over 35 years, Micross has provided the design, manufacturing and logistics expertise needed to support the Hi-Rel, Military and Aerospace market throughout the program life cycle. These products span a broad range of different types of electronic components and many types of packages. Micross space sector capabilities support assembly & test for the complete range of semiconductor technologies to space flight model grade.

7 Arquimea

ARQUIMEA (www.arquimea.com) is an engineering company with Headquarters in Madrid (Spain) and a subsidiary in Frankfurt Oder (Germany), specialized in the development and commercialization of electronic, microelectronic and electromechanical parts and systems for space and hi-rel applications, including actuators and mechanisms, sensing and monitoring systems, integrated circuits and robotic parts.

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- ARQUIMEA relies on an intensive R&D activity to produce the most innovative products and technologies that are commercialized worldwide.
- ARQUIMEA’s products and technologies are fully European and ITAR/EAR free. The company is a reliable certified aerospace supplier (ISO 9100:2015, ISO 9001:2008).

8 Magics

MAGICS Instruments NV (MAGICS®) is a fabless IC development company based in Belgium, specialized in the design of integrated circuits and system on chip solutions for intelligent sensing and control in harsh environments.

MAGICS has developed a unique rad-hard IC design environment to achieve high first-time-right rate and high reliability for space and nuclear applications:

- Industrial standard EDA tools: MATLAB for system behavioral model simulation; Cadence Virtuoso design tools for schematic edit, simulation and layout; Cadence Incisive and Innovus for digital design and implementation; Mentor Graphics Calibre for physical verification and sign-off.
- Experimentally verified transistor radiation model for TID (total-ionizing-dose) simulation.
- In-house proprietary TMR (triple modular redundancy) generator and SET simulator for single-event simulation.
- A wide range of qualified rad-hard analog/mixed-signal IP blocks (e.g., PGA, ADC, PLL, Clock reference, Bandgap, LDO, Temperature sensor, etc.).

MAGICS provides one-stop shop for custom rad-hard IC design, and helps customers to create system-on-chip solutions for their PCB systems. An SoC integrates an electronics system into one single chip, and require few external components, hence significantly reduces the cost and complexity of system-level integration. SoCs also consume less power, have smaller size, and provide greater reliability than their PCB counterparts.

From 2008 to 2017, MAGICS has successfully delivered several radiation-hardened integrated circuits development projects, including: picosecond time-to-digital converter for a pulsed-mode time-of-flight Light Detection and Ranging (LiDAR) system; MGy radiation tolerant sensor instrumentation link for nuclear environments; closed-loop motor control electronics for intelligent remote handling at ITER.

For more information please visit www.magics.tech/services.

9 Teledyne

Teledyne provides enabling technologies for industrial growth markets. We have evolved from a company that was primarily focused on aerospace and defense to one that serves multiple markets that require advanced technology and high reliability. These markets include deepwater oil and gas exploration and production, oceanographic research, air and water quality environmental monitoring, factory automation and medical imaging.

Our Aerospace and Defense Electronics segment provides sophisticated electronic components and subsystems and communications products, including defense electronics, data acquisition and communications equipment for air transport and business aircraft, harsh environment interconnects, and components and subsystems for wireless and satellite communications, as well as general aviation batteries.

10 Serma/HCM.Systrel

SERMA GROUP offers a wide range of services related to electronics. Physical analyses, electrical test, environmental qualification, reliability study, microelectronics assembly, thick films screen printing, ASIC & FPGA design and validation. SERMA GROUP provides various services to the space industry (agencies, primes, OEM, EEE parts manufacturers) to help them manufacture and use hi-reliability electronics systems that withstand harsh environments.

11 Thales Alenia Space Belgium

Thales Alenia Space in Belgium is a subsidiary of Thales Alenia Space, the European leader in satellite systems and a major player in orbital infrastructures.

Thales Alenia Space in Belgium is a world leader in Power Conditioning and Distribution for satellites. Our product range covers the needs of spacecraft electronics from micro satellites up to large geo-satcom.

The company also enjoys a position at the forefront of several flight electronics products : flexible microwave power amplifiers with travelling wave tubes power supplies for plasma propulsion thrusters, motor drive electronics, DC/DC converters,… The company is building a new facility dedicated to the production of photovoltaic assemblies (PVA). This facility will feature innovative technologies, making it the showcase for Thales Alenia Space’s Industry 4.0 approach to manufacturing.

Thales Alenia Space in Belgium is the main supplier of on-board electronics for Ariane 5. The company is also the European leader for the Checkout Systems and Control Benches for launchers. We are prime contractor (and manufacturer) for the Safeguard System dedicated to Soyuz (French Guyana) and to Ariane 6.

To support innovation in equipments, Thales Alenia Space in Belgium is also very active in microelectronics, with the Digital Programmable Controller(DPC) as the flagship

12 Microtest

Microtest, combining innovation, continuous improvement, and sustainability, is a reliable global supplier and partner for companies seeking advanced electronic and microelectronic solutions for various applications.

After its foundation in 1998 as a test house, today the Microtest portfolio of products and services includes:

- ATE manufacturing
- Test house & test program development
- Microelectronic design house
- Application board turn-key solutions

13 Renesas

Renesas Electronics Corporation delivers trusted embedded design innovation with complete semiconductor solutions that enable billions of connected, intelligent devices to enhance the way people work and live—securely and safely. A global leader in microcontrollers, analog, power and SoC products and integrated platforms, Renesas provides the expertise, quality, and comprehensive solutions for a broad range of Automotive, Industrial, Home Electronics, Office Automation and Information Communication Technology applications to help shape a limitless future. Learn more at renesas.com.

14 IHP – Innovations for High Performance Microelectronics

The IHP, an institute of the Leibniz Association performs research and development in the fields of silicon-based systems, highest-frequency integrated circuits, and technologies for wireless and broadband communication. The focus of research at the institute is oriented towards issues relevant for business, resulting in applications for telecommunications, semiconductor and automotive industries, aerospace, telemedicine, and automation technologies. The institute has developed into an internationally recognized competence center for silicon-germanium technologies.

The strength of the IHP is evident in the scientific contributions to leading conferences around the world, by continuous success in attaining thirdparty funds and the steadily increasing number of international users of the Multi-Project Wafer and Prototyping Services. Along with the IHP staff's exceptional competence, the cutting-edge modern technological equipment plays an important role in this success.

The IHP provides an important bridge between academia and industry. The Joint Labs with universities and universities of applied science in the Berlin-Brandenburg region have been particularly successful in this cooperation.

15 TRAD

For more than 24 years, TRAD Tests & Radiations has been recognized for its unique expertise on radiation effects. On a daily basis, TRAD assists companies wishing to better predict and minimize radiation effects on their products. TRAD offers a complete range of services and products allowing to meet all requirements of the radiation process or applicable norms:

- Assistance in radiation effect analysis; part list evaluation, TID & TNID calculation, shielding optimization, SEE analysis, environment definition
- A wide range of industry-specific software developed by TRAD: FASTRAD® & OMERE (Space), RayXpert® (Nuclear & Medical)
- Electronic components radiation testing, materials characterization, procurement and component expertise (EEE)
- Test bench development for TID and SEE on complex integrated circuits, memories, ASICs, FPGAs, etc.
- Technical assistance to radiations, facilities rental incl. Co60 and Vacuum Electron irradiation facilities - On-site training course for dose calculation, radiation space environment, radiation effects, FASTRAD®, etc.

TRAD heavily invests in its 800m² state-of-the-art facilities in Toulouse, with new equipments every year and a cobalt-60 source. The team of PhDs, engineers and technicians is dedicated to meet the client’s high expectations; TRAD takes pride in hiring and retaining the most qualified staff in electronics, physics and IT.

TRAD is proud to assist major companies and agencies worldwide such as Airbus Defence & Space, ESA, JPL, TESAT Spacecom, Thales Alenia Space, MIT, etc

16 Imec

Imec is the world-leading research and innovation hub in nanoelectronics and digital technologies. The combination of our widely acclaimed leadership in microchip technology and profound software and ICT expertise is what makes us unique. By leveraging our world-class infrastructure and local and global ecosystem of partners across a multitude of industries, we create groundbreaking innovation in application domains such as healthcare, smart cities and mobility, logistics and manufacturing, and energy. As a trusted partner for companies, start-ups and universities we bring together close to 3,500 brilliant minds from over 70 nationalities. Imec is headquartered in Leuven, Belgium and also has distributed R&D groups at a number of Flemish universities, in the Netherlands, Taiwan, USA, China, and offices in India and Japan. In 2017, imec's revenue (P&L) totaled 630 million euro.

Imec also supports radiation-hardened by design using layout and circuit design techniques applied to commercial foundry technology. The DARE (Design Against Radiation Effects) methodology and flow allow for the integration of existing and custom-designed digital and analog blocks on one single chip, as well as for all the necessary steps to deliver flight models; manufactured in the technology and assembled in the package best fit for your application.

Reviewers

- Laurent Berti
  (Imec)
- Franco Bigongiari
  (Sitael S.p.A.)
- Steven Redant
  (Imec)
- Volker Lück
  (Tesat)
- Geert Thys
  (Imec)
- Richard Jansen
  (ESA)
- Boris Glass
  (ESA)
- David Dangla
  (CNES)
- David Levacq
  (ESA)

Session Chairs

Radiation Effects on analogue and mixed-signal ICs

- Dr. Sebastian Millner
  (Tesat-Spacecom)

Custom Cell-, Circuit-, and System Design

- Marc Fossion
  (Thales Alenia Space Belgium)
- Michael Kakoulin
  (IMEC)
- Florence Malou
  (CNES)

Evaluation and Qualification

- Dieter Herrmann
  (DLR)

Space Applications

- Jose F. Moreno-Alvarez
  (Airbus Defence and Space)
- Jörg Ackermann
  (Integrated Detector Electronics AS)

Radiation Hardened Technologies

- Dr. Constantin Papadas
  (ISD SA)
- Franco Bigongiari
  (Sitael S.p.A.)
- Frank Henkel
  (IMST)

Poster Session

- David Levacq
  (ESA)

Program

Sunday, 17 June 2018

20:00	Welcome Drink	*Café Entrepot*

Monday, 18 June 2018

09:15	Welcome and Introduction	Steven Redant (Imec) Boris Glass (ESA)
09:45	**Radiation Effects on analogue and mixed-signal Ics** Convener: Dr. Sebastian Millner	
	Single Event Effects Analysis in ReadOut Integrated Circuits at Cryogenic Temperatures	Laurent Artola (ONERA)
	Static Linearity Test for Radiation Effects Characterization of an 18-bit SAR Serial IO COTS ADC: Analog Devices AD7982	Dr. Sonia Vargas-Sierra (Alter Technology)
	Validation of a High Resolution ADC for Space Applications	Kostas MAKRIS (ISD S.A)
11:00	Coffee break	
11:20	**Custom Cell-, Circuit-, and System Design: (1/3)** Convener: Marc Fossion	
	Rad-Hard Telemetry and Telecommand IC suitable for RIU, RTU and ICU Satellite Subsystems	Ernesto Pun (Arquimea)
	Microchip ATMX150RHA European Mixed Technology for Advanced Designs SAMRH71	Hans-Ulrich Zurek (Microchip)
	Status update on GR716 Rad-Hard Microcontroller For Space Applications	Fredrik Johansson (Cobham Gaisler)
12:35	Lunch	

14:00 **Evaluation and Qualification**
Convener: Dieter Herrmann

Re-Thinking Reliability Analysis	Art Schaldenbrand (Cadence Design Systems)
Digital Programmable Controller (DPC): radhard die in low cost plastic package	Alain van Esbeen, Marc Fossion (Thales Alenia Space Belgium)
ESCC Single Phase Qualification	Fernando Martinez (ESA)
Characterization, Screening and Qualification of the MEDA Wind-Sensor ASIC	Servando Espejo (IMSE-CNM-CSIC / Universidad de Sevilla)

15:40 Coffee break

16:00 **Custom Cell-, Circuit-, and System Design: (2/3)**
Convener: Michael Kakoulin

A radhard LVDS chip: transistor level design aspects	Jan Wouters (IMEC)
Correlators for Interferometric Radiometry in Remote Sensing Applications, A Scaling Perspective	Erik Ryman (Omnisys Instruments AB)

Social Program

16:50	Guided Tour	*Leuven*
19:00	Welcome Reception	*Leuven city hall*

Tuesday, 19 June 2018

09:15 **Keynote Speach**

Functional Safety Management in the automotive world and beyond? — Yves Renard (ON Semiconductor)

10:00 **Space Applications: (1/2)**
Convener: Jose F. Moreno-Alvarez

SIS20: A CMOS ASIC for Solar Irradiance Sensors in Mars Surface — Prof. Vázquez Diego (IMSE-CNM-CSIC / University of Seville)

Ultimate earth observation using time delay integration line scan imagers using the CCD-in-CMOS technology — Piet de Moor (Imec)

10:50 Coffee break

11:20 **Space Applications: (2/2)**
Convener: Jörg Ackermann

Channeltron Detector Readout ASIC in 0.35µm HV CMOS for Cold Solar Wind Analysis — King Wah Wong (IRAP CNRS); Prof. Hélène Tap (INP-ENSEEIHT LAAS)

A Fault Tolerant PMAD System Using Radiation Hardened Highly Integrated AFE Integrated Circuits — Mathieu Sureau (Microsemi Corp.)

A rad-hard systems-on-chip solution for close-loop motor control — Dr. Ying Cao (MAGICS Instruments)

12:35 Lunch

14:00	**Poster Session**	David Levacq (ESA)
	Space Applications	
I	*Multi-Channel Preamplifier IC for IR-Sensor and FPA Readout*	Jörg Ackermann
II	*A rad-hard signal conditioning ASIC for space grade transducers*	Dimitris Mitrovgenis, Theodoros Athanasopoulos
	Radiation Testing and Mitigation	
III	*The First SEE Tests Campaign in Turkey at the METU Defocusing BeamlinePreliminary Setup*	Mehmet Serdar
IV	*Heavy Ion Test Results of Different Analog to Digital Converters*	Sergei Iakovlev
V	*Radiation Tolerant Stochastic Fourier-Transformation Implementation*	Kris Niederkleine
	Custom Cell-, Circuit-, and System Design	
VI	*Radiation-Hard X-Band Phase Locked Loop and Transceiver in 0.25 µm SiGe Technology*	Dr. Wojciech Debski
VII	*SEPHY: a 10/100 Ethernet Transceiver for Space Applications*	Jesús F. López-Soto
VIII	*Radiation Hardened Pulse Width Modulator in CMOS-SOI*	Dimitrios Baramilis

14:00	**Industrial Presentations**	Hilde Derdin (Imec)
1	Microchip	Erwann Berlivet Pascale Charpentier
2	Alter Technology	Dr. Sonia Vargas-Sierra Xavier Wiedemann
3	Cobham	Teresa Farris Christian Sayer
4	Cobham	Fredrik Johansson Teo DeLellis
5	Microsemi	Dorian Johnson Mathieu Sureau
6	Micross	Ian Robinson
7	Arquimea	Ferran Tejada Daniel Gonzalez
8	Magics	Jens Verbeeck Dr. Ying Cao
9	Teledyne e2v	Dr. Romain Pilard, Joseph Yeomans, Kurt Rentel, Nicolas Chantier
10	Serma/HCM.Systrel	Frédéric Oudart Maxence Leveque
11	Thales Alenia Space Belgium	Alain van Esbeen Marc Fossion
12	Microtest	Moreno Lupi Francesco Parenti
13	Renesas	Oscar Mansilla Christophe Boucheron
14	IHP	Judith Kroel Dr. Jens Schmidt
15	TRAD	Christian Chatry
16	Imec	Ozgur Gursoy Geert Thys

16:00 **Custom Cell-, Circuit-, and System Design: (3/3)**
Convener: Florence Malou

Prototype of a multi-mode C-Band capable 12-bit 1.5/3/6 GSps Quad ADCin flip-chip non-hermetic technology	Dr. Romain Pilard (Teledyne e2v)
Atom-Switch FPGA for IoT Sensing System Application	Dr. Toshitsugu Sakamoto (NEC Corporation)
Robust CMOS time-based sensor interfaces for space applications presenter	Jorge Marin (KU Leuven)

19:00 **Conference Dinner** *Faculty Club*

Wednesday, 20 June 2018

09:00 **Keynote Speach**

Perspectives for Disruptive GaN Power Device Technology	Stefaan Decoutere (IMEC)

09:45 **Radiation Hardened Technologies: (1/3)**
Convener: Dr. Constantin Papadas

Microchip ATMX150RHA Rad-Hard CMOS 150nm cell based ASIC family Radiation Characterization Test Report Total Dose (TID) and Single Event Effects (SEE)	Eric Leduc (Microchip)
DARE180U platform improvements in release 5.6	Giancarlo Franciscatto (Imec)
The Design Against Radiation Effects (DARE) design platform for TSMC 65nm process.	Michael Kakoulin (Imec)

11:20 **Radiation Hardened Technologies: (2/3)**
Convener: Franco Bigongiari

Invited Talk: Overview of ST Space Qualification in 28nm-FDSOI	Dr. Gilles Gasiot (ST Radiation Team Crolles)
ATMX150RHA Circuit Design Platform	Erwann Berlivet (Microchip)
DARE SET Simulation Flow Integrated in Virtuoso ADE L/XL Design Environment	Staf Verhaegen (Imec)

12:35 Lunch

14:00 **Radiation Hardened Technologies: (3/3)**
Convener: Frank Henkel

ESS180RH: An 180nm digital library addressing Single Event Latch-up based on X-FAB XH018	Dimitris Mitrovgenis Theodoros Athanassopoulos (European Sensor Systems)
Mixed-Signal Test Vehicle in Microchip Atmel ATMX150RHA	Julien Fleury (Weeroc)
DARE180U New Analog IPs	Laurent Berti (Imec)

15:15 **Wrap-Up and Finish** — Boris Glass (ESA), Steven Redant (Imec)

Invited Talks

Functional Safety Management in the automotive world and beyond?

Yves Renard
(ON Semiconductor)

ISO 26262 is an automotive standard that was released in November 2011 and has as target to make cars safer. This point is especially important when thinking about the actual trend towards more and more autonomous cars where the amount of safety critical electronics is increasing quickly and where the impact of potential safety critical failures is very high. Wrong decisions taken by the electronic systems can have an important impact on the people inside and outside of the car. The purpose of the standard is, by focusing on systematic and random hardware failures, to help reducing the risk of safety critical malfunctions to an acceptable level. The standard proposes to achieve this through a series of work products and through robust design methods of the system itself and its electronic sub-components.

The target of this presentation is to give a quick overview of the purpose and content of the standard and to explain how it relates to semiconductor mixed-signal developments. A general flow will be presented which starts from a safety concept and ends with an architecture that achieves a high diagnostic coverage. The core of the presentation will be dedicated to explaining the challenges to perform a functional safety analysis according to ISO 26262 and present the work products that are recommended by the standard. Also some time will be spent during the presentation to explain the impact of the safety analysis on the architecture of the component under development and to understand when enough has been done to make the device safe.

Perspectives for Disruptive GaN Power Device Technology

Stefaan Decoutere

(Imec)

Today, GaN-on-Si is accepted as a break-through power electronics technology. The favorable materials characteristics and the enhancement mode lateral HEMT device architecture have led to disruptive device performance. Issues with trapping effects and reliability that plagued early versions of the technology have been addressed and first products are in the market. While we will see through further evolutionary improvements the maturity of today's GaN-on-Si technology further increase with fast pace, research is focused on substrate technology, novel device architectures, application specific customization and higher levels of integration. To unlock the full potential of the fast switching power devices, monolithic integration of a half-bridge, co-integration of the GaN drivers, and free-wheeling diodes offer a way to reduce parasitic inductances, while on-chip temperature sensors and protection circuits increase the robustness. Such power GaN-IC's pave the way for unprecedented compact high-end power systems.

Overview of ST Space Qualification in 28nm-FDSOI

Dr. Gilles Gasiot

(ST Radiation Team Crolles)

The good intrinsic radiation resilience of the 28nm-FDSOI technology was demonstrated and reported by ST in 2014. The full space compliance of the ST industrial design platform has additionally required a wide deployment in terms of proprietary radiation modeling, design mitigation and extensive testing against protons, heavy ions and gamma rays. This overview presents 100 new space IPs in 28nm-FDSOI (std cells, memories, serdes, converters, PLLs, analog IPs, sensors) whose space qualifications are being completed by ST thru 25 existing testchips. Last, but not least, the concurrent design of new best-in-class space SoC (ARM-R52, FPGA) is also illustrated in ST 28nm-FDSOI.

Table of Papers

Session A

Space applications for analogue and mixed-signal ICs

A Fault Tolerant PMAD System Using Radiation Hardened Highly Integrated AFE Circuits

S.A. Spanoche, M. Sureau

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Abstract

Fault tolerance of power management and distribution (PMAD) systems in a radiation environment is one of the important characteristics for the reliability of spacecrafts. Furthermore, using highly integrated ICs in the PMAD design leads to lower footprint, therefore it is advantageous to consider the design of redundant PMAD system using ICs that offer a high degree of integration.

This paper describes a PMAD topology using series MOSFETS driven by a single AFE IC that implements sense and control interfaces to the power devices. Special attention is given to the aspects of parametric drift due to radiation effects on the AFE and a method of how system design can alleviate its effect is shown.

In conjunction with an FPGA, the AFE sub-system can run MPPT on multiple strings of photovoltaic modules and deliver power to the main power distribution bus. Additional protection circuits manage power distribution to loads and to and from a battery unit.

I. The PMAD Topology

The PMAD system needs to optimally transfer power from the input sources and manage transmission of power to loads and to and from the battery system. It mainly consists of DC/DC converters, protection circuits and a power transfer and fault management function that is partly local and partly remote. In our proposed topology, the inputs are assumed PV module strings for which a fast and accurate MPPT control [1] needs to run in order to track varying angle, shading and/or temperature condition per string. Thus, several boost DC/DC power converters seek independently MPP per string while driving the power distribution bus.

Voltages on input and output nodes and currents through each converter are monitored and used to control each DC/DC converter. Additionally, temperature is monitored at key points and DC arc fault detector circuits are used per string to detect arc on each high current/voltage rail that could potentially develop arc.

Control is done digitally:

- an analog front end is used to convert to digital all sense lines and to drive MOSFETs from digitally generated PWM
- an FPGA implements the DC/DC control, MPPT and power and safety management

A communication function can also be implemented for the remote function.

The connection of loads to the power distribution bus is done via individual current / SOA protection circuits that interface with the same FPGA (see Figure 1).

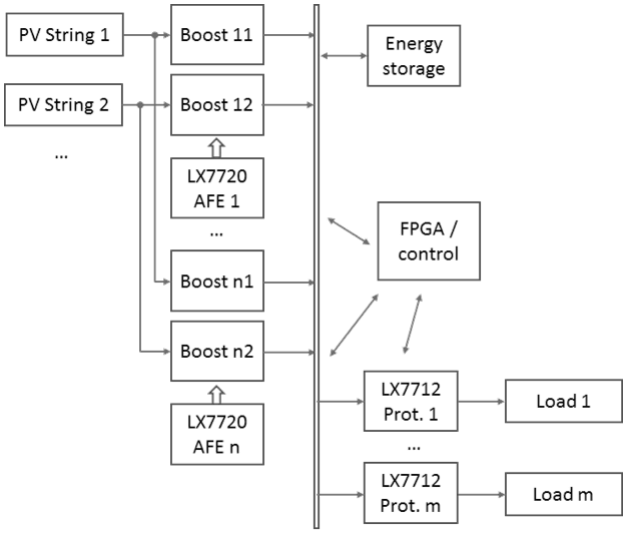

Figure 1: The PMAD block diagram

II. Fault Tolerant Power Stage Control

The DC/DC boost unit converter is implemented using a series connection of two NMOS transistors for each high and low side. This way, the controller can disable both high and low side paths in case of short circuit developing in one of the four MOSFETs at the expense of some converter efficiency loss (see Figure 2).

During regular switching periods the upper most (M11 and M21) and lower most (M14 and M24) MOSFETs are ON all the time while the mid MOSFETs (M12, M13, M22 and M23) are switching. From time to time, switching is exercising the upper most and lower most MOSFETs to verify their health state while the mid MOSFETS are turned ON continuously.

If shoot-through current or inductor current sensors detect a large change when moving from mid to upper most and lower most MOSFETs a fault is identified and the power stage is disabled and a redundant power stage is enabled (e.g. Boost 11 is disabled and Boost n1 is enabled in Figure 1).

The analog front end can sense both inductor and shoot through current if any. The shoot through current measure is based on a difference measurement: first the switching is done with enough dead band to guarantee no shoot through current

and the peak current is measured, then, in the next switching cycle, the timing to be measured is applied and the peak current is measured again. The difference between these values is a measure of the timing dependent shoot through current. This measure is repeated several times and the controller low pass filters this measure to eliminate input or output transient influence on the measurement.

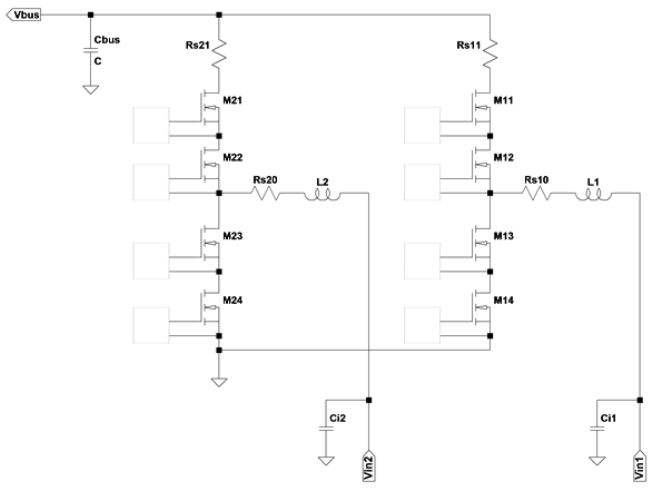

Figure 2: The DC/DC boost fault tolerant power stage

The shoot through current, together with a conversion efficiency measure (using input and output currents and voltages sense) are used by the FPGA-based controller to constantly fine-tune the MOSFETs timing in order to track the actual value and compensate for any long-term radiation or temperature induced timing drift.

This technique avoids needing to add a lot of margin for timing degradation and using a large dead time like in a classical design. The other alternative to classical design is to use a circuit that includes some loop controlled delay in the gate drivers. These circuits are more complex and expensive to build. Our solution instead uses the extra current sensor already available in LX7720 and compensates for all variation including power MOSFETs'.

III. Using an Integrated AFE as a PMAD Element

Traditionally, LX7720 (see Figure 3) [2] is used in motor control applications where it drives the power MOSFETS for the motor and solenoid control and acquires output currents and a resolver interface. However most of the LX7720 can be used in other power control applications. Particularly, in this PMAD system application, we use three voltage sense ADC channels (Vin1, Vin2 and Vbus – see Figure 2) and four current sense ADC channels are used to sense the inductor current (via Rs10 and Rs20) and shoot through current (via Rs11 and Rs21) for two fault tolerant power stages.

Four high side / low side pairs of gate drivers are used to drive all 8 MOSFETS (M11-M24) required to implement the two fault tolerant power stages. The LX7720 internal charge pump is activated to turn permanently ON the upper most side MOSFETs (M11 and M21) connected directly to the rail (except when the estimation of the health of the system is done and M11/M21 change roles with M12/M22).

Additionally, the LX7720 resolver driver outputs are used to drive the primary of an isolated forward DC/DC converter to power an auxiliary circuit used for PV arc fault detection. A good tolerance for larger power ground versus signal ground voltages makes this circuit operate well in this power control application. As seen in Figure 3, most functions integrated in LX7720 are used in this application.

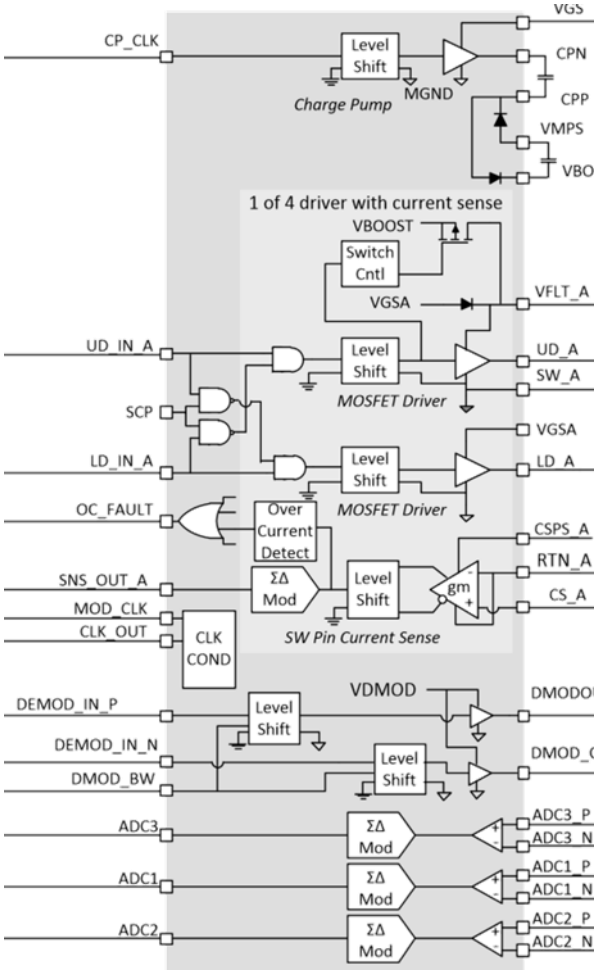

Figure 3: LX7720 block diagram detail

IV. Other System Implementation Aspects

The LX7712 [3] is a power line protection device that is used for spacecraft power distribution. It provides a means to turn on or off a DC load with current limit up to 5A (LCL class 4 or below and RLCL class 2 or below per ECSS-E-ST-20-20C). The LX7712 is an integrated circuit which includes a solid-state P Channel MOSET switch and catch diode (see Figure 4); integration allows the temperature of the switch to trigger an optional thermal shutdown. It can be configured as a latch-able current limiter or a fold-back current limiter. Multiple devices can be paralleled in a master/slave arrangement if an increased LCL class is needed.

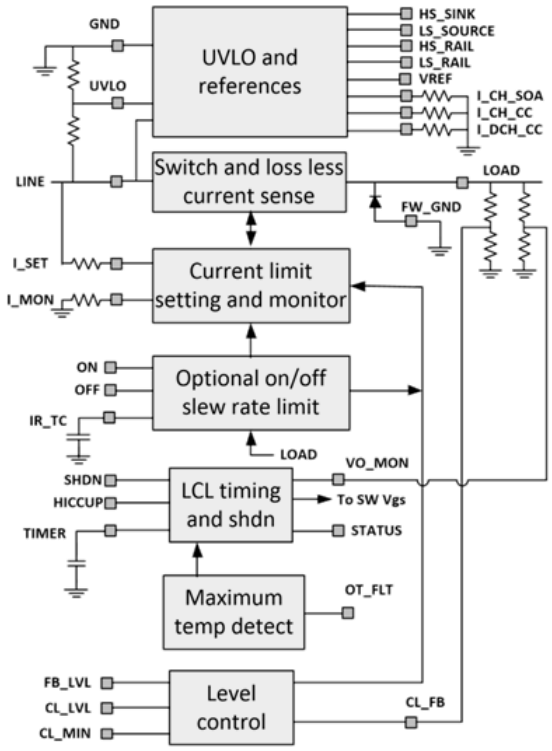

Figure 4: LX7712 block diagram

The latch-able current limiter can be configured to latch in the off state due to a fault (LCL) or to attempt to restart in a hiccup mode (RLCL). A fault time integrating function remembers the cumulative effect of short fault pulses. The fault timer can be configured to have a fixed duration or a duration that is a function of the voltage drop from line-to-load across the device.

A resistor programmable timer discharge function can insure the device has had adequate time to dissipate excess energy before attempting to restart.

In fold-back current limit mode the profile of the fold-back load current versus load voltage curve is resistor programmable. It is also possible to configure the fold-back feature for bi-stable operation; applying an overload forces the current limit to a safe trickle level and, when the fault is corrected, the current limit returns to its normal level. This prevents “soft short” power dissipation situations.

The controlled current ramp function can be used to limit the slew rate of the current during turn on and turn off and avoid EMI problems.

The overall SOA characteristic of the LX7712 is shown in figure 5. If higher currents are needed, the system can connect two or more LX7712 in parallel and connect them in a master/slave configuration to share the load current.

The FPGA implements several state machines to operate each LX7720 AFE:

- 2 PID controllers to operate the two DC/DC converters
- 2 maximum power point tracker state machines
- 2 shoot-through current / timing optimizer state machines
- 2 fault detection and fault management state machines

Beside these, the FPGA must also run load on/off control, diagnostics and communication functions to orchestrate the PMAD operation.

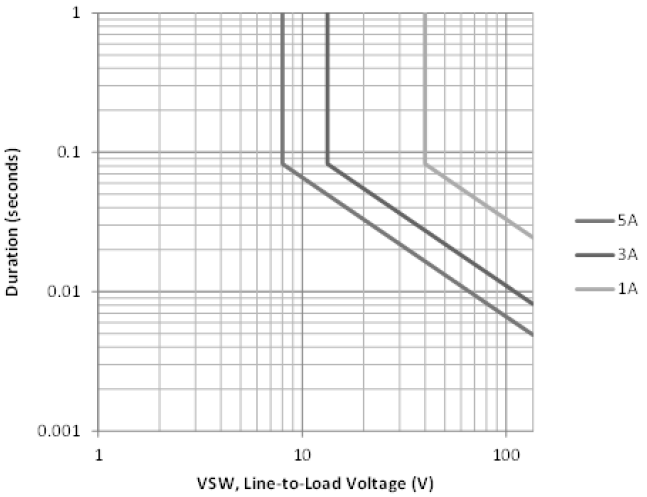

Figure 5: Safe operating area for LX7712 switch

Because the DC/DC converter source is a PV module or string the associated control is based on a slow / fast input voltage regulation loop approach. The fast loop implements a PID loop to regulate the input voltage of the boost DC/DC to a target voltage, the loop uses the difference of the input voltage to target voltage to drive the DD/DC converter duty cycle, this loop limits duty cycle such that SOA of devices is met (i.e. the MPP will not be reached if input or output currents and voltages exceed the safe levels or if the junction temperature is above a pre-determined value).

While the fast loop regulates the input voltage to a target voltage, the slow loop (MPPT state machine) dynamically determines that target voltage to reach maximum power point (MPP). One approach that can yield a very fast control for the slow loop is described in [1], here a PV model and a minimum number of off-MPP experiments are used to determine directly the ideal PMM after a light, temperature or shading change happens. The MPPT response time of this method after an abrupt shading change is e.g. 1ms (20 switching cycles) if the input filtering is not excessive. In case of partial shading, the control avoids large reverse biasing of the affected cell (hot spot suppression).

The shoot through current / dead time optimizer is designed to adjust timing of the high / low side MOSFETs such that the efficiency is optimized and estimated shoot through current is negligible while dead time is minimum.

The value of the shoot through current is a relative measurement as previously described and represents an averaged difference between the measured current at large margin v.s. estimated margin. The sense chain is limited to a known resolution. If the difference is smaller than that resolution then the timing does not yield shoot through current and the loop can further reduce the dead time, otherwise dead time is increased.

The efficiency optimization is done by changing the switching frequency and observing a measure of losses in the converter (Vout x Iout – Vin x Iin). The optimization space is a range of switching frequencies. This can be a discrete set for systems that cannot tolerate any switching frequency or a frequency range. The optimizer start form the largest frequency and uses a steepest descent algorithm.

V. Conclusions and Future Work

A new application for an IC traditionally used in actuator control is described. Based on the novel usage, LX7720 implements the analog front end of a PMAD system. The hardware offered by LX7720 allows to build a system that dynamically performs MPPT while it tracks the temperature and/or radiation induced drift of the power stage and gate drivers and optimizes dead time and conversion efficiency. A rad-hard FPGA and a group of LCL/RLCL using LX7712 integrated circuits complete the system with protection towards loads and remote control.

A technology demonstrator is being built. Measurement results will be available by the time of publication.

VI. References

[1] S. A. Spanoche, J. D. Stewart, S. L. Hawley and I. E. Opris, (2013, April) "Model-Based Method for Partially Shaded PV Module Hot-Spot Suppression," in IEEE Journal of Photovoltaics, vol. 3, no. 2, pp. 785-790.

[2] Microsemi Corp., LX7720, Rad Hard Spacecraft Power Driver with Rotation and Position Sensing, Datasheet, (available upon request)

[3] Microsemi Corp., LX7712, Rad Tolerant Power Line Protector Device, Datasheet, (available upon request)

A rad-hard signal conditioning ASIC for space grade transducers

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Abstract

European Sensor Systems develops and manufactures high quality sensors based on MEMS technology. The company has designed, fabricated and tested a radiation tolerant signal conditioning ASIC for capacitive sensors as part of a space grade transducer. This paper presents the architecture and implementation of the ASIC, the results of the irradiation campaign and the tests performed at the engineering models that incorporate the ASIC.

I. INTRODUCTION

In the course of the ESA activity "Standard Accuracy Pressure Transducer" [1], European Sensor Systems has been developing a "Space Qualified Family of MEMS Pressure Modules for Satellite Applications" based on MEMS capacitive sensors. In order to interface with the MEMS a custom radiation-hardened signal conditioning ASIC was needed.

The parts of the pressure transducer are enclosed into an all welded titanium mechanical housing. The constituent parts are: 1) the pressure component, which contains the MEMS and the ASIC, 2) the power supply unit, which provides a regulated voltage to the ASIC 3) the thermistor, which is used for calibration and 4) the mechanical structure for the housing of the pressure transducer. The architecture is shown in Figure 1.

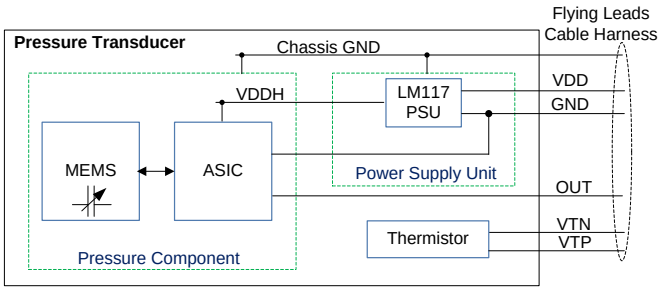

Figure 1: Transducer Architecture

The MEMS sensors are designed to cover the application's pressure ranges (7, 22, 150, 310 bar) with dimensions 2×2×0.4 mm^3 using European Sensor Systems TM30P1111 technology, which is a combination of SOI, bulk and surface micro-machining process for the fabrication of capacitive pressure sensors. The ASIC (ESS214B) is capable of interfacing the above MEMS sensors, provides accurate capacitance to analog/digital conversion and is described in this paper. It is a design re-spin of ESS214 and addresses the post-irradiation performance issues encountered in the first version [2].

The paper is organized as follows: Section II presents the architecture of the ASIC, Section III presents the design implementation, Section IV presents the electrical, mechanical and thermal tests that have been performed at transducer level and Section V presents the irradiation test results at die level.

II. ASIC DESCRIPTION

A. Features

The ASIC can support a full-scale input capacitance range of ±5.6pF with a base capacitance up to 40pF. The ASIC has a 10-bit resolution analog output (OUT) from 0V to 5V (corresponds to 105% of maximum expected operating pressure). Moreover, the ASIC offers, a non-calibrated 32-bit digital output for pressure measurement and a 32-bit digital output for temperature measurement of the on-chip temperature sensor. The digital outputs are available via the I^2C compatible serial interface or the input serial digital (ISD) interface. The ASIC has an internal clock oscillator of 10 MHz, which is the frequency of operation of the digital part. The die is supplied with VDDH=5.7V provided by the LM117 regulator [3]. The analog and digital cores operate at 3.3V and the I/O communication is performed at 0V/5.7V. A One-time Programmable (OTP) memory is also incorporated.

B. Architecture

The Capacitance-to-Digital Converter combines the Capacitance-to-Voltage converter with a second-order ΣΔ modulator and a decimation filter to produce a high resolution output with a programmable update rate. The architecture is shown in Figure 2.

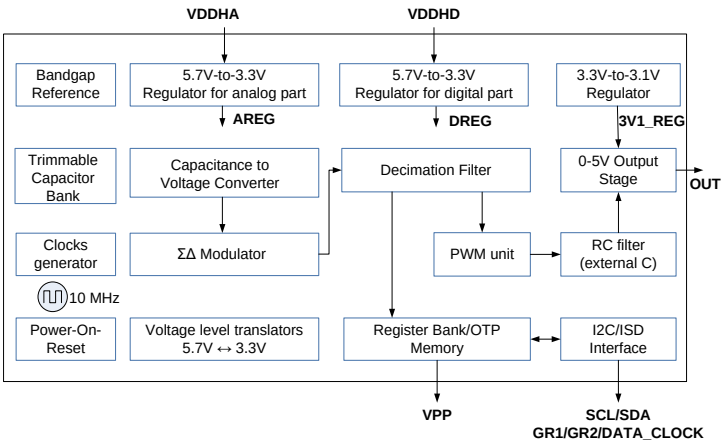

Figure 2: ASIC Architecture

The Capacitance-to-Voltage converter uses the chopper stabilization technique [4], whereas the ΣΔ modulator uses the correlated double sampling technique [4] to reduce low frequency noise respectively. Sensor capacitance variations can be compensated by an on-chip programmable capacitor bank. The voltage gain of the Capacitance-to-Voltage is programmable. The Pulse Width Modulation (PWM) unit has a programmable offset and scale factor. The architecture of ESS214B is quite similar to its predecessor ESS214 [2] with the design modification of the output stage discussed in the next section.

III. ASIC IMPLEMENTATION

A. *XH018 Technology*

ESS214B is based on the architecture of its commercial counterparts [5], which were already manufactured in XH018. X-FAB XH018 Process is a 0.18 micron Modular Mixed Signal HV CMOS Technology [6]. Based upon the industrial standard XH018 has single poly with up to six metal layers 0.18-micron drawn gate length N-well process.

B. *Output stage*

At the previous version the 10 KHz output had a voltage range of 0V to 5.7V and was filtered off-chip by an RC filter in order to generate an analog signal at the voltage range of 0V-5.7V. The inverter of the last stage of the level-converter was implemented using high-voltage transistors. The off-resistance of the High Voltage NMOS was susceptible to Total Ionization Dose (TID) thus altering the output voltage [2].

At this revision the scheme shown in Figure 3 has been implemented for the output stage. The 10 KHz digital output of the PWM unit is buffered and inverted before filtering. It is at the level of 0V to 3.1V. The RC filter has a cut-off frequency of 10 Hz, with a resistance (Rfilt) integrated on-chip and a capacitor (Cfilt) located off-chip. The filtered signal (Vx) is then applied to an inverting amplifier configuration. The last stage of the amplification stage is a high-voltage stage. The output signal (OUT) is merely amplified by adjusting the ratio R_2/R_1 to give a voltage output range at the 0-5V range.

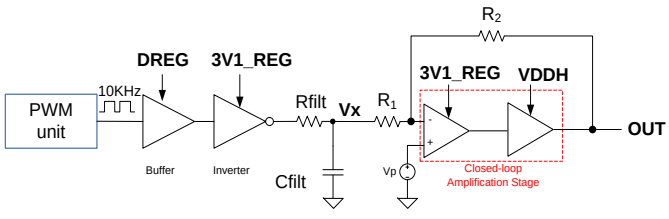

Figure 3: Output stage

C. *Design details*

For the implementation of the ASIC, the analog on-top methodology has been followed. The layout view of ESS214B is shown in Figure 4. The bigger portion is occupied by the digital part. To facilitate wire-bonding the pad sizes are 100x200 um^2. The die size is 6.3 mm^2.

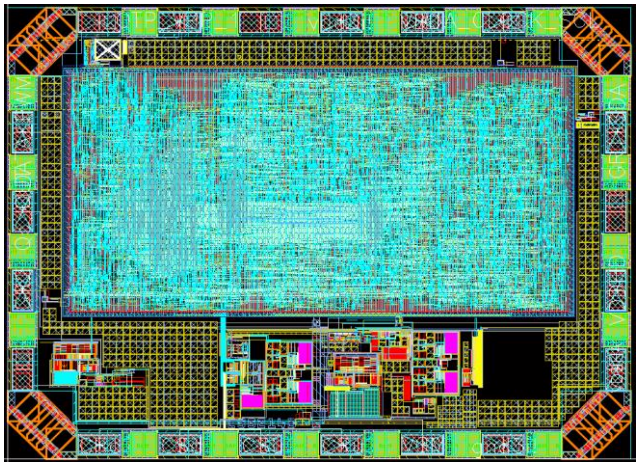

Figure 4: ASIC layout view

D. *Radiation mitigation strategy*

In order to address the problem of Single Event Upsets, the Triple Module Redundancy method with voting has been adopted to all flip-flops of the digital part.

In order to address the problem of Single Event Latch-up (SEL), for the analog part all PMOS devices have been enclosed by N-type guard rings and all the NMOS devices have been enclosed by P-type guard rings. For the digital part a SEL immune library was developed. ESS180RH [7] is a family of digital standard cells based on D_CELLSL_JI3V of XH018. ESS180RH [7] contains combinational (logic gates), sequential (scan flip-flops) and special cells (layout fillers, antenna protection cells, level shifters). The NMOS and PMOS devices of each logic gate have been surrounded by P-type and N-type guard rings respectively.

IV. IRRADIATION CAMPAIGN

The test setup preparation for the various irradiation tests was based on ESCC Basic Specification No. 25100 [8].

A. *TID*

TID tests have been performed at ten dies up to a total dose of 128.8 Krad at ESA ESTEC facility. After the TID irradiation and measurement steps, the samples were submitted to temperature annealing. ASIC samples were biased and measured after 24 and 168 hours of operation at room temperature. An accelerated ageing test followed the room temperature annealing test. The whole sample pool was placed on a temperature chamber at 100°C for 168 hours. After the accelerated ageing test the electrical performance of the samples was evaluated.

The DUTs hosted by a daughter card PCB are shown in Figure 5. Each daughter card can host up to 5 DUTs. Thus, two daughter cards are assembled each one hosting 5 DUTs, while a third same daughter card is populated with the 3 reference DUTs. During each irradiation step the daughter cards with ten ESS214B DUTs are transferred to the irradiation chamber, while the third daughter card is operating outside the irradiation chamber.

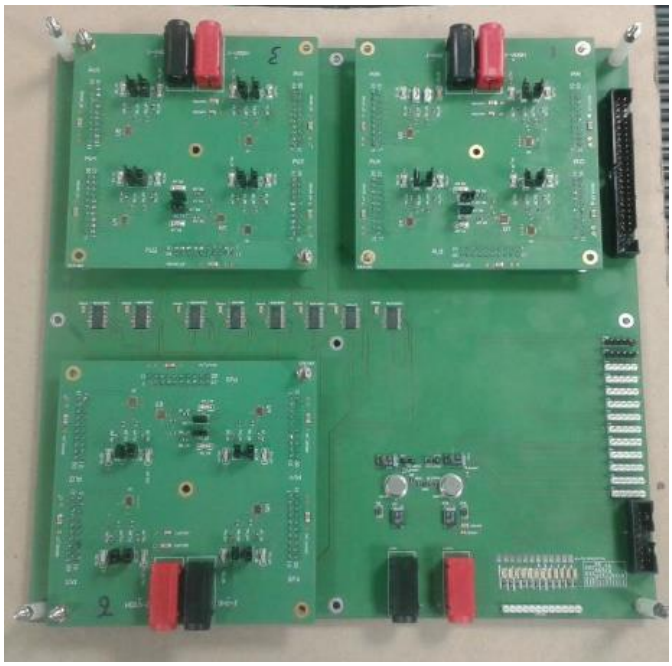

Figure 5: TID motherboard with daughter cards

The irradiation steps are described in Table 1. The total ionising dose is 1.288 kGy = 128.8 Krad

Table 1: TID Irradiation steps

Multiple Irradiation Steps	Total Ionization Dose (water) Gy	Dose Rate (water) Gy/h
1	66.96	4.062
2	22.23	4.052
3	76.28	4.034
4	77.02	4.024
5	91.39	4.022
6	278.3	4.018
7	192.0	4.070
8	74.74	4.068
9	109.7	4.066
10	279.1	4.057
Total 1.288 kGy		

The measured quantities between each irradiation step are the bandgap reference voltage, the output voltage of each regulator (AREG, DREG, 3V1_REG), the current drawn from the analog voltage supply (VDDHA), the current drawn from the digital voltage supply (VDDHD), the digital outputs (pressure channel and temperature channel) and the analog output (OUT).

The digital output of the pressure channel is not affected by the TID. On the contrary, all the regulated voltages are slightly affected, which can be attributed to a shift of the bandgap reference voltage. Irradiation induced holes get trapped in the body of the field oxide near the Si-SiO2 interface. This increases the base leakage current and degrade the gain of the diode-connected bipolar transistors used in the bandgap reference circuit. The shift of the bandgap reference voltage affects the 3V1_REG node, which sets the voltage level of the filtered PWM output (Vx) and as a consequence affects the analog output.

A. SEE: SEL

For the radiation tests the ion cocktail of Table 1 has been applied to the DUTs. Three dies have been tested for SEE/SEL in the HIF Cyclotron, of Université Catholique de Louvain, Belgium.

Each daughter card has a heating pad attached at its bottom using a thermal conductive adhesive for setting the temperature to a level higher than 75 °C in a closed-loop control by a microcontroller. The SEU board is shown in Figure 6.

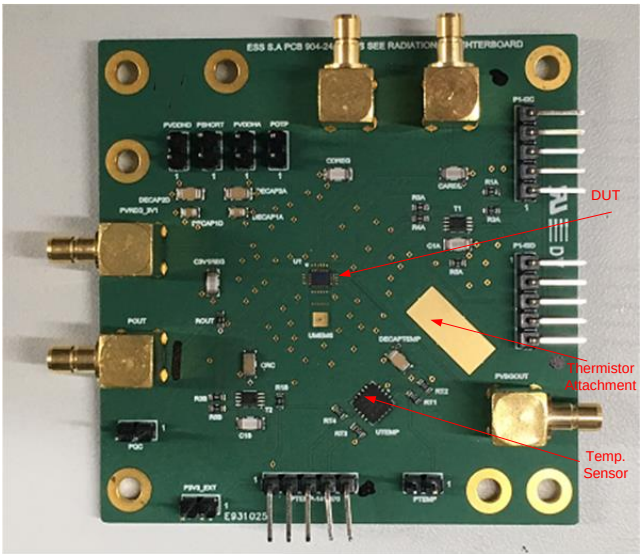

Figure 6: SEU Daughter card

The irradiated dies were operating under the expected conditions. During the experiment, no SEL event has been detected in the analog voltage supply (VDDHA) or digital voltage supply (VDDHD). The test has been performed at 75 °C. The detailed steps are shown in Table 1.

Table 1: SEL Irradiation Steps

Ion	Energy (MeV)	LET (Si) (MeV·cm²/mg)	Fluence (ions/cm²)	Temp (°C)	SEL
$^{13}C^{4+}$	131	1.3	10^7	75	No
$^{22}Ne^{7+}$	238	3.3	10^7	75	No
$^{40}Ar^{12+}$	379	10.0	10^7	75	No
$^{58}Ni^{18+}$	582	20.4	10^7	75	No
$^{84}Kr^{25+}$	769	32.4	10^7	75	No
$^{124}Xe^{35+}$	995	62.5	10^7	75	No

B. SEE: SEU

The same setup with the SEL event has been used with the exception that the 3 DUTs were irradiated at room temperature.

The digital registers were continuously monitored an SEU error is logged if two consecutive readings differ. Post-processing of irradiation results suggests that the SEU immunity at least up to 32.4 MeV·cm^2/mg using Kr-769. The detailed steps are shown in Table 2.

Table 2: SEU Irradiation Steps

Ion	Energy (MeV)	LET (Si) (MeV·cm^2/ mg)	Fluence (ions/ cm^2)	Temp (°C)	SEU
$^{13}C^{4+}$	131	1.3	10^7	Ambient	No
$^{22}Ne^{7+}$	238	3.3	10^7	Ambient	No
$^{40}Ar^{12+}$	379	10.0	10^7	Ambient	No
$^{58}Ni^{18+}$	582	20.4	10^7	Ambient	No
$^{84}Kr^{25+}$	769	32.4	10^7	Ambient	No
$^{124}Xe^{35+}$	995	62.5	10^7	Ambient	2-4

C. *Displacement Damage*

Displacement damage tests have been performed at three ASICs at UCL LIF facility up to 26.7 x 109 # 62 MeV protons/cm^2 without any functional performance degradation.

V. ENGINEERING MODEL VERIFICATION

The mechanical, electrical, thermal and environmental tests described in this section were performed at the level of the engineering model of the transducer shown in Figure 7.

Figure 7: Engineering model of space grade transducer

Functional tests are positioned multiple times within the test plan in order to quantify the effect of various parameters (mechanical, electrical, thermal, and environmental) on the transmitters under test. The proof pressure test aims to verify the structural capability of the units under test when proof pressure is applied at ambient temperature. The external leakage test measures the leakage of the sensed medium to the surrounding environment of the units under test. The functional tests comprise calibration, current consumption and output signal tests. The vibration tests are a series of mechanical tests, which aim to monitor the effect of sinusoidal and random vibration on the transducers under test. The thermal vacuum cycling test aims to simulate the thermal conditions under vacuum to be encountered by the units under test during flight. The insulation resistance test aims to quantify the electrical insulation between all insulated points and the case of the units under test. The purpose of electrical bonding test is to verify that all mechanical assemblies are electrically connected to the mounting flange. Before the onset of the test campaign, the units under test undergo a standard cleaning procedure in the manufacturing stage, while towards the end of the test campaign a cleanliness verification procedure is performed in order to monitor potential levels of induced contamination.

The engineering models were tested by executing the campaign described above, the results are currently being processed and the results will be reported in the forthcoming Test Review Board (TRB) meeting.

VI. CONCLUSIONS

The architecture and design of a radiation tolerant ASIC as part of a space grade transducer has been presented. The manufactured dies have been tested under irradiation for total ionization dose, single event effects and displacement damage. The radiation mitigation strategies applied at electrical and physical level have been proven sufficient though some optimization of the bandgap reference circuit is provisioned. The ASICs has been incorporated in the engineering model, and tested under all mechanical, electrical, thermal and environmental parameters.

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SIS20: A CMOS ASIC for Solar Irradiance Sensors in Mars Surface

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Abstract

This paper reports the design and characterization of the ASIC SIS20, planned for an instrument aimed to measure Solar Irradiance on the surface of Mars. It has been designed using the AMS0.35µm CMOS technology and with the rad-hard digital library developed at IMSE (Spain). The ASIC is intended for flying with the ExoMars2020 mission. The main blocks composing the ASIC and their functionality are briefly described. In addition, some representative results from the lab are presented, demonstrating a correct operation (inside specifications) in the range -125ºC to 50ºC.

I. Introduction

The presence of atmospheric/ environmental/ meteorological research stations on the surface of Mars, has been critical to understanding some aspects of the climate and atmospheric dynamics of the planet by providing complementary information from that obtained through orbiting devices. Among them, solar irradiance and temperature sensors are typically present in meteorological instruments.

This paper presents SIS20, an ASIC in a standard CMOS technology designed as a mixed-signal front-end for a solar irradiance sensor in the context of the ExoMars2020 mission (part of the METEO package [1]). The environmental context in terms of dust and extreme low temperatures imposes relative strong requisites in the design [2].

The distribution of the paper is as follows. Section II describes the ASIC and the major blocks in the design. Present experimental results from the lab are given and discussed in Section III. Finally, some conclusions are given in Section IV.

II. System Description

Figure 1 shows a conceptual block diagram of the ASIC-SIS20. The main functionality is twofold: read (analog) and convert (to digital) the photocurrents generated by a set of off-chip photo-diodes. However, it has been designed to perform additional functions of interest.

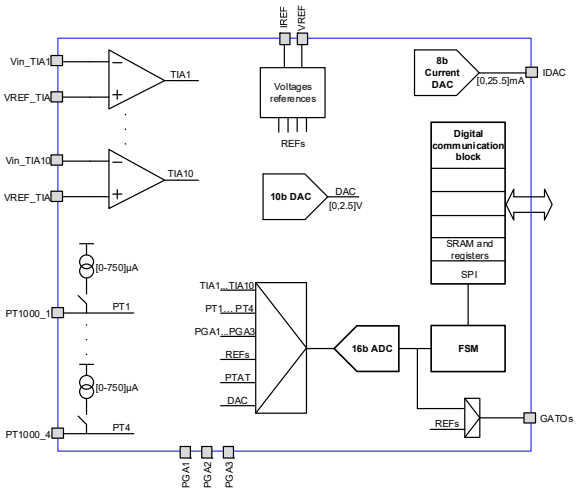

Figure 1: Simplified block system diagram of ASIC-SIS20

The four major sub-systems of the ASIC are:

- An Analog Front-End comprising:
  - 10 identical photodiode trans-impedance amplifiers (TIAs) or reading channels with two external (switched) feedback networks (low/high gain modes) per channel.
  - 4 PT1000 for resistance measurements.
  - An 8-bit current-output DAC to drive an off-chip LED as a light source for calibration and monitoring purposes.
  - 3 general purpose voltage amplifiers, with configurable gain (1/50).
  - Internal voltage (bandgap based) and current reference circuits.
  - Miscellaneous pins and multiplexers (GATOs) for testing and characterization purposes.
- A 16-Bits ADC channel preceded by an extended input multiplexed and capacitive input impedance instrumentation amplifier with configurable gain (1/ 50).
- A 10-bits DAC used to generate reference voltages for internal signal ranges accommodation.

- A digital circuitry comprising:
  - Digital signal processing blocks.
  - A disable 100Kbits/sec slave SPI interface for configuration and data transmission.
  - A bank of registers for ASIC configuration, control and data I/O transmissions.
  - A Power-on-reset (POR) circuitry.
  - CLK signal generator.

A deeper explanation of the some of the most significant blocks is followed.

A. Transimpedance amplifiers (TIAs)

The ASIC contains 10 identical photodiode transimpedance amplifiers (TIAs) or reading channels. An external RC feedback network is connected to every TIA, being possible to configure each RC network either in low or high gain modes in each channel. Such gains are managed to compensate the radiation conditions taken into account dust presence and sun exposure (day/night). Switching is made internally in the ASIC through CMOS switches integrated in the TIAs. One of the 10 TIAs is not connected externally and is used to measure the leakage current (expected to be within the ±2nA range) for calibration purposes.

Each transimpedance channel is composed of a Miller amplifier (a folded cascode OTA with p-channel input differential pair followed by a common-source, p-input stage) and switches controlled by specific bits of configuration registers. With those switches, the amplifier offset could be measured and the digital conversion can be done directly between the terminals of the feedback resistor, being the measurement insensitive to the amplifier offset. The main simulation parameters of the Miller amplifier at 0ºC are shown in Table I. External resistor values employed are 100kΩ (low gain) and 10MΩ (high gain) with feedback capacitor (due to stability conditions) values of 20pF and 2pF, respectively.

Table I: Characteristic parameters of the Miller amplifier at 0ºC.

	Mean	Sigma
DC_GAIN [dB]	133.8	0.017
PM [º]	61.99	0.042
BW_3dB [Hz]	0.294	0.004
CMRR [dB]	127.6	3.762
PSRR [dB]	91.82	0.291
Offset [μV]	22.3	200.6

B. ADC channel and Input Multiplexers

The AD converter channel, composed by a two-stage instrumentation amplifier and a dual-slope converter, uses a fully differential architecture and operates with an on-chip generated clock of frequency around 50MHz. The output is codified with 16 bits (15 bits + 1-bit-sign).

The two-stage instrumentation amplifier provides capacitive input impedance, gain configuration and common mode adjustment. Its first stage is based on a two single-ended opamp configuration and a programmable resistor network that makes possible to set two different gains (1 or 50). In the low gain mode (gain =1), the peak-to-peak differential input signal range is 3.6V, and ±36mV for the high gain (=50) case. The second stage of the amplifier has unity gain and is composed of resistors and a fully differential opamp with common mode feedback. Zero-crossing discontinuity could be a major issue in fully differential dual-slope converters. To avoid this problem, a level-shifting signal could be optionally activated to add a positive DC signal to the second stage input, shifting the differential input signal into the positive half-range. The associated differential output signal swing is ±2.0V and the output common-mode reference level is 1.5V.

The dual-slope ADC is composed of an integrator, a comparator and a finite state machine (FSM). The integrator comprises a differential RC configuration and a fully differential opamp, identical to that employed in the second stage of the amplifier. The FSM configures the integrator for the conventional “two-slopes” operation. It uses a ~50MHz clock, generated on-chip. During the first integration, the integrator is reset and the input signal is integrated during 2N-3 (2N/8) clock cycles, with N being the required number of bits in the conversion process. In the second integration, the comparator (based on a fast regenerative latch and a preamplifier) detects the zero-crossing of the input signal and the reference signal is integrated with the opposite sign to the input signal.

The complete conversion process is controlled by the digital control block, which is responsible for the control of the signal conditioning block, the gain and level-shift in the preamplifier and also for the starting the FSM.

The ADC channel is used to measure (digitally coded) not only the internal signals generated by the TIAs and PT100, but also other internally generated signals. For that, the ADC channel is preceded by CMOS switch-based multiplexers. The effects of their on-resistance are avoided thanks to the capacitive input of the ADC.

In normal operation, a Finite Sequential Machine (FSM) controls the ADC by regulating the sequence of operations, performing the required switching, controlling the internal comparator, etc. This FSM operates at a relative high frequency, because the conversion process requires at least 2^{15} clock cycles.

C. General purpose voltage amplifier

The instrumentation amplifier of the ADC can also be employed as a generic amplifier or PGA. For that, three input pins are provided. The input connection is carried out through the ADC multiplexer, being possible to set the amplifier gain to 1 or 50.

D. PT1000

SIS20 contains 4 identical channels for temperature measurements based on the resistance dependence of PT1000 thermistors with the temperature. The operative range of temperature is -125ºC to 100ºC.

Each channel has an independent node (named positive), but the other (negative one) is common to the 4 channels. The temperature to voltage conversion is carried out by connecting a 4-bit resolution current source (programmable from 0 to

750μA) to the positive input of the selected PT100 through digitally controlled CMOS analog switches. On the other hand, the negative common node can be connected to ground or to an internal generated reference voltage of 0.3V (also available at the input of the ADC) with enough current sinking capability. This option is exploited to improve the resolution of the measurements under certain circumstances.

E. 10-bit sub-ranging DAC

The aim of the 10-bit DAC is to facilitate and improve the resolution of the processed data. Namely, the 10-bit voltage-output DAC is used to generate a reference voltage in the range [0, 2.5V] that, connected to the negative input rail of the ADC channel, subtracts the corresponding value from the voltage present at the positive one. The DAC topology consists on a conventional resistive ladder and an analog multiplexer. The LSB equivalent output voltage is 2,441mV.

F. Current-output DAC

An 8-bit current-output DAC is used to drive an off-chip LED that will be used as a light source for calibration and for monitoring the measuring system. The output current range is [0, 25.5mA] and the LSB equivalent output current is 100uA.

G. Voltage and current references block

A voltage reference (VREF) of 2.5V is generated internally using a band-gap circuit and an amplifier-based buffer. Moreover, a current reference (IREF) circuit with a feedback loop and external precise 10kΩ resistor are employed to obtain a steady current reference of 100μA.

H. ASIC temperature, power supply indicators and power-on reset circuit

The bandgap generates a proportional to absolute temperature (PTAT) current, which is forced to flow through an internal grounded resistor. The associated voltage can be sent to the ADC channel and employed to measure the real-time ASIC temperature.

A resistive divider is used to generate a VDD/3 level, which is sent to the ADC channel and used to monitor the real-time ASIC power supply voltage.

Power-on reset (POR) circuit generates a reset in the circuit after power up.

I. Digital processing/communication unit

The ASIC-SIS digital processing block comprises a serial peripheral interface (SPI), a static RAM Controller, a math computing unit and a circuitry for testing purposes. It performs several actions:

- It acts as the communication interface with the external devices.
- It configures and monitors the internal registers.
- It performs simple math data processing (accumulation of data for example)
- It controls and monitors the circuitry included for testing purposes.

The SPI is a 100kbits/sec synchronous serial data slave interface that provides communication with an external master device. This master device can read/write the internal registers of the ASIC using an 8bit-word command. Furthermore, the SRAM controller deals with the generation and synchronization of the signals needed to access in read and write mode of the ASIC internal registers. The math computing unit takes a fixed number of measurements and provides an accumulated and a pseudo-sigma value for the set of measurements. Finally, the test unit is used to monitor specific internal signals of the ASIC and verify the correct operation of the math computing unit.

III. EXPERIMENTAL RESULTS

The ASIC has been integrated in the standard AMS CMOS 0.35μm technology using the rad-hard library previously developed by our group at IMSE [3] [4]. It operates essentially from a 3.3V supply, but digital IO pins operate from 5.0V and have 5.0V logic levels. Figure 2 shows the chip microphotograph. It occupies and area of 5μmx4μm approximately.

The design was taped out in June 2017. Samples are packaged in a 68 pins module. A complete functional testing in the specified range of temperature (-125º C to 50º C) has been carried out for several samples. Figure 3 shows the PCB test board.

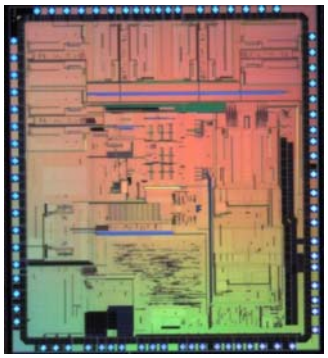

Figure 2: Chip microphotograph

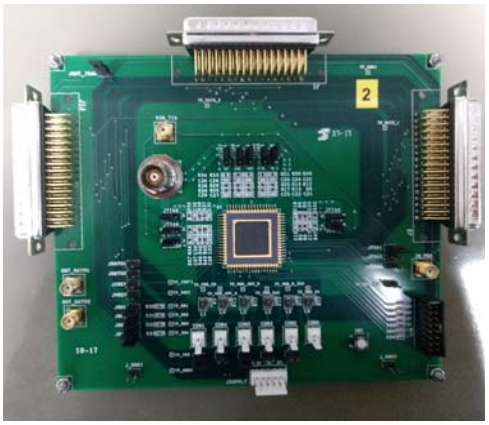

Figure 3: PCB test board

Experiments in the lab have been carried out for a set of 10 samples, in the low and high gain configurations of TIAs and ADC channel and in the specified range of temperatures

[-125ºC, 50ºC]. Some of the most significant results are given below.

Figure 4 depicts a representative voltage-current characteristic of a TIA once the leakage current has been compensated. Curves for low and high gain configurations are shown for three different temperatures (-125ºC, 25ºC and 50ºC). The low/high gain external RC feedback network used corresponds to a 100kΩ/100MΩ resistor and a 20pF/2pF capacitor. The slope of the linear part of the curve represents the measured resistances. It can be seen that they operate correctly in the specified range of temperatures. The amplifier offset has been measured in each case, exhibiting a maximum value of 470µV (reached at -125ºC). Anyway, offset effects can be compensated during the current measurements.

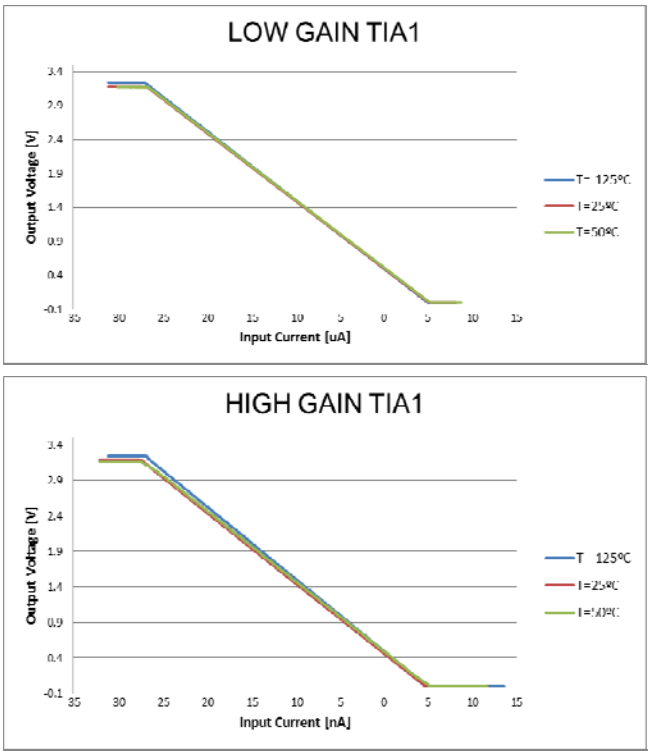

Figure 4: TIA1 characteristic with compensated leakage current

Figure 5 shows the ADC chain (including preamplifiers) output value (accumulator code) measured by the math computing unit over 256 measurements versus the applied differential input. Although it presents very good behaviour in terms of linearity and noise, gain and offset errors need to be compensated by calculations (this must be done for each ASIC sample separately). Such corrections should be done on Earth using the ASIC characterization data. For this reason, some on-chip fixed voltage references derived from the bandgap are intentionally generated.

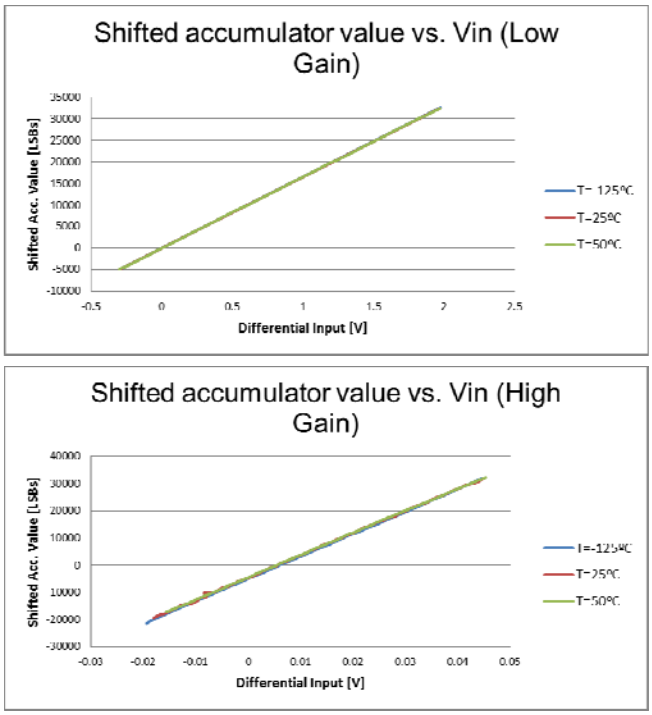

Figure 5: Accumulator code value versus differential input for ADC low and high gain

Every PT1000 has been also verified in the temperature range of -125ºC to 50ºC. Currents from 0 to 750µA have been considered. The worst case of current relative error is only 4.74%.

The correctness of the programmable voltage in the range [0, 2.5V] at the 10-bit DAC output has been confirmed. Indeed, the current DAC has been also proved to work correctly in the output current range of [0, 25.5mA].

The bandgap as well as the voltage and current references blocks works properly. PTAT indicator exhibits an optimal performance. Observable nodes VREF (voltage reference) and IREF (current reference) achieve rather outstanding values. With respect to the corresponding voltage of IREF (1.0V nominal goal for a 100µA current through a 10kΩ resistor), it exhibits a mean of 0.98V and a standard deviation of 0.02%. On the other hand, VREF (2.5V nominal goal) shows a maximum variation of ±21ppm/ºC, a mean of 2.46V and a standard deviation of 0.45%. Figure 7 presents VREF vs temperature [-125ºC, 50ºC] for different control words.

With respect the digital block, it has been tested in the said conditions using Arduino DUE. It can be mentioned that the communication operation, registers configuration and data interchanges (read/write functions) have worked in accordance to their purposes and specifications.

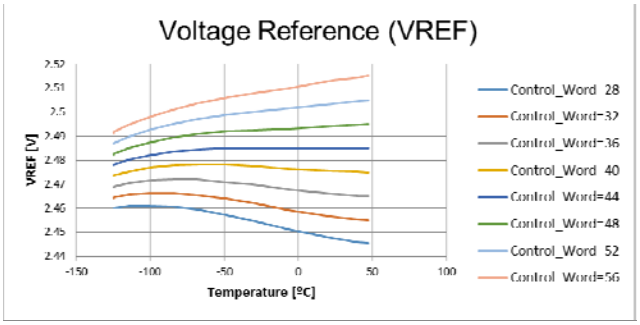

Figure 6: Voltage reference (VREF) evolution with temperature and control word

IV. Conclusions

A Mixed-Signal ASIC (SIS20) in a standard CMOS 0.35mm technology has been presented. It has been designed for an instrument aimed to measure Solar Irradiance on the surface of Mars (expected flying with the ExoMars2020 mission). The design has been carried out using the rad-hard library developed at the Institute of Microelectronics of Seville (IMSE). The main blocks composing the ASIC and their functionality have been briefly described.

The functional operation and technical specifications have been verified in the lab for the specified range of temperature (-125ºC to 50ºC). The qualification of the ASIC is still pending. However, it is expected to be satisfactory attending previous experiences on ASICS of the same characteristics and designed in the same technology using RHDB techniques and the same rad-hard library [5].

Acknowledgment

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Multi-Channel Preamplifier IC for IR-Sensor and FPA Readout

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Abstract

The IDE1060 is an integrated circuit (IC) with 34 preamplifiers for reading out infrared (IR) sensors and focal-plane imaging arrays (FPA). We designed the circuit under contract with the European Southern Observatory (ESO) where the device shall be used with typical large-format astronomical IR sensors, *e.g.*, Raytheon Aquarius and Teledyne HAWAII-2RG. The IDE1060 is intended to replace the fast readout amplifiers described in [1]. The circuit is designed for extreme environmental conditions: cryogenic to room temperature, latch-up immunity and high energy threshold for single event upsets from ionizing radiation. We expect the circuit to be suitable for space-borne astronomical instruments as well. The device has been manufactured by AMS, and the characterization is planned for this year.

I. Introduction

A. ASIC Requirements and Applications

The requirements for the application specific integrated circuit (ASIC) are derived from the needs in terrestrial IR astronomical instruments. Low noise and operation at cryogenic temperatures are among the most important requirements for this application. In addition, the circuit was designed for space applications, requiring special design measures for latch-up immunity and single-event mitigation. The ASIC covers a wide range of different detectors and it is suitable for both cryogenic and space applications.

B. Design Heritage

The operational amplifier architecture used in the IDE1060 has been used successfully in previous IDEAS products: IDE3466 [2] and IDE3380 (SIPHRA) [3].

II. ASIC Design Specifications

A. Block Diagram

Figure 1 shows a block diagram of the sensor readout circuit IDE1060. The IC contains 34 identical preamplifier channels with input signals `IN[1:34]` and `REF` and differential output signals `OUTP[1:34]` and `OUTN[1:34]`. The channel gain is programmable in 8 steps from 2 to 16 (6dB to 24dB) using `GAIN[2:0]`. Each channel consists of two operational amplifiers (OA), a programmable resistive network and switchable capacitors that can be used to reduce the video channel bandwidth to about 3MHz using `BW-SWITCH`. The differential channel outputs can drive large capacitive loads of several hundred pF. The bias currents for the amplifiers are generated on-chip using an external bias resistor connected to `RBIAS`.

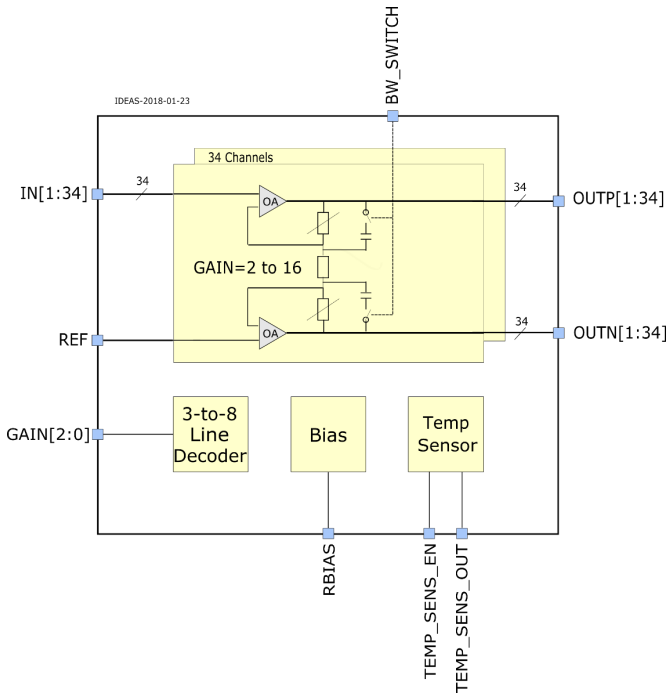

Figure 1: Block diagram of the IDE1060.

B. Key Features

Table 1 summarizes the key features of the IDE1060. The 34 differential voltage-amplifying channels have a programmable gain in 8 steps from 2 to 16 (6dB to 24dB). The differential channel outputs can drive long cables with several hundred pF of capacitance or used with external operational amplifiers and resistors to form classical three-amp instrumentation amplifiers. In addition, the chip contains one standalone amplifier that can be configured externally for different applications or debugging purposes. The chip also provides a temperature sensor. The IC operates at a nominal supply voltage of 3.5V and dissipates about 20 mW per channel at 77K. Various power-down modes are available for applications with less than 34 channels. The IDE1060 is latch-up immune and SEU-tolerant. The IC has been designed in a 0.35-μm CMOS process, and is available as bare die or in a ceramic QFP208 package.

Table 1: IDE1060 key features.

34 differential voltage amplifiers
Programmable gain, 6dB to 24dB 8 settings: 2, 4, 6, 8, 10, 12, 14, 16
Input-referred voltage noise 4.3nV/$\sqrt{\text{Hz}}$ at 10kHz, 6dB, 3.5V, 77K 33μV_{rms} at 1Hz to 50MHz, 6dB, 3.5V, 77K
>50MHz bandwidth at 6dB, 3.5V, 77K, 200pF load
<80ns settling time (0.01%) at 6dB, 3.5V, 77K
2V peak to peak max input swing at 6dB
Rail-to-rail output swing
Single supply voltage 3.3V to 3.6V
Operating temperature cryogenic operation (77K) with R(RBIAS)=174kΩ room temperature (298K) with R(RBIAS)=TBD
Latch-up immune, high threshold for single event upsets
On-chip temperature sensor
Power consumption 20mW per channel at 3.5V and 77K Several programmable power-down modes

1) Channel

A simplified view of one channel is shown in Figure 2. The channel consists of two operational amplifiers (OA) in a balanced non-inverting amplifier configuration with programmable gain. The input signal is applied to IN and a constant reference voltage is applied to REF. The differential output signal can be measured between OUTP and OUTN. The switchable capacitors for video-channel bandwidth reduction are not shown in the figure below.

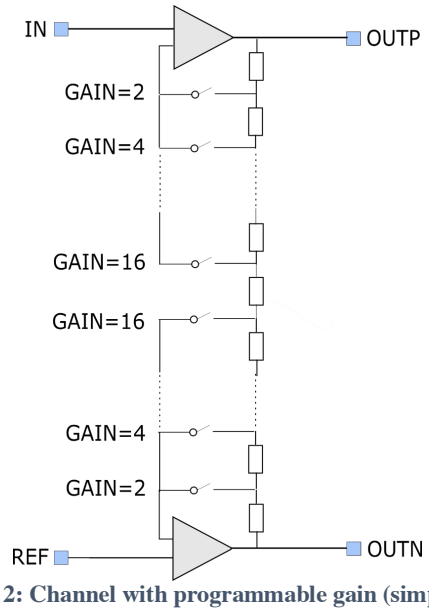

Figure 2: Channel with programmable gain (simplified).

2) Operational Amplifier

Figure 3 shows a simplified schematic of the operational amplifier. The amplifier consists of a folded-cascode input stage and a class-AB controlled output stage [4]. The architecture of the amplifier resembles the simplified schematic shown in the datasheet for OPAx350 [5], which is the amplifier used in the latest revision of the cryogenic preamplifier circuit described in [1]. Since the lowest gain in our application is specified to be 2, a rail-to-rail input stage consisting of parallel PMOS and NMOS differential input stages is not needed. Thus, the class-AB OA has an NMOS-only input stage, which has the advantage of lower input capacitance and less noise and does not suffer from input crossover distortion, a phenomenon commonly observed in rail-to-rail input stages when both input pairs are active.

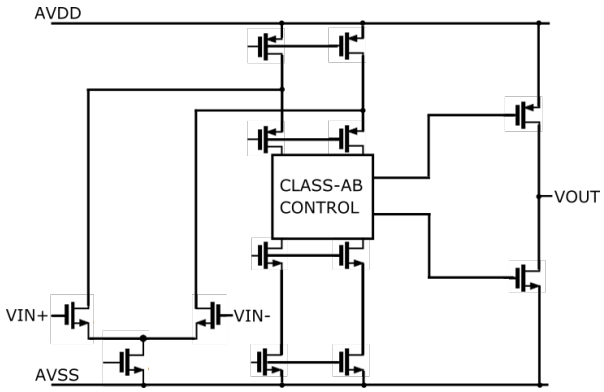

Figure 3: Simplified schematic of the class-AB operational amplifier.

III. ASIC LAYOUT

Figure 4 shows the layout of the chip. The active area is 5.62 mm x 11.64 mm. The area is relatively large, and half of the size is used for routing the output lines. The chip could be designed much smaller depending on package requirements. The IDE1060 has been designed in a 0.35-μm CMOS process and has been manufactured by AMS. All inputs are protected against electrostatic discharge (ESD).

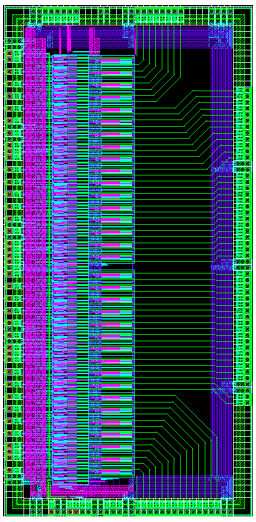

Figure 4: ASIC layout.

IV. ASIC Design Verification

The IC has been designed and verified using Cadence Virtuoso, Spectre, Assura DRC and LVS. All simulations have been run across corners (AVDD=3.3V-3.6V, process variation and Temp=77K-300K). The results shown in this chapter focus on the performance at 77K. Simulation results for both the operational amplifier and for a complete channel will be presented in this chapter.

A. Operational Amplifier

1) DC Characteristics

The typical quiescent current consumption of the operational amplifier is 2.77mA at 77K.

Table 2: Op-amp quiescent current consumption at 77K.

Min [mA]	Typ [mA]	Max [mA]
1.49	2.77	5.79

2) AC Characteristics

Figure 5 shows the open-loop alternating current (AC) frequency response of the operational amplifier at 77K. There are two ordinates: to the left is the output amplitude V from -50dB to +120dB and to the right the phase margin (PM) from -280 to +20 degrees. The abscissa is the frequency from 1Hz to 1GHz. From the figure one can obtain the direct current (DC) gain of 110.6dB and the unity gain-bandwidth (UGBW) of 84MHz with a phase margin (PM) of 63.5° for the nominal load capacitance of 200pF. The corner simulation results for 77K are listed in Table 3.

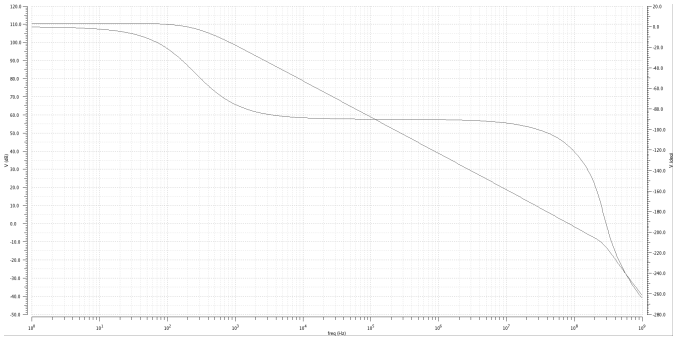

Figure 5: Frequency response of the operational amplifier.

Table 3: Op-amp DC gain, unity-gain-bandwidth (UGBW) and phase margin (PM), load=200pF at 77K.

Parameter	Min	Typ	Max
DC gain [dB]	104.5	110.6	115.8
UGBW [MHz]	59.2	84.0	119.0
PM [deg]	47.7	63.5	70.9

Figure 6 shows the power-supply rejection ratio (PSRR) of the operational amplifier with a capacitive load of 200pF as a function of frequency at 77K. The PSRR is 106.3dB at 1Hz and still 25.0dB at 10MHz. The corner simulation results for 1Hz at 77K are listed in Table 4.

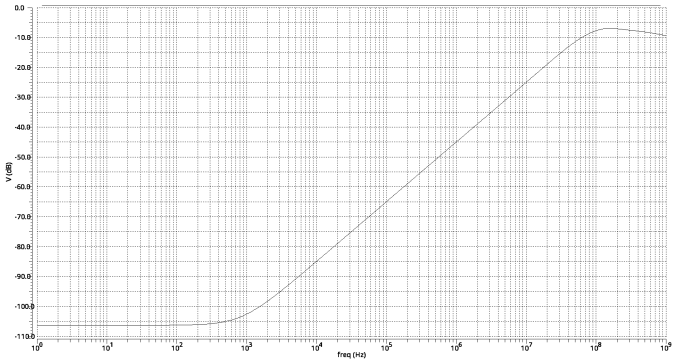

Figure 6: PSRR of the operational amplifier vs frequency.

Table 4: Op-amp PSRR at 1Hz [dB], load=200pF at 77K.

Min [dB]	Typ [dB]	Max [dB]
92.5	106.3	109.2

The input-referred noise of the operational amplifier has been simulated in a unity-gain configuration. Table 5 summarizes the corner simulation results for integrated input-referred noise and spot noise at a frequency of 10kHz at 77K.

Table 5: Op-amp input-referred noise at 77K.

Gain	Integrated (1Hz to 500kHz) [μVrms]	Integrated (1Hz to 50MHz) [μVrms]	Spot noise (f=10kHz) [nV/$\sqrt{}$Hz]
1	1.0	16.7	1.8

3) Transient Characteristics

Figure *7* shows the step response of the operational amplifier in a non-inverting configuration with gain=2 at 77K. The typical slew rate is 47.2V/μs and the settling time to within 0.01% of the final value is 72ns. The corner simulation results for 77K are listed in Table 6.

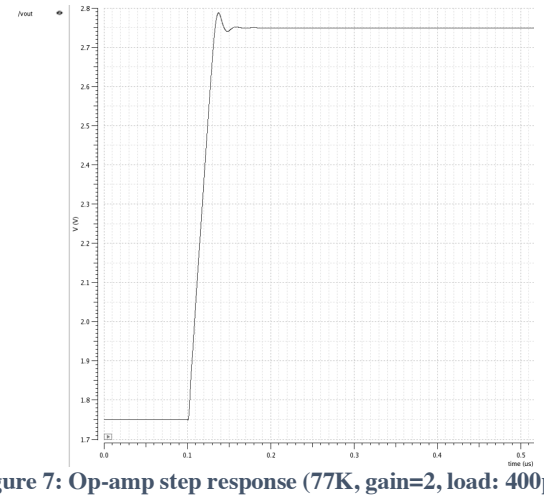

Figure 7: Op-amp step response (77K, gain=2, load: 400pF).

Table 6: Op-amp slew rate and settling time (77K, gain=2, load 400pF).

Parameter	Min	Typ	Max
Slew rate [V/μs]	37.6	47.2	61.4
Settling time (0.01%) [ns]	56.4	72.0	91.5

B. Channel

1) Channel Noise

Low input-referred noise is among the most important design requirements for the IDE1060. Table 7 summarizes the corner simulation results for integrated input-referred noise and spot noise of a complete channel at a frequency of 10kHz at 77K using four different gain settings.

Table 7: Channel input-referred voltage noise (77K, 3.5V).

Gain	Integrated noise (1Hz to 500kHz) [μVrms]	Integrated noise (1Hz to 50MHz) [μVrms]	Spot noise (f=10kHz) [nV/√Hz]
2	2.8	33.2	4.3
4	2.5	30.8	4.0
8	2.1	27.6	3.5
16	1.8	25.6	3.1

2) Channel Bandwidth and Gain

Figure 8 shows the differential output signal of the channel for eight different gain settings from 2 to 16 at 77K. A 100-kHz sinusoidal signal with an amplitude of 100mV is applied to IN, while a constant voltage of AVDD/2 is applied to the reference input.

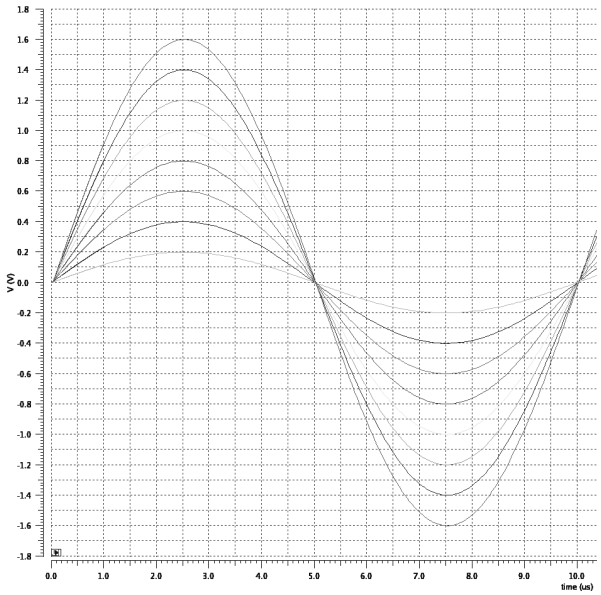

Figure 8: Differential output signal for GAIN=2 to 16 (input signal amplitude: 100mV, frequency=100kHz) at 77K, AVDD=3.5V.

Figure 9 shows the cut-off frequencies of the channel for different gain settings at 77K.

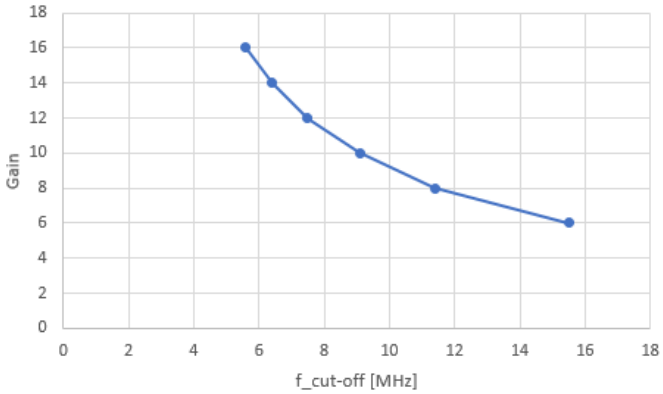

Figure 9: Gain setting vs cut-off frequency at 77K, AVDD=3.5V.

V. ASIC CHARACTERIZATION

The IDE1060 will be packaged in a ceramic 208-pin quad flat pack (QFP) package and mounted on a test board. For specification compliance tests, external signal sources will be connected directly to the test board. For the final tests, comparing the new preamplifier solution with the original design, an HAWAII2RG detector will be placed in the cryogenic chamber and connected to the test board. All tests will be carried out in the cryogenic chamber under vacuum conditions at 77K. Figure 10 shows a photograph of the cryogenic chamber in our lab. A chip is mounted on the circuit board inside the chamber.

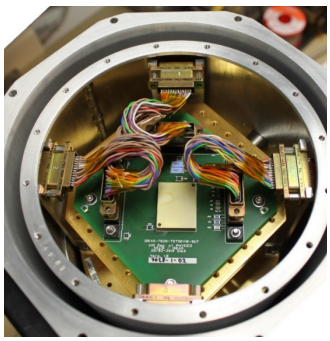

Figure 10: Test board in cryogenic chamber.

VI. SUMMARY

We have designed a 34-channel preamplifier circuit with programmable gain for readout of infrared sensors and focal-plane imaging arrays in cryogenic and space applications. The video-channel bandwidth and the number of active channels can be selected by the user. Simulation results for both the standalone amplifier and for a complete channel have been presented. The circuit has been designed using a 0.35-μm AMS CMOS process. Samples will be available in Q3 2018.

VII. ACKNOWLEDGEMENTS

The authors would like to acknowledge the support from the European Southern Observatory.

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Channeltron Detector Readout ASIC in 0.35µm HV CMOS for Cold Solar Wind

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Abstract

Low-power analog front-end circuits for channeltron detectors (or Channel Electron Multiplier: CEMs) have been fabricated in 0.35-µm CMOS technology to characterize low energy solar wind particles. They have been designed to readout signals for incident charges ranging from 50 fC to 20 pC. Each front-end circuit consists of a charge preamplifier, an amplifier, a discriminator, a monostable circuit and an LVDS driver. Requirement on the complete front end is to consume less than 6.5 mW/channel for a maximum event detecting rate of 40 MHz.

I. INTRODUCTION

THOR (Turbulence Heating ObserveR) is a microsatellite aimed to investigate the fundamental theme "turbulent energy dissipation and particle energization". It embarks among other instruments CSW instrument (Cold Solar Wind) which is primarily dedicated to the study of solar wind turbulence at the ion scale. The He++ solar wind population will be measured within the energy range of [20 eV/q – 20 keV/q]. To fulfil the requirements, the CSW instrument can be divided into two main units: the detector unit and the electronics unit. Our work is part of the detector unit comprising of a deflector, a collimator and a top-hat electrostatic analyser. Through this analyser, the energy-per-charge selected ions are focused onto the main detection plane consisting of 32 channel electron multipliers (CEMs) or channeltrons. The CEMs' output charge (approximately 107 electrons) is collected and read-out by two 16-way ASICs for signal processing and discrimination. A prototype of the front-end circuit is presented here. It consists of three ways of achieving the required performance: "cluster A", "cluster AB" and "cluster RAB". Each one of the design has been characterized electrically on a test board.

II. CEM DETECTOR READOUT ARCHITECTURE

The incoming charges provided by the CEM detector is firstly integrated in a charge sensitive pre-amplifier (CSA) and then further amplified without being "shaped" for "cluster A and "cluster AB" designs. The following signal processing consists of binary readouts based on comparators that detects the incoming particle if the amplified output signal amplitude is above a pre-set threshold [1], it is then followed by a monostable and finally an LVDS output driver.

Table 1: ASIC specifications

Parameter	Value	Unit
Power / per channel	<6.5	mW
Power supply	3.3	V
Input Charge	[0.05 – 20]	pC
Linearity range (fC)	50 to 800	fC
ENC	12.5	fC
Input Parasitic Capacitance	10	pF
Radiation with 3mm Aluminium	30	krad

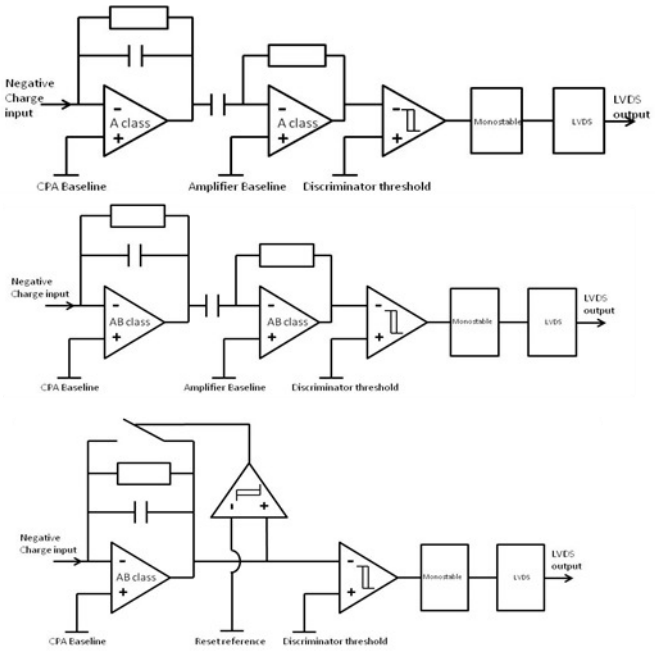

Figure 1:Front End simplified schematic: (a) cluster A, (b) cluster AB and (c) cluster RAB.

Here, the targeted maximum operating frequency is 40 MHz (which corresponds to detect one event every 25 ns) while consuming less than 6.5 mW/channel. Table 1 summarizes the main required performances.

A. CEMs Analog Front end architectures

Due to the low power and high-speed requirements, as previously mentioned, three different architectures were designed: "cluster A", "cluster AB" and "cluster RAB" (see

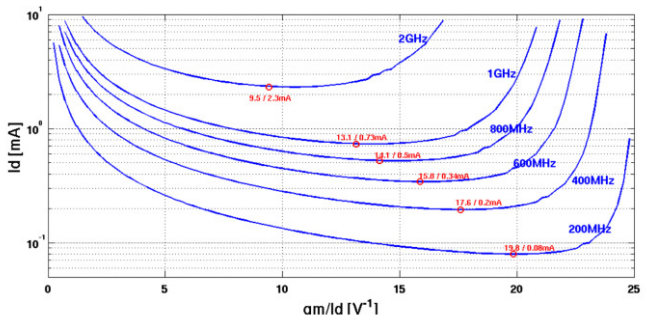

Figure 2:Power optimization of an ideal common source for different GBW in AMS 0.35µm

Fig. 1). They were named according to the amplifier operating class, either A or AB. The cluster A relies on a conservative design which is used as reference for the cluster AB and RAB. Cluster RAB stands for Reset AB, this design makes use of a reset scheme at the CSA level.

Note that the class A provides the lowest noise while the class AB the lowest power consumption. In addition to further reduce the power consumption and achieve higher speed, the pulse shaper stage has been replaced by an amplifier stage for the cluster A and AB while it is not necessary in the cluster RAB.

B. CSA architectures

All the channels make use of a RC CSA for integration of the input charge. The CSA is based on a transconductance amplifier (OTA) with a feedback capacitor C_f to perform the charge integration and a resistor feedback R_f to discharge C_f and to provide a DC path for the detector leakage current. Such a differential approach improves the rejection of common mode external noise. In addition, based on the methodology extensively described in [1], sizing as well as biasing of the transistors are optimized for internal noise and bandwidth performance. The feedback R_f and C_f values depend on the required time constant.

One of the challenging requirement is on the pulse repetition rate at 40 MHz (every 25 ns) while the input event may last up to 13 ns. The electronic needs to be fast enough to closely follow the rise of the current input pulse. It also needs to limit its discharge time to be quickly ready for the next pulse. In addition, the dynamic range spanning from 50 fC to 20 pC, it becomes essential to limit any overshoot of the signal especially at 20 pC input charge as the overshoot would be treated as an incoming small event.

The gain bandwidth product has been evaluated to be no less that 600 MHz [2] and the chosen approach for a fast recovery time is to limit the integration time ($R_f.C_f$) to 1 ns, this value proves to be a good compromise between gain loss and recovery speed at the CPA output.

In order to have a good estimate of the minimum required power consumption to achieve such performances, an approach based on the gm/Id methodology has been used [3]. From the intrinsic gain stage of a common source transistor with an ideal active load and a capacitive loading C_L, power optimisation versus gain bandwidth product can be estimated as shown in Fig. 2. It clearly shows that to achieve a 600 MHz gain bandwidth product, the lowest current biasing should be around 0.34 mA.

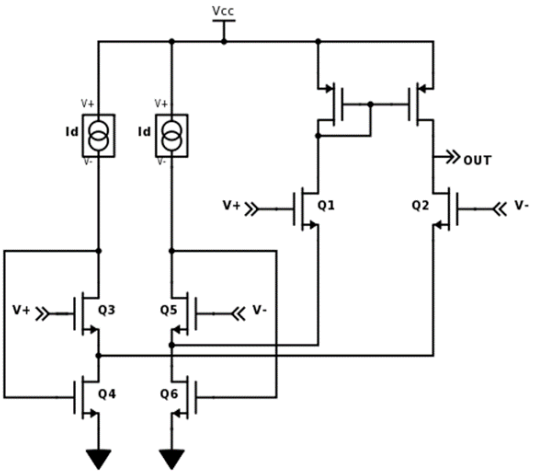

Figure 3: Schematic of CPA class AB operational amplifier

Another consideration is the input dynamic range: a 20-pC input charge over 13-ns duration leads to a peak current of approximately 2.5 mA. Power consumption for class A CSA is thus driven by the maximum input charge constraint.

The CSA amplifier is a first order amplifier consisting of one OTA stage only, this ensures no overshoot of the signal at CSA output and limits the power consumption to the bare necessity. The conservative “cluster A” channel makes use of a conventional class A amplifier while class AB amplifiers are used to boost up the performances without being constrained by the maximum input charge for the quiescent current for “cluster AB” and “cluster RAB” channels. Super class-AB OTAs with adaptive biasing have been designed to provide a dynamic output current scaling [4] (Fig. 3).

To further reduce power consumption, cluster RAB forces the discharge of C_f before signal saturation. This allows making even more power efficient design choices. Above a given signal amplitude, the discharge takes place using a reset. As a result, the CSA does not need to remain linear for high value input charges and does not need another amplification stage as it is the case for the previous two designs.

C. Amplifiers design

At the output of cluster A and cluster AB CSA, 50-fC charge output signal is as small as a few mV only. In order to be detectable using a threshold tunable discriminator, it becomes essential to amplify the signal to a reasonable level.

An accurate amplification is not necessary in our case; the open loop gain is used in order to maintain a good tradeoff in power consumption versus gain.

D. Discriminator and Monostable design

The discriminator is a regular comparator with about 10mV of hysteresis in order to avoid switching on noise.

The monostable is a retriggearable monostable. The output pulse duration is tunable. The circuit is made retriggearable in case a second event occurs during the pulse duration.

E. Layout considerations

The circuit has been implemented in AMS 0.35µm HV CMOS technology. This technology has a triple well option allowing isolation of transistors from the bulk. This is an advantage in terms of noise and crosstalk reduction and allows to improve its robustness regarding Single Event Latchup (SEL). To further reduce crosstalk, power supply of the analog part of the channel is isolated from the discriminators (comparators, monostable) and LVDS outputs. A microphotograph of the chip layout is shown in Figure 3.

A total of 9 channels are integrated in the chip: 3 channels per cluster type to check cross-talk effects.

III. ASIC CHARACTERIZATION

A. Simulation Results

In order to assess the robustness of the readout circuits, the charge injection worst case consisting in successive 50 fC and 20 pC charge injections at the highest 40 MHz rate, has been simulated. Fig.5 shows that after a 20-pC charge injection, the system can still detect a 50 fC charge injection.

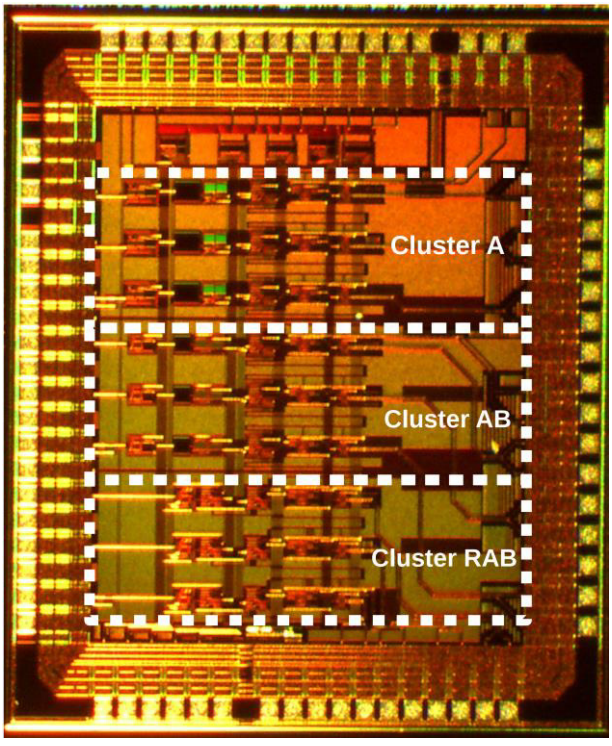

Figure 4: ASIC microphotograph

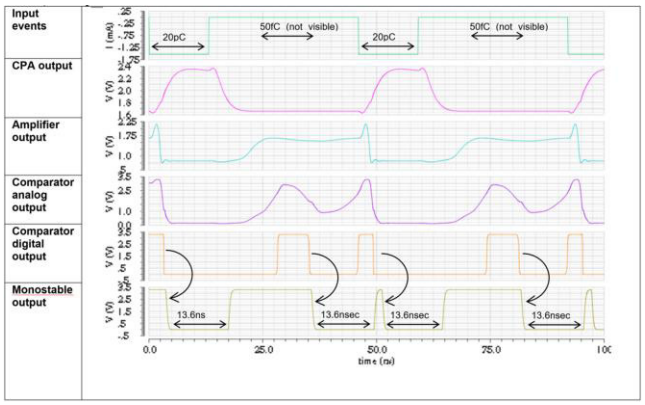

Figure 5: Simulation of successive 50 fC and 20 pC charge injections at a 40 MHz rate for cluster AB design

For CEM calibration purpose, detection linearity is required up to 800 fC. Fig.6 shows the linearity of the system within [50 fC – 800 fC] as well as a 1.2 V/pC sensitivity.

B. Measurements

The ASIC has been electrically characterized on a test board (Fig.7). A 1-nF injection capacitance driven by a signal generator has been used to generate the input charge. The ASIC input is loaded by a 10-pF capacitance representing the parasitic capacitance of the detector with its ESD protections.

One of the measurement consists in checking the ability of the readout circuit to count up to a 40 MHz without suffering from pile up issues. Due to the current test bench, it has only been possible to perform 50 successive incoming charges of maximum 2 pC at a rate of 40 MHz. This test results points clearly out that the cluster A and AB successfully detect all the events (Fig. 8).

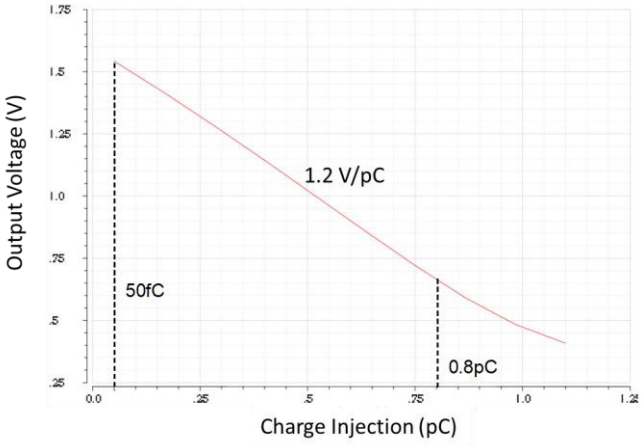

Figure 6: Simulation of the output voltage of the analog front-end readout circuit versus the input charge injection

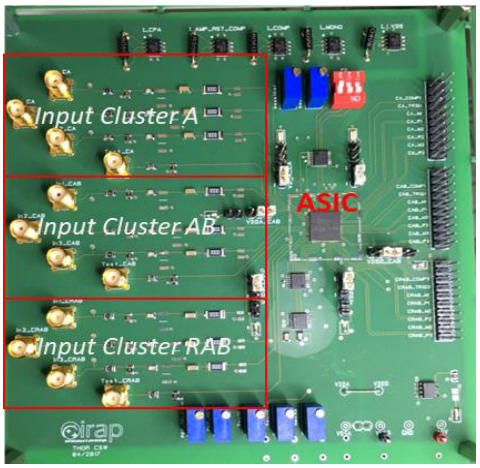

Figure 7: ASIC test board

Finally, the Table 2 summarizes the measurement results.

Table 2: Measurement Results

Parameter	Spec	Cluster		
		A	AB	RAB
Power (mW)	<6.5	14.5	6.25	4.2
Qmin (fC)	50	50	60	50
Qmax (pC)	20	>20	>20	>20
Linearity range (fC)	50 to 800	50 to 1100	60 to 1000	50 to 2000
Frequency (MHz)	40	40	40	20

IV. CONCLUSION

A CEM detector readout ASIC for Cold Solar Wind has been presented. Two of the designs ("A" and "AB") feature double separation pulse of 25 ns for input charges spanning from 50 fC to 20 pC for a 10 pF input parasitic capacitance. Power consumption are 14.5 mW and 6.25 mW per channel for each design. The last design "RAB" consumes 4.2 mW per channel for a detection rate of 20 MHz only.

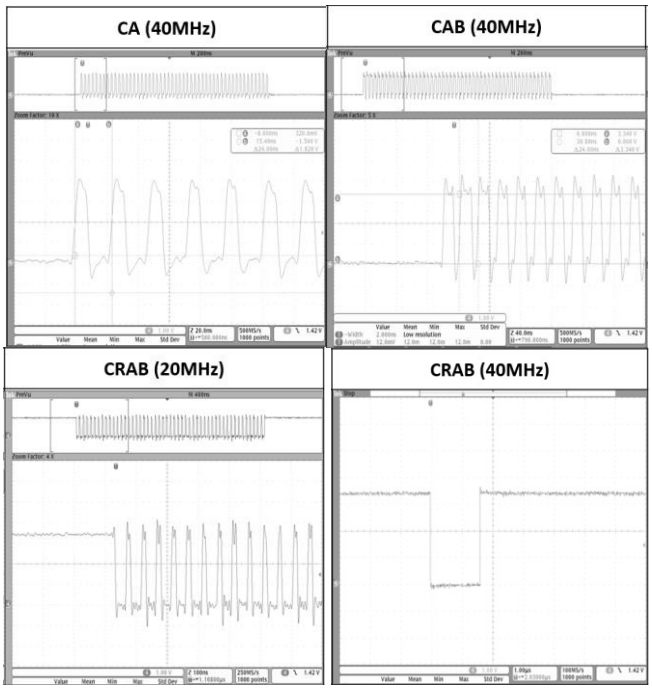

Figure 8: Comparator output corresponding to 50 successive incoming charges of 2 pC at 40 MHz rate for clusters CA and CAB and at 20 MHz and 40 MHz rate for cluster CRAB

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A rad-hard system-on-chips solution for closed-loop motion control

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Abstract

This paper describes the design and implementation of a system-on-chips solution for closed-loop control of remote-handling robotic tools in radiation environment. Five ASICs have been designed in two commercial CMOS technologies (DARE350ON and DARE65T [1]), including a resolver or LVDT to digital converter, a resistive bridge sensor signal conditioner, a 24V/48V 10-channel limit switch conditioning IC, a 24V/48V10-channel low-side driver IC, and a BiSS-based communication ASIC. Several rad-hard and silicon-proven Analog/Mixed-signal IPs on the 65nm CMOS technology have also been developed, e.g., ADC, PGA, LDO, Clock generator, Voltage reference, and PLL.

Radiation-hardened-by-design (RHBD) techniques are used in the design of the ASICs to achieve TID tolerance of more than 1 MGy (100 Mrad) and SEL/SET/SEU hardness of higher than 60 MeV•cm^2/mg.

I. Introduction

The original intended application of the development is for remote handling equipment at ITER (a first-of-kind Tokamak fusion nuclear plant). In order to reduce the number of cables inside the equipment and from the deployment area to their cubicles placed at about 150m distance, front-end acquisition, actuation and digital transmission electronics have to be located close to sensors and actuators on ITER remote handling maintenance systems. Front-end electronics face gamma radiation up to a total dose of 100 Mrad, and total neutron fluence up to 10^{15} n/cm^2. Hence those electronics are required to be radiation-hardened against total-ionizing-dose (TID) radiation, as well as single-event effects (SEE) caused by neutrons (14 MeV). In order to broaden the application scope of the system, the chips were also designed to be resistant against higher energy particles (e.g., >60 MeV protons and heavy ions).

A typical closed-loop position sensing and motion control system involves the following sensor/actuator types:

- Position sensors (resolvers, LVDTs, IMUs)
- Resistive bridge sensors (thermocouples, potentiometers, load-cells, strain gauges, magnetic sensors)
- Limit switches
- Relays (both mechanical and solid-state)
- Motors

In many remote handling equipment applications, a fieldbus is required to connect all sensors and some digital (ON-OFF) actuators to a motion controller while motors actuators are directly cabled to their drives in order to form a real-time, deterministic control loop. In this development, the BiSS-interface (bidirectional/serial/synchronous) is used as the fieldbus protocol. The BiSS-interface is an open-source protocol. It is based on a protocol which implements a real time interface. It enables a digital, serial and secure communication between controller, sensor and actuator. The BiSS protocol is designed in B mode and C mode (continuous mode). It is used in industrial applications which require transfer rates, safety, flexibility and a minimized implementation effort. The BiSS interface physical layer is defined as either RS485 (10 Mbps) or LVDS (100 Mbps). The BiSS interface employs a synchronous method for data transmission, therefore, the overhead (Flag bits + CRC) of the protocol can be minimized, comparing to other fieldbus protocols (e.g., CAN, EtherCAT, and Profibus).

Finally, five system-on-chips have been developed for the closed-loop control system, which are:

- ASIC1: a resolver/LVDT to digital converter that reads out angle information from a resolver or linear distortion information from a LVDT;
- ASIC2: a resistive bridge sensor conditioner to read out RTDs, thermocouples, and strain gauges;
- ASIC3: a 10-channel limit switch conditioning IC to readout the on/off status of 24V/48V limit switches;
- ASIC4: a 10-channel low-side driver chip to drive 24V/48V mechanical/solid-state relays;
- ASIC5: a bus communication ASIC including the BiSS-interface [2] protocol controller, the SPI master protocol controller, and on-chip RS-485 bus transceivers.

The potential space applications of the closed-loop motion control system could be:

- Control of remote handling manipulators and remote operated vehicles;
- Speed control of reaction wheels;
- Control of electrical propulsion system;
- Altitude control of satellites;
- Control of electrical valves.

In the following sections, more details about the ASIC's functionalities and designs are described. Technical specifications of several Analog/Mixed-signal Intellectual Property (IP) cores on the 65nm CMOS process will also be given, as well as applied radiation-hardened-by-design techniques.

II. ASIC DESCRIPTION

A. Resolver/LVDT to digital converter

ASIC1 is a Resolver/LVDT to digital converter, which is designed to readout the angular information from a resolver or the linear distortion information from a LVDT. A digital control bit is used to switch between the two functions. A block diagram of the ASIC1 is shown in Figure 1.

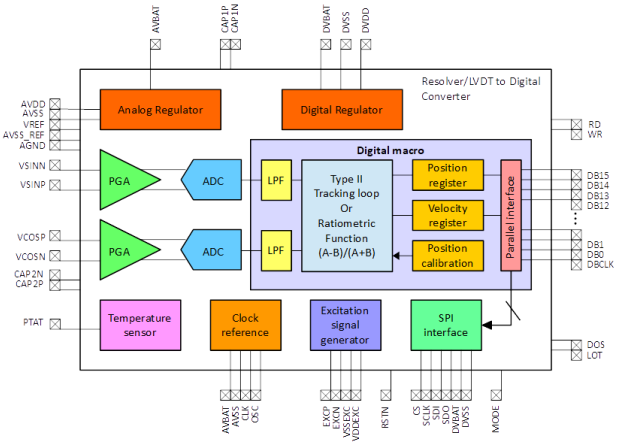

Figure 1: Block diagram of the resolver/LVDT to digital converter

The resolver is read by digitizing both signals coming from the resolver secondary windings (Vcos and Vsin) by the signal conditioning circuits (PGA and ADC) shown in the figure. The output signals of two delta-sigma ADCs are first streamed to two identical digital low pass filters (LPF), which removes high-frequency quantization noise from the ADC output. The Filtered ADC signals are then fed into a digital tracking loop where the angular calculation is performed. The results are kept in the position and velocity registers, accordingly.

An excitation signal generator provides a sine wave signal to the primary winding of the resolver or the LVDT. However, a typical resolver/LVDT requires a low-impedance 3-Vrms to 7-Vrms signal to drive the primary winding. Operating with a 1.2V supply, the RDC can only deliver a 1.8V peak-to-peak differential signal on the excitation outputs. This signal might not have sufficient amplitude and drive capability to meet some resolver/LVDT's input specifications. A solution to this problem is to use an off-chip amplifier to amplify the sinusoidal signal sent to the primary winding. A digital format of the excitation signal is needed by the tracking loop for demodulating the sin/cos signals, which will be generated by the on-chip reference.

An example of system-level integration of the ASIC1 is shown in Figure 2. In total five off-chip capacitors would be required. Two of them are used for stabilizing the on-chip power regulators, and the other three are needed by the Analog-to-digital converter.

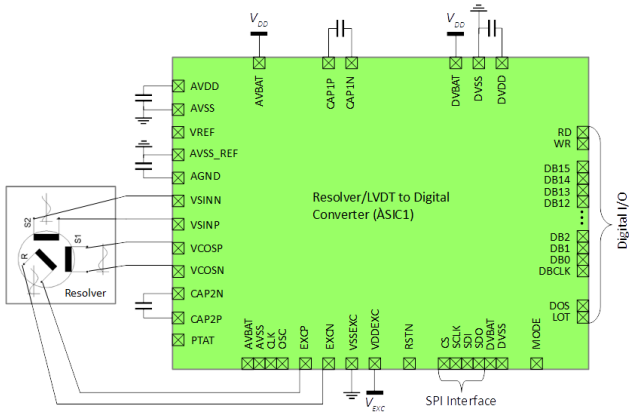

Figure 2: System integration of ASIC1

Major specifications of the ASIC1 are listed in Table 1.

Table 1: ASIC1 Electrical Specifications

Specifications	Unit.	Typical
Supply voltage	V	1.2
Power consumption	mW	20
Resolution	bits	16
Accuracy	arc min	3
Bandwidth	Hz	800
Tracking rate	rps	500
Excitation frequency	kHz	2.5
SPI data rate	Mbps	10

B. Resistive bridge sensor conditioner

ASIC2 is a generic signal conditioning circuit for reading out sensors such as RTD, thermocouple and strain gauge (as shown in Figure 3). An RTD or strain gauge converts a physical value (temperature or pressure) to a variable resistive value. A Wheatstone bridge circuit is often used to measure a variable resistance with great accuracy. The output of a bridge circuit is a small voltage signal, which needs to be amplified by a low-offset, programmable-gain instrumentation amplifier. After the amplification, an ADC converts this signal into a digital bit stream. The same signal conditioning circuit can also be used to readout a thermocouple temperature sensor. However, in this case, a second signal conditioner will be required to readout a reference temperature at the cold junction, which could be done by employing the on-chip silicon temperature sensor.

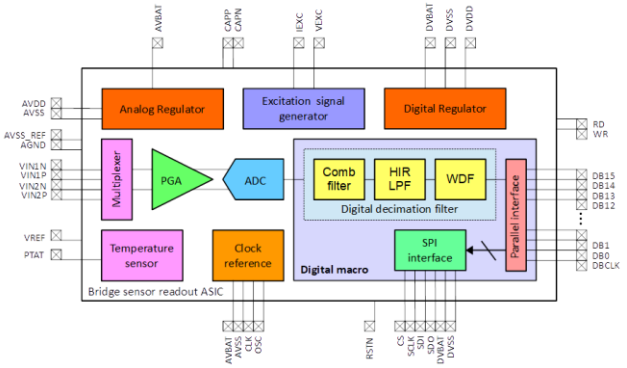

Figure 3: Schematic of the resistive bridge sensor conditioner

A multiplexer with two differential inputs can be used to connect multiple sensors to the same signal conditioning circuits. Furthermore, a clock reference provides the timing signal for the ADCs and all other digital processing blocks. A low-dropout voltage regulator (LDO) is employed to provide supply voltages for all functional blocks. A serial peripheral interface (SPI) is used here to communicate the output results. The DC excitation voltage for the bridge circuit can also be generated from the ASIC.

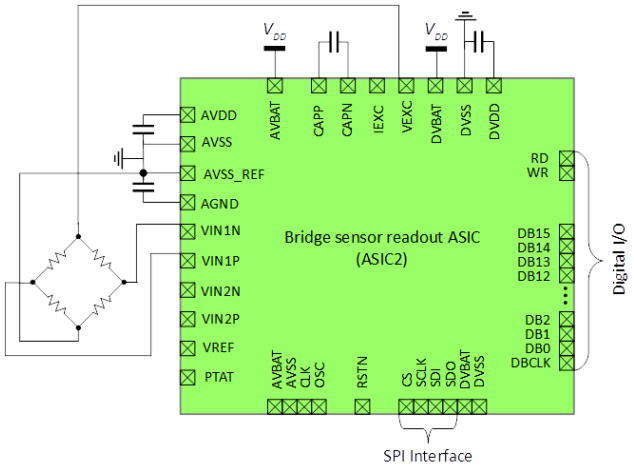

Figure 4: System integration of ASIC2

An example of system-level integration of ASIC2 is shown in Figure 4, and major specifications of the ASIC2 are listed in Table 2.

Table 2: ASIC2 Electrical Specifications

Specifications	Unit.	Typical
Supply voltage	V	1.2
Power consumption	mW	10
Gain range		1 ~ 256
Gain offset	%	2
Gain error	%	±0.5
Bandwidth	Hz	2.5k
Gain drift	ppm/°C	10
Offset drift	nV/°C	10
Input noise	nV/√Hz	35
Offset	µV	5
ADC resolution	bits	16
Excitation voltage	Vdc	1.2
Excitation current	µA	200
SPI data rate	Mbps	10

C. *Limit switch conditioning IC*

The ASIC3 consists of 10 individual sensing channels. Each of them capable of reading the status of the limit switch connected to it. They are all identical and are a cascading of several level shifters to translate the high voltage output signal of the limit switch to a low 3.3V domain.

The status of the limit switches can be read out via SPI or parallel interface. If the parallel interface is used only 5 of 10 channels at the same time can be read out. The parallel interface is mainly used for test. A readout of the status of all channels at the same time can be done via SPI interface.

The ASIC is designed in such a way that the limit switch needs to be on the high side (see Figure 5). The high output voltage of a limit switch (24V/48V) first needs to be down shifted to a lower level. This is done by a resistive divider. To make the design ESD proof, it is necessary to put the upper resistor of this divider off chip.

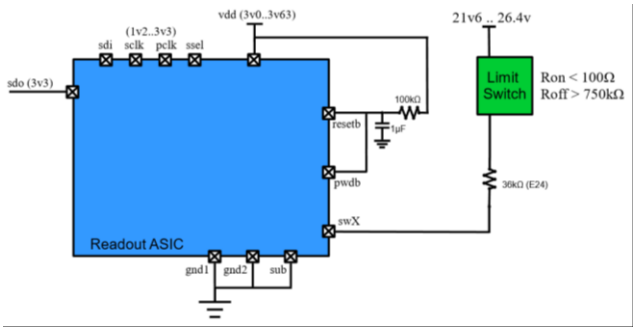

Figure 5: System-level integration of the limit switch conditioning IC

D. *10-channel low-side driver IC*

The ASIC4 consists of 10 individual driver channels. Each of them capable of sinking 130mA through a low-side switch from a high voltage supply of 24V/48V at a maximum switching frequency of 17kHz.

Each of the 10 driver channels has a built-in protection mechanism by means of an over-temperature detection (OTD) and over-current detection (OCD). Those detection blocks can instantly shut down the driver channel in case of an over-temperature or an over-current event.

The OTD block monitors the temperature of the driver channel nearby the output device. If temperature becomes too high, the specific channel immediately goes in a non-conductive state. When temperature drops again to a safe operation region, the normal operation of the channel is resumed. The OCD block monitors the current through the switch device of the channel. If an over-current situation is detected the driver channel goes immediately in a non-conductive state. The non-conductive state after an OCD event is preserved until a reset pulse is send to the driver channel. This reset pulse comes from the digital macro and needs to be initiated by a SPI command. If the over-current situation still exists after a reset, the driver channel goes back in the non-conductive state.

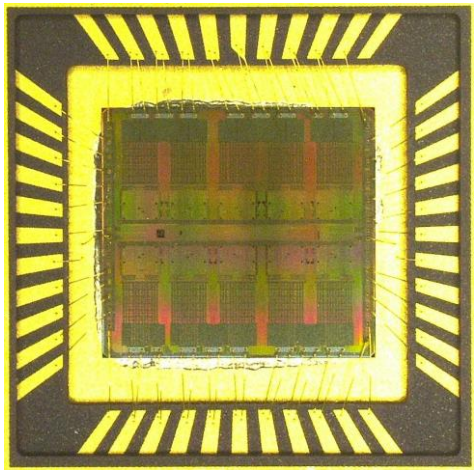

Figure 6: Die photo of ASIC4

To achieve Mrad-level ionizing radiation tolerance, thorough radiation hardness techniques in design and layout are implemented. Also, techniques are used to increase robustness towards SEL and SET/SEU. In design, techniques as triple mode redundancy (TMR), Analog voting and DICE latching are applied. Sizing of all devices is done by simulating them with adapted simulation models to mimic the effect of the ionization. A customized radiation-hardened layout [3] is made for the high voltage output switching DMOS present in every driver channel.

E. Bus communication ASIC

The bus communication ASIC consists of a BiSS-interface controller, a SPI master controller and three RS-485 transceivers. The communication ASIC connects all other four ASICs into the same bus system, as shown in Figure 7. The integrated on-chip RS-485 drivers are capable of transmitting signals over a 150-meter cable at a speed of 5 Mbps. They can handle large ground potential differences along the long communication cable in the bus system. The acceptable input common mode range can vary between -7V up to +7V.

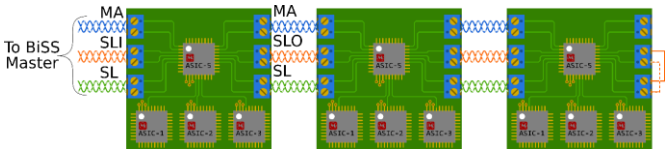

Figure 7: BiSS-interface bus configuration

III. Rad-hard 65nm CMOS Analog/Mixed-signal IP library

Generic rad-hard Analog/Mixed-signal IPs on 65nm CMOS have been developed [4] to enable easier integration of the system-on-chips, including an Analog-to-digital converter (ADC), a programmable gain amplifier (PGA), a clock reference, a bandgap voltage reference, a PTAT temperature sensor, a linear regulator and a Phase-locked loop (PLL). Technical specifications of these IP blocks are summarized in Table 3.

MAGICS Instruments has developed a unique rad-hard IC design environment to achieve high first-time-right rate and high reliability:

- Industrial standard EDA tools: MATLAB for system behavioural model simulation; Cadence Virtuoso design tools for schematic edit, simulation and layout; Cadence Incisive and Innovus for digital design and implementation; Mentor Graphics Calibre for physical verification and sign-off.
- Experimentally verified transistor radiation model for TID (total-ionizing-dose) simulation.
- In-house proprietary TMR (triple modular redundancy) generator and SET simulator for single-event simulation.

The following RHBD techniques are applied in the design of the IPs to improve their radiation hardness:

- use dynamic compensation techniques [5] to mitigate radiation-induced performance drifts;
- use enclosed-layout I/O transistors to reduce radiation-induced leakage currents [6];
- use guard-rings and body contacts to mitigate inter-device leakage and single-event-latchup [7];
- use radiation-aware transistor sizing to limit radiation-induced threshold voltage shift;
- use triplication and voting for all digital circuits to mitigate single-event-upset;
- use averaging and filtering in analog circuits to reduce single-event-transient.

IV. Conclusion

This work presents a rad-hard system-on-chips (SoCs) solution for sensing position, analog and digital signals, and for actuating digital outputs over the BiSS field bus, in order to perform motion control. A SoC integrates an electronics system into one single chip, and requires very few external components, hence significantly reduces the cost and complexity of system-level integration. The deterministic, real-time, low-power, small-size and radiation-hard features of the closed-loop system make it a very suitable candidate for applications in the harsh space and nuclear environment.

Furthermore, the reliable rad-hard IC design environment and the IP library greatly enhance the reproducibility, maintainability, and upgradability of the platform.

V. Disclaimer

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Table 3: Technical specifications of 65nm CMOS rad-hard Analog/Mixed-signal IPs

Programmable Gain Amplifier	**Phase-Locked Loop**	**Analog-to-Digital Converter**
Gain: 1 ~ 256 Gain error: ±0.5% Gain drift: 10 ppm/°C Offset: 5 µV Offset drift: <10 nV/°C Input noise: 20 nV/√Hz TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)	Frequency: 2.2 ~ 3.2 GHz Bandwidth: 0.7 ~ 2 MHz RMS jitter: 350 fs Power: 12 mW TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (silicon proven)	Resolution: 16 bits Bandwidth: 20 kHz SNDR: 96 dBFS Power: 5 mW TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)
Voltage reference	**Clock reference**	**Temperature sensor**
Temperature range: -50 ~ 125 °C Temperature coefficient: 30 µV/°C Power: 80 µW TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)	Frequency: 8 ~ 12 MHz Temperature coefficient: 30 ppm/°C RMS jitter: 25 ps Power: 360 µW TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)	Temperature range: -50 ~ 125 °C Temperature coefficient: 1.5 mV/°C Accuracy: <1 °C Power: 60 µW TID tolerance: >100 Mrad SEL tolerance: >100 MeV·cm2/mg SET/SEU tolerance: >60 MeV·cm2/mg Status: functionality (silicon proven), TID tolerance (silicon proven), SEE tolerance (simulation)

Ultimate earth observation by time delay integration line scan imagers using the CCD-in-CMOS technology

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Abstract

Imec has been developing a combination of CCD and CMOS technology in one process flow. This enables low noise Time Delay Integration (TDI) line scanners including the signal drivers and readout circuit on-chip – which is not possible using CCD imagers. Moreover, multiple TDI sensors can be integrated within a single chip. This, in combination with spectral filters integrated on-chip allows high resolution and spectrally resolved earth observation from low orbit (e.g. micro-)satellites.

I. Introduction

Low orbit earth observation missions have been using line scan imagers using CCD technology for a long time. Today we see an increased activity in the development and launch of very small satellites (cube satellites or nanosatellites) which are used in constellations in order to image the earth with an unpreceded short revisit time. Hence there is a need for highly integrated and miniaturized line scan imagers, capable of both high resolution and spectrally resolved imaging.

II. Time delay integration

Given the linear movement of the satellite in low orbit over the earth, and hence the linear movement of the scene image over the imager, the Time Delay Integration technique can be used. Conceptually one can use a linear array of photosensitive pixels to capture a full 2-dimensional image. In the across track dimension, the image is collected by the number of pixels in the linear array. In the along-track dimension, the image can be captured by sequentially in time taking the data of the linear array, in such a way that the time delay is exactly matching with the linear movement of the scene. In other words, one takes an image line by line delayed in time, synchronized with the linear scene movement.

An optimized way of capturing a 2-dimensional image, is not to use a single row of photosensitive pixels but a number of rows. Each of this rows detects the same scene information but delayed in time for each row. In practice the second row takes the same across-track line image as the first row at a given time, but delayed in time. One could now use an external data processing unit to add the correct scene data of all rows together. This results in an increased signal, and an increased signal to noise ratio.

III. CCD vs. CMOS TDI

The state of art for TDI imaging is currently defined by CCD technology due to its outstanding image quality and low noise. CCD technology allows for an increase of sensitivity by moving and integrating collected photo-charge in a CCD array in synchronisation to and along the track of a moving scene. Since readout only occurs at the end of the array, little read noise is added. CCD technology, however, does not allow for ADC integration, and comes with speed and power bottlenecks due to the need of the high-speed horizontal shift register.

There are two important drawbacks of using CCD for earth observation using small satellites:

- High power consumption is required to read out the CCD array whereas in a satellite power consumption needs to be severely restricted.
- The inability of integrating driving and readout electronics on chip means that the imager system size (with its required surroundings) becomes much bigger which is problematic for small satellites. These problems become even worse when multiple CCD arrays are required to accommodate for the spectral resolution

Integrated TDI sensors can also be realized in CMOS image sensor technology taking advantage of the improved CMOS pixel technology and integrated circuits such as analog-to-digital converters (ADCs). Despite these improvements, larger numbers of stages (e.g. >8) result in excessive readout noise and power consumption for CMOS TDI solutions, since every row of a 2-dimensional imager has to be read as opposed to only the output stage in a CCD-based TDI imager. Hence the CMOS TDI imager has to operate at the same frame rate as a CCD TDI operates at line rate.

For CMOS TDI, these are the limitations and drawbacks:

- No possibility for large amount of TDI stages (up to 256) for high sensitivity.
- Reduced image quality due to excessive readout noise.
- High power consumption and data rates

IV. TDI USING CCD-IN-CMOS TECHNOLOGY

To address the issues outlined above, imec has developed a CCD-in-CMOS process integrating CCD TDI pixels in a 130nm backside illuminated CMOS process. Efficient charge transfer of CCD pixels is combined with CMOS high-speed and low-power electronics in the same imager die. Measurements done on a pixel test chip show a peak QE of 89%, 20ke- full well and a CTE of >0.99995 at 250kHz, while the CCD pixels operate well up to ~ 500 kHz line rate.

Imec has proven this technology by presenting a single-chip TDI sensor with 7 colour bands of 256 stages each. Line-by-line stage selection per band, individual band selection and bi-directionality enable multispectral TDI. Design and program freedom allows to a) switch on/off individual bands and b) allocate more or less TDI rows to different spectral bands, to optimize the signal to noise ratio (SNR). Each band uses individual on-chip sequencers and CCD drivers for the 5.4µm four-phase TDI pixels. CCD bands operate continuously and time interleaved, and top or bottom outputs can be connected to shared column-parallel ΔΣ-ADCs through a column line, akin to row selection in CMOS imagers. ADC outputs are serialized to 32 1.2V LVDS outputs along with two clock signals. These outputs are capable of running at an aggregate of >50Gb/s using on-chip PLLs. High dynamic range TDI can be enabled, using multiple bands per colour, but a different number of stages. Figure 1 shows a picture of the sensor with its 7 bands. The FSI version is shown as reference (left), the more light sensitive BSI version is shown next to it (right).

As a proof-of-concept, an RGB butcher-block filter has been used as glass lid for the sensor as early demonstration of the integration of filters resulting in a multispectral TDI imager. The sensor, camera system and a colour image captured by the setup are depicted in Figure 2. An implementation with 7 bandpass filters is in preparation. Table 1 shows the specifications of the 7-band TDI imager.

V. REFERENCES

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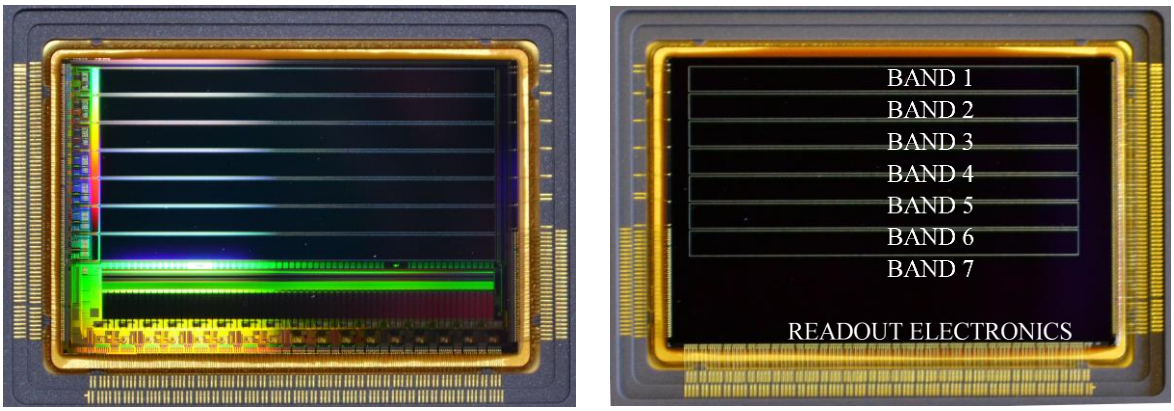

Figure 1: 7-band CCD-in-CMOS TDI chip picture: frontside illuminated (left) and backside illuminated (right).

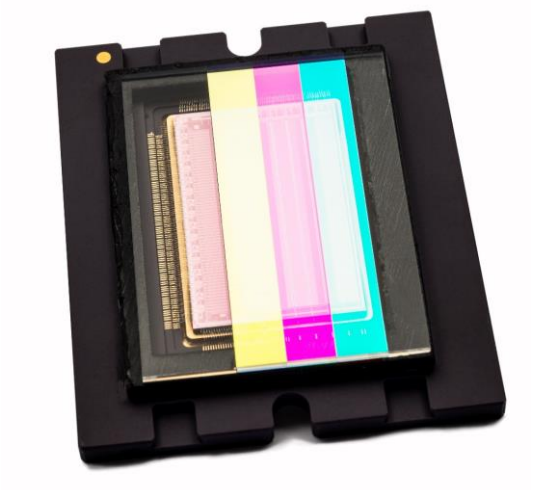

Figure 2: Color image captured by the 7-band CCD-in-CMOS TDI imager using an RGB filter on a glass lid.

Table 1: Specification summary of the 7-band TDI imager.

Spec target*	Value
Array size	4k x 256 per band
Pixel size	5.4µm
Stage selection	1-to-256 per band individually
Bi-directional	Yes
Number of bands	1 band or 7 bands # bands can be enabled
Line rate	Up to 300kHz* aggregate (e.g. 57kHz per band when all bands enabled)
Power	~ 2.5 W
Dynamic range	>60dB
CTI	$<10^{-5}$ at >300kHz
QE	>90% VIS /wo color filters >60% UV
Package type	Ceramic µPGA
Output type	32x 1Gb/s LVDS
Color filters	On glass lid or on the sensor

Session B

Radiation-hardened technologies for analogue and mixed-signal ICs

Mixed-Signal Test Vehicle in Microchip Atmel ATMX150RHA

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Abstract

A test vehicle has been designed and tested by Airbus Defence and Space and CNES to evaluate the ATMX150RHA technology from Atmel Microchip. The design and test have been fully subcontracted to Weeroc. A 16-bit 10MSPS dual DAC and a series of analogue switch compose the main core of that test vehicle. On top of these main features, a selection of high voltage transistors, capacitances and resistors from the analogue library has been added for further total dose irradiation test. Fast LVDS transmitter and receiver from Atmel new 3.3V I/Os library have been added to characterize these new I/Os.

This paper describes the results obtained in measurement of the 16-bit DAC IP.

I. 16-BIT DAC ARCHITECTURE

This first iteration of a 16-bit DAC IP has been designed based on 3 main requirement specifications:

- resolution (16-bit)
- speed (4 Msps)
- reference modulation

Bibliography has been conducted during the definition phase. The required resolution and speed pointed out that current steering based DAC is the most suitable architecture for this design and requirements. Further investigations [1] helped to narrow down the design to hybrid segmented architecture which combined the thermometer-coded current sources combined with binary-coded current sources. Lastly, the segmentation of the DAC is decided with the required reference modulation frequency and design complexity [2][3]. The DAC is segmented into 4-bit MSB thermometer-coded unary current mirrors and 12-LSB binary-coded current mirrors. Architecture of the DAC is shown in Figure 1.

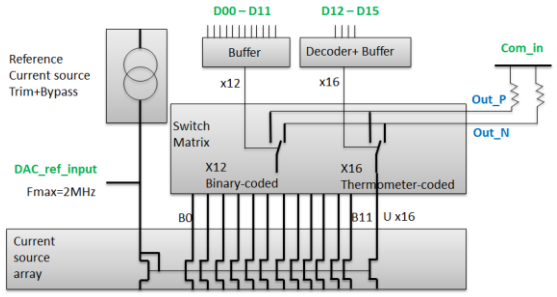

Figure 1 - 16-bit DAC Architecture

The power supply for this IP is VDD = 3.3 V and it is separated according to different domains:

- Digital (VDD_D & GND_D)
- Analog (VDD_A & GND_A)
- Output stage (VDD_AO & GND_AO)

The input Common Mode pin,"Com_in", is expected to be at 3.3 V and the DAC output current is drawn from that pin. Most of the analog section is operated with a 3.3 V supply. On the other hand, the digital core is powered with 1.8 V, thus requiring internal step-down for the power supply by internal regulators.

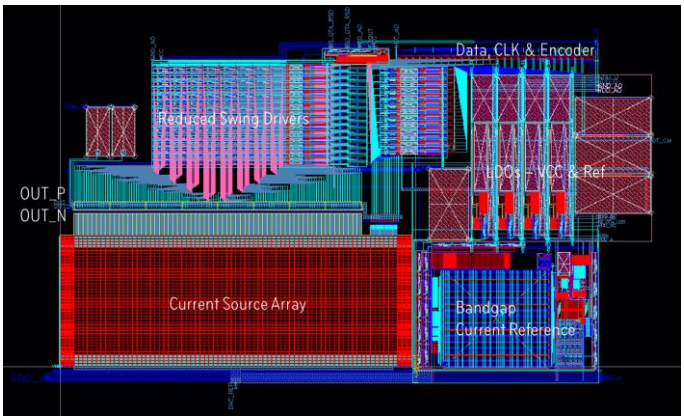

Figure 2 - 16-bit DAC Layout

A. Reference current generation

The reference current of the 16-bit DAC is generated by a combination of several components: bandgap reference, stabilised power supply and size-compensated current mirrors. The block schema for reference current generation is depicted in Figure 3.

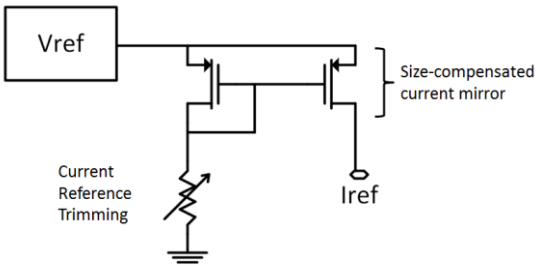

Figure 3 - Reference Current Block Scheme

B. *Current Source Array*

The current-source array is composed of a 12-bit section of binary weighted transistors for LSBs and 15-bit unary transistor matrix for the 4 MSBs. A variable reference current is set as an input, that reference current has a maximum value of 2.5mA. Sum of output current is 4 times the input current and is therefore limited to 10mA. Dummy transistors ensure good uniformity of the transistor current source matrix array which is composed of 3510 unitary transistors. Transistors have been matched to maximize the uniformity and minimize the input capacitance to maximize the current source array bandwidth. The size of the whole current source matrix is 700µm x 300µm on silicon.

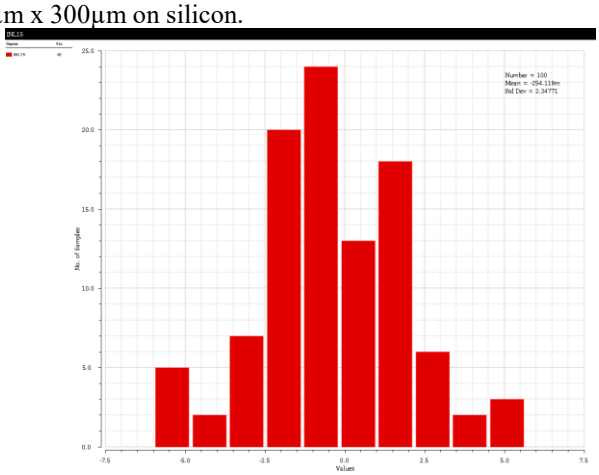

Figure 4 - MSB monte-carlo simulation of non-linearity (in LSB)

Monte-Carlo simulation has been performed to perform the sizing optimization at the requirement specification (DNL +/- 4 LSB, INL +/- 5 LSB). Simulation of the MSB is shown in Figure 4 and full DAC simulation is shown in Table 1.

Table 1 - Current simulation and non-linearity on every DAC bit

Bit#	Min (µA)	max (µA)	mean (µA)	sigma nA rms	min INL LSB	max INL LSB
I0	0,1942	0,1977	0,196	0,737	0,3	0,3
I1	0,3344	0,3404	0,3375	0,917	0,2	0,2
I2	0,6397	0,6472	0,6434	1,557	0,2	0,2
I3	1,27	1,278	1,274	1,82	0,3	0,4
I4	2,484	2,509	2,498	5,003	0,3	0,4
I5	4,851	4,919	4,884	15,15	-0,2	0,2
I6	9,701	9,809	9,764	20,46	-0,4	0,3
I7	19,46	19,59	19,53	27,95	-0,4	0,4
I8	38,96	39,18	39,06	44,59	-0,6	0,8
I9	77,94	78,24	78,1	60,15	-1,1	0,8
I10	156	156,4	156,2	82,11	-1,4	1,4
I11	312,1	312,8	312,4	132,9	-1,9	2,1
I12	624,4	625,4	624,9	198,7	-2,1	3,0
I13	1249	1251	1250	308,3	-3,9	4,6
I14	2498	2501	2499	528,2	-5,9	4,6
I15	4997	5002	4999	931,3	-5,9	5,8
Total	9992,3	10005,3	9997,8	-	-	-

C. *Switch Array*

For steering out the current from the current source array to the output, fully differential switches have been implemented. There are 32 switches in total and basic principle is depicted in Figure 5.

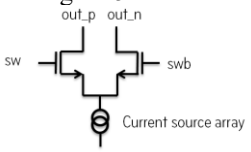

Figure 5 – Switch Basic Scheme

”Out_p” and “out_n” are the common outputs where all the switches are connected. “sw” and “swb” denotes the signal for driving the switch gate so that the switches can be turned ON or OFF. Turning ON the switches will steer the incoming current to the output “out_p” or “”out_n”. Of course the current steered to the outputs is sourced from the current source array discussed in previous section.

The current switches are required to deliver up to 10 mA per output; therefore the size of the switches is adapted following the output requirement. Other requirements for the switch design are for example having a settling time and glitches area within the specification (respectively < 50ns and < 35pA/s) on the outputs.

The transistor type chosen for the switch is 1.8V MOS nfet which has the lowest threshold voltage (Vth) (0.38~0.52V in typical case) and the highest saturation current among the transistors offered by ATMX150RHA technology.

The glitch amplitude can be relatively high (85 µA) especially when several current mirrors are turned ON and OFF at the same time. Glitches can be minimised or even suppressed completely if there is only a small number of a switch or the outputs are independent for each switch. However with high number of switches such as in this design, glitch reduction technique could have some limitations. Basic techniques used for minimising the glitches include using a reduced-swing switch driver, slower rising/falling edge and dummy structure.

In this design the Reduced-swing Switch Driver is used since this solution can be applied systematically to all switches in this DAC. Additionally, a low-pass filtering is also applied to the current output in order to reduce furthermore the glitches amplitude.

D. *Reduced-swing Switch Driver*

Glitches on the output occur due to the discharge of Gate-Drain capacitance (Cgd) during the switches transition from ON to OFF and vice-versa. This discharge amplitude depends heavily on switch driver amplitude and also rise/fall time of the switch driver signal. Additionally the discharge current can be absorbed through a dummy structure. However the

discharge absorbing mechanism will start to exhibit some limitations when facing with huge number of switches such as in this design. Therefore the glitch reduction strategy is mostly focused on reducing the switch driver signal amplitude. The driver design is depicted in Figure 6.

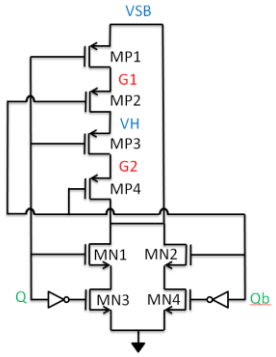

Figure 6 - Reduced-swing Switch Driver

Settling time, overshoot, undershoot and Glitches have been simulated for all main DAC code transition. Results are shown in Table 2.

Table 2 – Transient characteristics of DAC outputs

Transition DAC code	Settling Time[1] (ns)		Max Overshoot Amplitude (µA)		Max Undershoot Amplitude (µA)		Max Glitch Surface[2] (pA.s)	
	OutP	OutN	OutP	Out_N	Out_P	Out_N	OutP	Out_N
0 -> 1	<1	1	-	-	-	-	-	-
1 -> 2	<1	1	-	-	-	-	-	-
3 -> 4	<1	1	-	0.02	-	0.15	-	-
7 -> 8	1	2	-	0.04	-	0.25	-	20
15 -> 16	1	3	0.09	0.04	-	0.4	0.04	51
31 -> 32	5	4	0.1	0.04	-	0.5	0.014	26
63 -> 64	6	4	0.1	0.07	0.01	0.7	0.03	28
127 -> 128	7	4	0.13	0.13	0.04	0.95	0.075	30
255 -> 256	9	4	0.17	0.25	0.11	1.5	0.025	33.5
511 -> 512	10	7	0.3	0.5	0.2	2	0.05	38
1023 -> 1024	12	10	0.5	1	0.5	4	1.8	40
2047 -> 2048	13	16	1	2	1	8	4	42
4095 -> 4096	20	20	2	5	7	17	8	47
8192 -> 8193	22	22	5	9	10	36	0.95	41
16383 -> 16384	27	29	11	18	26	63	1.4	34
32767 -> 32768	33	32	33	31	84	85	15	16.3

II. 16-BIT DAC MEASUREMENT RESULTS

A test board (Figure 7), a specific firmware and software (Figure 8) have been designed to characterize the 16-bit DAC.

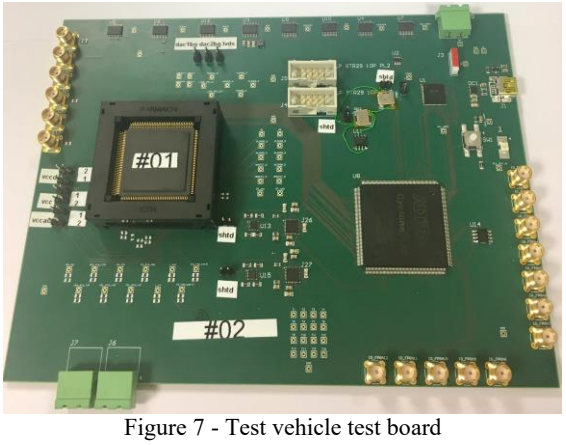

Figure 7 - Test vehicle test board

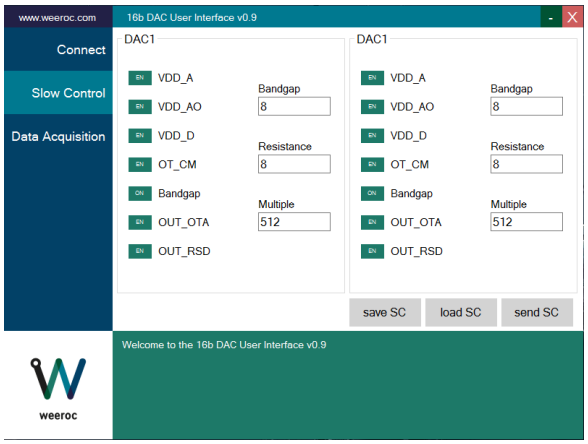

Figure 8 - Test system software

This test board has been used to test all parameters of the 16-bit DAC shown below.

A. Static measurements

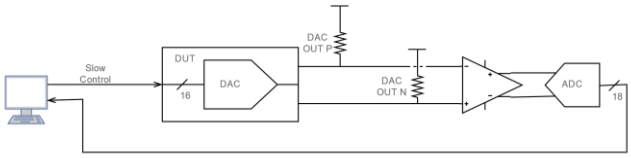

Figure 9 - DAC linearity test setup

1) Offset and Gain Error

The linearity has been done by sweeping all the codes between 0 and 65535 and by collecting the 18-bit ADC output values. Assuming the gain of 2 in the voltage buffer and a DAC code sweep from 0 to 65535, the ADC code should vary from 65535 to -65535. Hence the ideal gain is -2 and the ideal intercept of the linearity is 65535. The gain of the DAC is measured at -1.999093 with an intercept of 65476.13.

The requirement on the gain error is ± 1 % on the full scale range. The error on this measurement is -0.0455 %. The offset error is -0.09 % FSR with a requirement of ± 0.2 % FSR.

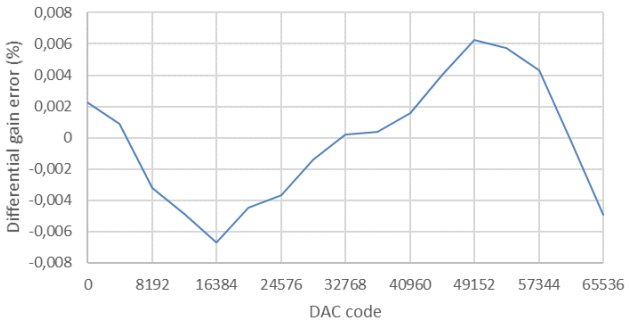

Figure 10 - Differential Gain Error

2) INL and DNL

The INL (Integral Non Linearity) and DNL (Differential Non Linearity) has been measured by sweeping the input DAC code from 0 to 65535. Measurement shows a non-linearity at the binary to thermometer interface as shown in Figure 11.

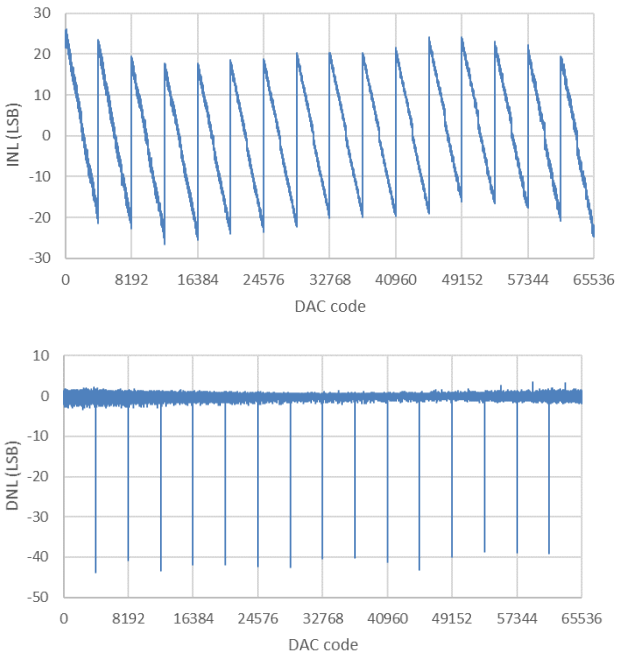

Figure 11 - INL (top) and DNL (bottom) of 16 bit DAC

The DNL for the codes n x 4096 is about -40 LSB. It doesn't depend on the noise, this is a true DNL error observable as a large chainsaw effect on the residual (Figure 11). By doing the fit on a small portion between two thermometer bit changes, the INL remain within +4/-4 LSB (Figure 12). The requirement being a +4/-4 LSB INL, the requirement is fulfilled for the binary partition of the DAC.

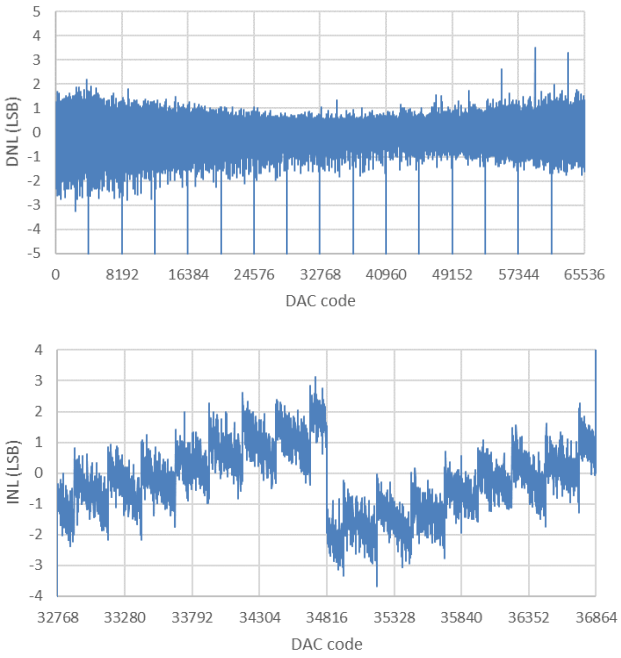

Figure 12 - INL y-zoom (top) and DNL x-zoom (bottom) of 16 bit DAC

In order to correct the 4 MSB bit error, the current reference of the thermometer bits should be trimmed. Because there is a unique current reference in the DAC, this is not possible. The DNL and INL requirements could be achieved by adjusting individually the current reference for the two partitions, binary and thermometer. That trim capability will be added in the second version of the IP to get a true 16 bit DAC.

B. Transient Measurements

Transient tests are performed by sending test vectors to the DAC input command. These vectors are either generated automatically or sent manually through the GUI. Outputs of the DAC are connected directly to a high resolution oscilloscope (12-bit, 1 GHz BW). During the tests, other components (buffers, ADCs, …) are set to off or shut down state. The test setup is shown in Figure 13. The following tests are performed:

- Min to max , max to min and mid-scale transitions
- Glitch measurement
- Settling time measurement
- Rise/Fall time measurement

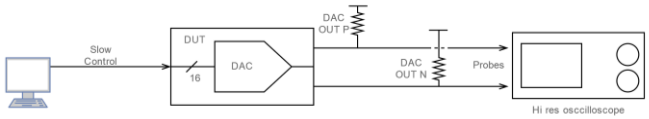

Figure 13 - Transient Measurement Test Setup

Transition times shown in Table 3 are close to specification (50ns) for the full range transition span and in specification for the smaller transition span.

Table 3 - Settling Time Measurement

Min to max rise time	54 ns
Max to min fall time	57 ns
32767 →32768 code transition	35.2 ns
32768 →32767 code transition	35.2 ns

Since the ringing from the min to max transition is barely visible, only the midscale transition glitch is measured. The amplitude and surface of the glitches are the following:

- Transition 32767 → 32768 :
  - Surface : 44.08 pWb (0.44 pA/s),
  - Amplitude (peak to peak) : 20 mV
- Transition 32768 → 32767 :
  - Surface : 53.87 pWb (0.54 pA/s),
  - Amplitude (peak to peak) : 25 mV

C. AC measurements

AC measurements of the DAC are performed by generating digital sine wave at various update rate and output frequency. The sine wave is generated by using a NCO (numerically controlled oscillator). The GUI of the evaluation setup is used for setting the update rate and output frequency out the generated waveform. The DAC outputs are connected directly to the high resolution oscilloscope with spectrum analysis capability. During the tests, other components

(buffers, ADCs, ...) are set to off or shut down state. The test setup is shown in Figure 14.

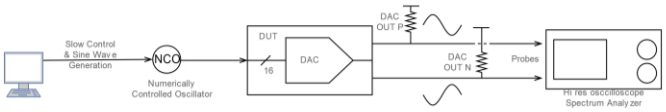

Figure 14 - AC measurement Test Setup

AC spectrum is analysed for different frequencies dynamic range has been measured.

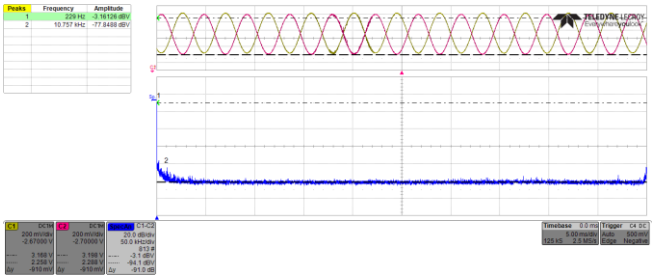

Figure 15 - AC analysis - Frequency 1KHz - SFDR 75dB

SFDR is measured from DC to Nyquist frequency (Update Rate / 2) by including spurious created by the signal harmonics (Figure 16). The sine wave for the tests ranges from 1 kHz to 1 MHz and the tests are performed for 1 MSps, 4 MSps and 10 MSps update rate. SFDR is about 75dB for low frequency signals.

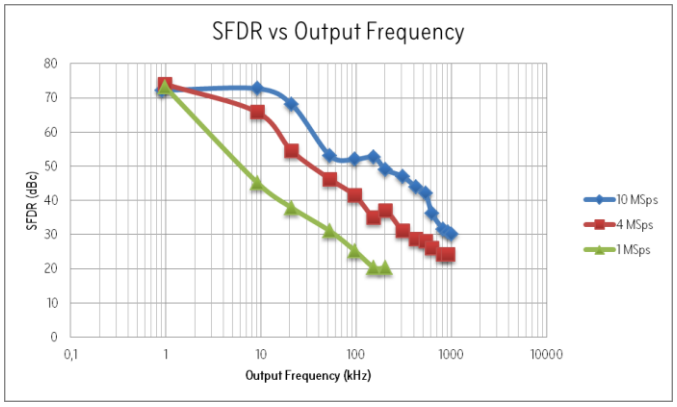

Figure 16 - SFDR vs. Sine wave output frequency

III. Conclusion

A first iteration of a 16-bit DAC has been designed using the new ATMX150RHA radhard technology. The block is working and two improvements must be conducted in a next iteration to have an IP fully in specification.

The first correction will be the improvement of the thermometer to binary matching. The second improvement will be a noise reduction done with a floorplanning modification in the padring.

Beyond these two detected bug, the DAC 16-bit is in specification for all requirements and the ATMX150RHA technology is showing very good analogue performances well modelled in the process design kit.

IV. References

[1] Gaurav Raja & Basabi Bhaumik (2006). 16-bit Segmented Type Current Steering DAC for Video Applications. Proceedings of the 19th International Conference on VLSI Design (VLSID'06). 1063-9667/06

[2] Geert A. M. Van der Plas, Michel S. J. Steyaert & Al (1999). A 14-bit Intrinsic Accuracy Q^2 Random Walk CMOS DAC. IEEE journal of solid-state circuits, vol. 34, no. 12, december 1999. 0018–9200/99

[3] S.Ramasamy, B.Venkataramani & Al (2010). The design of an area efficient segmented DAC. 2010 International Conference on Signal and Image Processing. 978-1-4244-8594-9/10.

The Design Against Radiation Effects (DARE) design platform for TSMC 65nm process.

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Abstract

DARE65T is a new radiation hardened (RH) high-performance system-on-a-chip (SoC) design platform including mixed-signal and analogue building blocks. It is built on the commercial TSMC 65nm LP 1.2V/2.5V CMOS technology. The DARE65T incorporates a set of standard and IO cell libraries, LVDS and SSTL cell libraries, memory and analogue IPs. The DARE65T development is based on common radiation design rules, which are implemented in an analog design kit (ADK). This approach facilitates also full custom radiation aware analogue design. DARE65T meats the main performance requirements of Space equipment designers.

The DARE65T platform provides SEE hardening capabilities among with low-power consumption and high density features. The used mitigation methods guarantee TID tolerance higher than 100 krad as well as SEL hardening for LET values higher than 60 MeV/cm2.mg.

The paper is focusing on radiation effects (TID, SEL, SEU, SET) mitigation methods and details the development of the DARE65T library, provides its features and first results.

I. Introduction.

In the last decades the evolution of the technologies for space ASIC and chip production is bringing a high level of miniaturization, giving benefits in terms of less power consumption, less mass, less volume, reduced number of components on the boards, better testability, higher performances and reliability. Newest space technologies (optical and RF communications) as well as miniature CubeSats and communication satellites are demanding more and more performance from electronic components. At the same time, satellites' reliability and lifetime requirements are still requesting for TID and SEE radiation hardness. Space System Designers are always looking for the best integration, area, power, performance, mass, volume, radiation hardness and cost tradeoffs. Hence, there is always a demand to go for not only nodes with more capabilities, but also to more advanced nodes, for they bring new capabilities to the playing field. As the lead time to access new technologies for the development of ASICs for Space applications is several years, and the long-term availability is limited by the technology lifetime, it is important to give system designers for Space applications access to these technologies as early as possible.

The new RH high-performance DARE65T platform is developed to meet those demands. It is built on the commercial TSMC 65nm LP 1.2V/2.5V CMOS technology. Thus it provides two kinds of core libraries: high speed and low-leakage. It has also a list of analogue blocks and SRAM memory solution to help building complex mixed-signal RH ASICs. As it was mentioned the Space designs are demanding more and more performance. The ASIC performance means not just a clock frequency, but also high-speed interfaces. Among classical requirements for LVDS IO cells in order to build SpaceWire interface links, there are new requests for DDR interface and high-performance link, for example, RapidIO or PCIe or JESD204. DARE65T platform supports such needs providing set of LVDS and SSTL IO cells. The relevant section of the paper gives detailed overview of such platform capability.

II. DARE65T mitigation methods.

In order to provide a cost-effective solution for low-volume radiation-hardened applications, a commercial foundry process is used for DARE libraries. Although no process tuning is available in such processes, the features already provided by the technology can be used for efficient mitigation of radiation effects. Thus commercial TSMC technology was selected for new platform: 65nm LP 1.2V/2.5V CMOS technology. This process has triple-well availability. Triple wells have been used for better SEU performance and SEL immunity.

The first significant step is to define the design platform basis concerning radiation effects (TID, SEL, SEU, SET) mitigation methods.

A. TID hardness.

The most interesting TID measurement results for TSMC 65 nm process have been found in [1] and are shown here below.

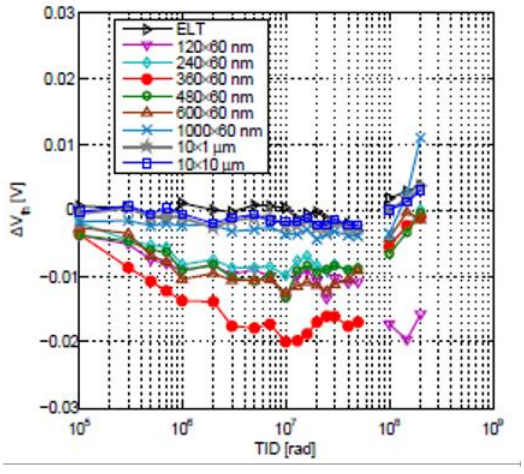

Figure 1: Threshold voltage shift measured for NMOS core (RVt) devices [1]

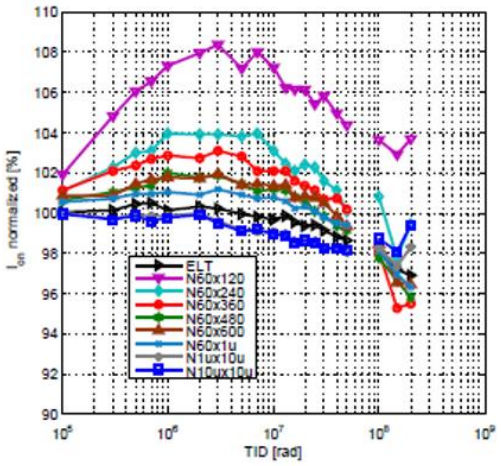

Figure 2: Max. drive current (Vgs=Vds=1.2V) measured for NMOS core (RVt) devices, normalized to pre-rad [1]

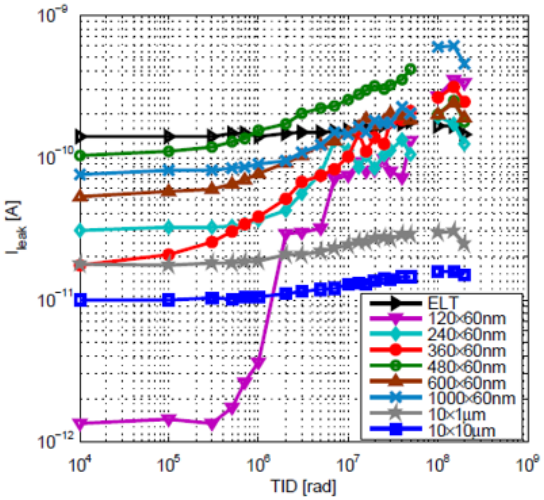

Figure 1: Leakage current measured for NMOS core (RVt) devices. **Error! Reference source not found.**]

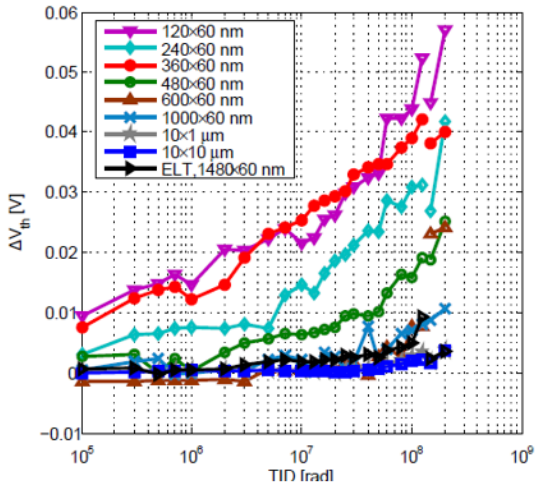

Figure 4: threshold voltage shift measured for PMOS core (RVt) devices [1]

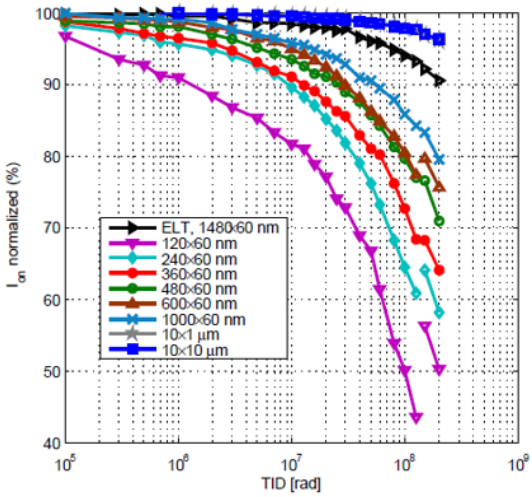

Figure 5: Max. drive current (Vgs=Vds=1.2V) measured for PMOS core (RVt) devices, normalized to pre-rad [1]

From the results shown on Figures above it appears that ELT transistors as TID mitigation method might be replaced with a normal transistors with the limits of the minimum core NMOS and PMOS transistors width. The 2 limitations might be set one is for digital designs and another one (larger W) for analogue designs.

The paper [1] provides also the TID behaviour of IO (2,5V) transistors (PMOS and NMOS). Similar conclusion is made for TID mitigation method for IO transistors.

For the DARE65T library with basic TID requirement of 100krad a minimal specification of core & IO transistors width could be enough to reach the needed TID hardness.

B. SEL hardness.

An n+ diffusion area in the p-substrate next to a p+ diffusion area in n-well forms a parasitic thyristor. Technologies are normally conceived so that parasitic thyristors do not impact circuit performance. Charged particles generated by heavy ion strikes may fire a parasitic thyristor and induce the circuit to go in latch-up. Another paper [2] provides good radiation experimental SEL results of 65nm semiconductor structures with and without guard rings. The experiments were made on 4 different RAM cells:

- "6T" is standard high density block with 6-transistor (6T) cell without any solutions for SEL prevention.
- "6T_GR" is based on 6T cell with N+ and P+ guard rings.
- "DICE_GR" block has solid guard rings
- "DICE" block has intermittent rings

No SEL is found at room temperature in all SRAM blocks at effective LET 60 MeVxcm^2/mg. The SEL occurs in "6T" block only at effective LET 60 MeVxcm2/mg and at elevated temperature.

This effect will be mitigated by introducing guard rings connected to supply or ground voltages. Both n+ and p+ guard rings will be employed in DARE65 libraries. P+ guard rings are also used for mitigating TID induced leakage. Over time, positive charges that are trapped in the STI oxides may shift the threshold voltages of parasitic NMOS field

transistors formed between two n-type regions (n+/n+, n-well/n-well, or n+/n-well). This effect can be mitigated with p+ guard rings in between n-type regions [3].

Additional SEL mitigation method which will be used is a minimum double contact requirements in source/drain areas of transistors.

The article [2] makes also interesting note that not only solid guard rings help to significantly enlarge the threshold LET for the latch-up effect, but also there is no SEL in the block with intermittent guard rings, too. That result will be used for SRAM memory implementation.

C. SEU behaviour.

The paper [2] gives also good description of SRAM structures SEU cross-section. The experiments were made on 4 different RAM cells, described in II.b. Fig. 6 [2] shows SEU cross-section LET dependence for the SRAM blocks. Note that error cross-sections, not event cross-sections, are shown here. One can see from Fig. 6 that high-LET cross-section values for "DICE" and "DICE_GR" are about 3 orders of magnitude lower than cross-sections for "6T" and "6T_GR".

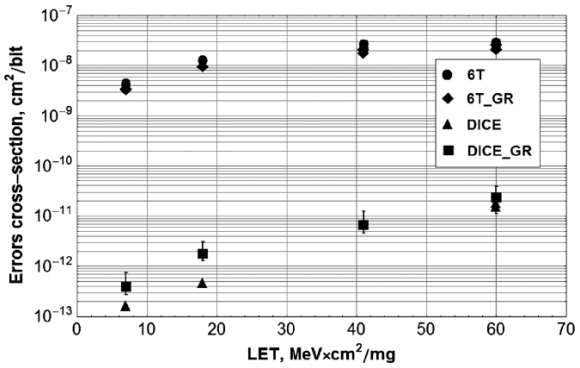

Figure 6: SEU cross-section LET dependence for SRAM blocks in 65 nm [2].

The list of SEU/SET mitigation methods used in DARE65T is provided below:

- Device spacing – to avoid "double hits"
- No Hot MOS (i.e. MOS where the bulk is respectively not connected to GND and VDD).
- Drive Strength Hardening – especially to create SET hardened standard cells.
- SET filters
- DICE FF
- Bit alignment in SRAM blocks – to avoid MBU

III. DARE65T LIBRARIES

As it was mentioned DARE65T is mixed-signal microelectronics platform that will deliver digital libraries, standard and high-speed IO cells, analogue IP and memory blocks suitable for radiation hardened applications.

The DARE65T operating conditions:

Temperature range: minus 55 – plus 125 ^{0}C;

Core supply voltage: 1.2 V ± 10%;

IO supply voltage: 1.8, 2.5, 3.3V ± 10%.

A. DARE65T_ADK

The DARE65T_ADK is radiation hardened extensions of the standard TSMC TS65LP foundry PDK. ADK incorporates and provides automatic checks of all chosen design rules, designers must follow in order to create RH ASICs. The DARE65T_ADK is integrated in Virtuoso (Cadence). ADK consists of 3 main parts:

- Schematic checks
- Layout checks
- SET simulation environment

Schematic and layout checks provide the automatic verification of RH design rules and radiation effects mitigation methods listed in section II. Thus schematic checks provides errors [4] when

- minimal specification of the core transistors width is violated;
- minimal specification of the IO transistors width is violated;
- NMOS transistor bulk net is found;
- Hot NMOS or PMOS is found.

The schematic checks has also several warning. For example, when transistor model without matching is used or unwanted device was placed in the schematic (DARE65 platform has a restriction for device usage).

Layout checks based on Calibre deck highlights the RH design rules violations [4], for example

- Poly crossing NTAP or PTAP
- N-Well regions on different net not separated by P+ guard ring
- N+ Active region(s) with leaky path to N-Well
- P-Well regions not separated by N+ diffusion guard-ring
- etc.

Another important point when doing radiation hardening by design for mixed-signal and analog blocks is simulation of SET events. ADK also provides the environment for such simulations. It is needed to find the SET sensitive nodes in a design and then adapt the design to bring the SET hardness in compliance with the specification. In order for an analog designer to do this efficiently the tools used are integrated in the normal analog design flow [5]. The SET simulation environment consists of several elements[5]:

- SET striker (Verilog-A) – it allows to perform single SET injection during simulation.
- Deepprobe – it removes the need to adapt the design of the DUT for SET simulations.
- Periodic SET striker – it generates events with a specified period and allows to replace all SET strikers with one in a schema.

The article [5] provides detailed description of DARE65T SET simulation environment.

B. DARE65T_CORE library

The digital core library comprises numerous combinational cells, SET-hardened cells, non-hardened and SEU-hardened sequential cells. The library is designed to offer good SEL hardening in a very compact standard cell template. General library figures are listed in Table 1.

Table 1: DARE65T core library figures

Parameter	Value
Number of cells	102
Raw gate density	344 kGates/mm^2
The pitch	0.2 µm
Cell height	12 tracks
Multi Vt support	SVt, HVt, LVt

The DARE65T_CORE library has similar performance to commercial TSMC 65nm LP 9 T library with moderate area increase. For example DARE65 NAND2 cell has similar timing performance and it is 1,5 larger then commercial 9T cell. The EXORD1 cell has similar performance and area figures. DARE65 standard cell library has SEL & TID only hardened FF which are 2 times only bigger then commercial counter pair and SEL&SEU&TID hardened DICE flipflops. DICE FF is implemented with respect to device spacing and thus 2,5 times larger than non SEU hardened FF (with the same performance). The figure 7 provides the visual comparison between DICE and usual FF of DARE65T_CORE lib.

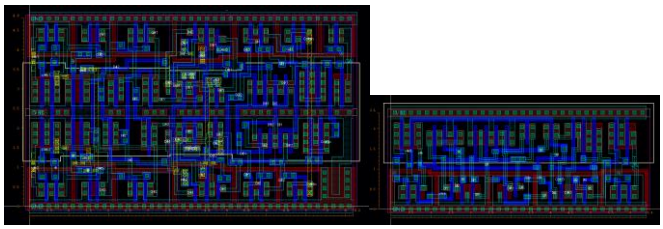

Figure 7: DARE65T_CORE DICE and std FF.

The DARE65T libraries supports all 3 Vt flavours (SVt, LVt, HVt) similar to commercial libraries. There will be 2 kind of standard cell libraries optimized by transistors geometry available:

- Low power consumption (mainly leakage)
- High performance.

Table 2 lists all types of DARE65T_CORE cells.

Table 2: DARE65T_CORE cell types

Type	N
Non-SET hardened combinational cells	52
SET hardened combinational cells - 25 MeVxcm^2/mg	7[1)]
SET hardened combinational cells - 40 MeVxcm^2/mg	7[1)]
SET hardened combinational cells - 60 MeVxcm^2/mg	7[1)]
Non-SET hardened sequential cells	9
SEU hardened sequential cells [2)]	5
ANTENNA cells	1
TIEH and TIEL	2
Non-SEU hardened clock gating cells	1
SEU hardened clock gating cells	3
Filler cells	8

Note: 1) – including SET hardened TMR voter cell
2) – SEU hardened cells has min LETh 60 MeVxcm^2/mg

C. DARE65T_SRAM

DARE65T design platform offers single port SRAM (SPRAM) and dual port SRAM (DPRAM) solutions. The DARE65T_SRAM library is based on custom TID and SEL hardened SRAM cell it is optimized for area and power consumption.

The memory blocks are designed to be insensitive to multi-bit upsets (MBU). This is achieved by arranging the bits of a same word far enough from each other. In this case every two bits of a same word are separated by 16 bits which corresponds to an interleaving distance higher than 15 µm. This way an error detection and correction circuit (EDAC) can be used to mitigate soft errors due to single-bit upsets (SBU).

The SPRAM cell area is 1,9 x 1,85 um^2. As it can be seen on Figure 8 the SPRAM memory cell has closed guard ring around nmos transistors in order to mitigate SEL & TID effects. Based on the experimental results mentioned in section II.B the intermittent guard ring might be used. It will allow to increase the memory density in 1,5 times. The impact on SEL and TID hardness should be acceptable. The HD SRAM memory cell will be introduced based on test vehicle radiation test results.

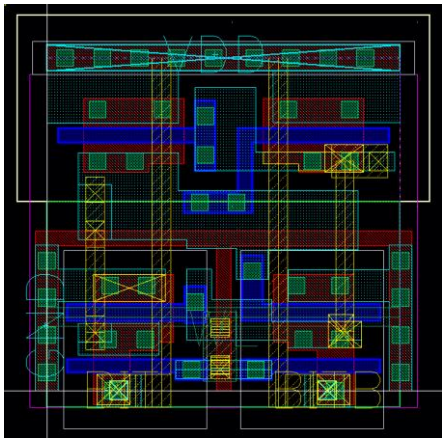

Figure 8: DARE65T SPRAM memory cell.

The DARE65T DPRAM cell area is 1,9 x 2,75 um2.

D. DARE65T_IO

The I/O library includes several digital and analog pad limited I/O cells. As in the core library, all I/O cells are hardened against SEL effects. Digital input I/O cells are also hardened against SET to prevent events from propagating to the core logic. The digital IO cells have the following features:

- cold spare
- slew-rate control
- programmable pullup, pulldown.

An extensive list of tri-state output, bidirectional bidirectional I/O cells with different driving capabilities is available. Power and ground I/O cells as well as breaker cells are available for the definition of multiple I/O power domains.

The DARE65T_IO library is based on 2,5V transistors with overdrive to 3,3 V. It is designed and optimized to work at different supply voltages: 3,3V, 2,5V and 1,8V.

E. DARE65T_SSTL & LVDS

As it was mentioned in the introduction there is great demand on high-speed interfaces. So among standard LVDS IO cells DARE65T platform will offer SSTL IO cells for 1,8V and 1,5V power supply (DDR2 and DDR3 respectively).

The DARE65T_SSTL library contains the following abutable cells, which once assembled, constitute an SSTL ring segment:

- SSTL_VREF - SSTL reference cell
- SSTL_RX_SE - SSTL single-ended receiver
- SSTL_RX_DIFF - SSTL differential receiver
- SSTL15_RXTX_SE - SSTL15 single-ended transceiver
- SSTL15_RXTX_DIFF - SSTL15 differential transceiver
- SSTL15_ZQ - SSTL15 ZQ auto-calibration cell
- SSTL18_RXTX_SE - SSTL18 single-ended transceiver
- SSTL18_RXTX_DIFF - SSTL18 differential transceiver
- SSTL18_ZQ - SSTL18 ZQ calibration cell
- SSTL_VDD1V2 - Core power supply
- SSTL_VSS1V2 - Core ground
- SSTL_VDD1V8 - IO power supply (1,5 and 1,8V)
- SSTL_VSS1V8 - IO ground
- SSTL_POC - Power-on control cell
- SSTL15_DLL – DLL cell

The cells are implemented with respect to the JEDEC standards JESD79-2F (DDR2/SSTL18) and JESD79-3F (DDR3/SSTL15). The target data rate is 800 Mbps.

DARE65T_LVDS library will have transmitter and receiver cells both made on 2,5 V overdrive 3,3 transistors. It will allow them to operate at 2,5 and 3,3 V voltage supply with up to 400 Mbps (200 MHz) data rate.

F. DARE65T first analogue blocks.

As mixed signal design platform DARE65 offers foundation rad hardened analogue IPs. Table 3 lists the analog blocks which will be available on early stage.

Table 3. DARE65T first RH analogue IP.

Analog IP	Main features
DARE65T_PLL	200-1200 MHz output frequency 2,5-32 MHz reference frequency Supply voltage 1,2V.
DARE65_IVREF	1,2V and 2,5 supply voltages 0,6V output reference voltage Reference current output Accuracy (before trimming) ± 2,5 %
DARE65_ADC	10 bit resolution Integrated temperature sensor 10 kHz sampling rate. Supply voltage 1,2V.
DARE65_POR	TBD

IV. Further Work

The next step of DARE65 development is test vehicle design. The test vehicle will include all the platform elements. The electrical and radiation tests of test vehicle will proof the DARE65T design platform concept and solutions.

The further development of mixed signal RH DARE65 design platform is significant point to make it suitable for any high-performance space applications. The next development steps could be:

- RH NVM memory solution (antifuse or similar)
- RH high speed links (for example RapidIO, PCIe, JESD204 multistandard SerDes)
- DDR2 and DDR3 PHY and controller
- High-performance ADC and DAC

V. Summary

This paper introduced the development of a new radiation hardened library platform for mixed-signal space applications. A set of libraries including numerous core cells, I/O pads, SRAM blocks and analog circuits is being developed and will offer a complete solution for high-performance applications that require TID tolerance 100-300 krad.

DARE65 libraries are reliable design platform for competitive high-performance radiation hardened ASICs.

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VII. ACKNOWLEDGEMENTS

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ESS180RH:
An 180nm digital library addressing Single Event Latch-up based on X-FAB XH018

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Abstract

European Sensor Systems develops and manufactures high quality sensors based on MEMS technology. The company has designed, fabricated and tested a radiation tolerant signal conditioning ASIC for capacitive sensors. This paper presents an approach for radiation mitigation against Single Event Latch-up (SEL) effects of the digital part at the physical level of the ASIC by implementing a custom digital library based on X-FAB XH018 technology.

I. INTRODUCTION

Harsh radiation environments constitute a major challenge for space applications. Pervasive particles from cosmic rays induce cumulative and transient effects that can cause soft errors or even permanent damage in electronics circuits.

The charge deposited by a single ionizing particle can produce a wide range of effects. Some of them, such as Single-Event Transient, Single-Event Upset and Single-Event Functional Interrupt are temporary and can be recovered. Others can lead to permanent damage such as Single-Event Latch-up (SEL) or Single-Event Gate Rupture. At this paper only the SEL mitigation strategy is discussed.

A SEL can cause a permanent and potentially destructive state of the device under test. A parasitic thyristor structure is triggered by an ion strike and a low impedance, high current path is created. When it occurs, a high current flows and if the current is not limited, a brief latch-up can result in a permanent damage.

To begin with, for a preceding project, European Sensor Systems had developed a mixed-signal ASIC at the course of the ESA funded activity "Accelerometer Component to TRL 5" [1] to interface with its MEMS capacitive accelerometer. The chip was designed and manufactured using X-FAB XH018 without any special precautions against SEL at the digital part. The components under test had been found to be SEL sensitive with a Linear Energy Transfer (LET) threshold between 6.4 MeV·cm^2/mg and 15.9 MeV·cm^2/mg, which had been significantly lower than the required value of 80 MeV·cm^2/mg. SEL effects had not been destructive though, since the tested dies had recovered after a power cycle. The outcome of that activity was the necessity to address the intrinsic SEL vulnerability of XH018 in a more radical way in future ASIC developments.

As a result, in the course of the ESA activity "Standard Accuracy Pressure Transducer" [2], European Sensor Systems has been developing a "Space Qualified Family of MEMS Pressure Modules for Satellite Applications" based on MEMS capacitive sensors. The sensors have being manufactured using European Sensor Systems TM30P1111 technology, which is a combination of SOI, bulk and surface micro-machining process. In order to interface with the MEMS a custom radiation-hardened capacitive sensor signal conditioning ASIC was needed. The ASIC SEE tolerance target was 60 MeV·cm²/mg. For the analog part, the well-known layout techniques at the physical level have been implemented [3]. For the digital part a SEL immune library was required and is discussed here.

The paper is organized as follows: Section II presents the implementation of the ASIC, Section III presents the radiation mitigation strategy and IV presents the radiation test results of the SEE/SEL campaign.

II. ASIC IMPLEMENTATION

The ASIC is based on the architecture of its commercial counterparts [4], which were already manufactured in XH018, so selecting an inherently SEL immune SOI technology was not a reasonable and attractive choice. Besides that, at that time, the IMEC DARE180X [5] was under development and not fully tested, so it was decided to build a new custom digital library immune to SEL allowing full in-house control of synthesis and place and route operations.

A. XFAB - XH018

X-FAB XH018 Process is a 0.18 micron Modular Mixed Signal HV CMOS Technology [6]. Based upon the industrial standard it has single poly with up to six metal layers 0.18-micron drawn gate length N-well process.

B. ASIC architecture

In the course of this activity a mixed-signal radiation-hardened capacitive sensor signal conditioning ASIC has been designed, fabricated and tested.

The ASIC is capable of interfacing both single and differential capacitive sensor architectures. The range of the full-scale input capacitance changes up to ±5.6pF, with a base capacitance of up to 40pF in order to cover the application requirements for pressure ranges of 7, 22, 150 and 310 bara.

Sensor capacitance variations can be compensated by an on-chip trimmable capacitor bank. The Capacitance-to-Digital Converter combines the Capacitance-to-Voltage converter with a second-order ΣΔ modulator and a decimation filter to produce a high resolution output with a programmable update rate. The ΣΔ has a programmable output rate from 0.05 Hz to 15.6 KHz.

It has the following outputs: a 10-bit resolution analog output, a non-calibrated 32-bits digital output for pressure measurement and a 32-bits digital output for temperature measurement of the on-chip temperature sensor. The digital outputs are available via the I^2C compatible serial interface or the input serial digital (ISD) interface. The resolution of the digital outputs is more than 16 Effective Number of Bits at low update rates.

The ASIC has an internal clock oscillator of 10 MHz, which is the frequency of operation of the digital part. The die is supplied by a 5.7V. The analog core voltage is 3.3V, the digital core voltage is 3.3V and all I/O operations are performed at 5.7V. The chip, draws 6 mA current and its size is 3x2 mm^2. The manufactured ASIC is shown in Figure 1.

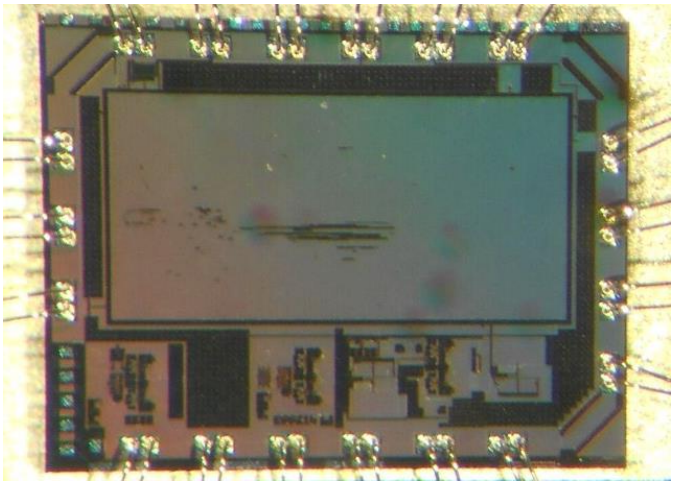

Figure 1: ASIC die

III. Radiation Mitigation Strategy

A. SEE/SEL in the analog part

For the analog part, preventing latch-up from occurring was realised by reducing the gain of the two parasitic transistors by increasing the distance between the two parasitic complementary transistors where possible, reducing parasitic well and substrate resistors by using low resistance ground contacts and by surrounding MOS transistors with guard rings. In practice, all PMOS devices have been enclosed by N-type guard rings and all the NMOS devices have been enclosed by P-type guard rings.

B. SEE/SEL in the digital part

For the digital part a SEL immune library was developed. The digital part comprises the decimation stages for the pressure and temperature channel, the I^2C compatible slave interface, the ISD interface, the registers bank, the OTP memory controller, the PWM unit along with the associated control and glue logic. For all the above functional blocks the rad-hard library has been used with the exception of the OTP memory, which is powered down after downloading its contents to the registers.

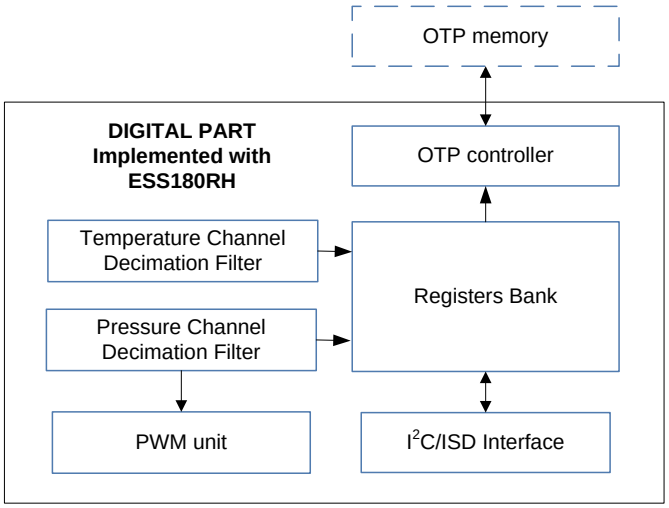

Figure 2: ASIC digital part architecture

ESS180RH is a family of digital standard cells based on D_CELLSL_JI3V of XH018. There was an iterative procedure in order to identify, which logic cells from the D_CELLSL_JI3V digital library form a subset capable of meeting the design requirements with minimum area overhead. In total, there are 28944 cells (34.8% sequential, 5.5% inverter and 59.7% logic).

D_CELLSL_JI3V is a 3.3V triple-well isolated CMOS. The main advantage is that the switching noise of the junction isolated digital cells does not affect the silicon substrate. ESS180RH contains combinational (logic gates), sequential (scan flip-flops) and special cells (layout fillers, antenna protection cells, level shifters). In the layout the triple well NMOS and PMOS devices have been surrounded by P-type and N-type guard rings respectively as shown in Figure 3.

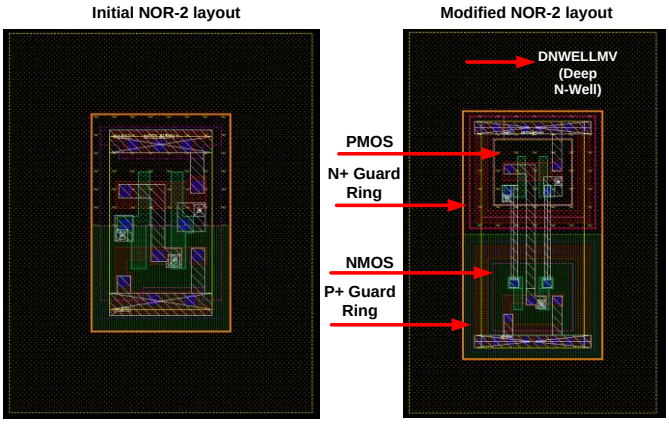

Figure 3: Rad-hard NOR gate with two inputs

The increase of the layout area compared to a conventional cell varies from 2x for the bigger cells to 4x for the smaller cells.

Once the layout of each cell is finished, a Library Exchange Format (LEF) file is generated, which includes design rules and abstract information about the cells.

An RC parasitic extraction is performed in order to obtain an extracted netlist for analog simulations. The purpose of this step is to perform the modelling of interconnects (resistive and capacitive parasitics) and capturing of the Layout Dependent Effects that affect the transistor characteristics and depend on layout placement.

The extracted netlist of each cell is then used to perform analog simulations. The output of this step is the creation of the Liberty™ library format, which is an ASCII representation of the timing and power parameters associated with each cell. The timing and power parameters are obtained by simulating the cells under a variety of conditions (Process, Voltage, and Temperature) corners and are used for static timing analysis and power analysis.

The structure of the .lib file is quite complex. The detailed description of the .lib file and the derivation of the timings is out of the scope of this document. Instead some important aspects are described here for the combinational and sequential cells. The timing characterization is performed using a two-dimensional timing model where the two independent axis variable are input slew and output load capacitance. This means that a two-dimensional matrix is created for each metric, where each row corresponds to the Input Slew and each column to the Output load capacitance.

The characterization is performed for three corners: typical (3.3V/25 °C), worst speed (2.6V/175 °C) and worst power (3.6V, -40 °C). The procedure for the creation of the library is automated and can be easily applied to other foundries or PDK flavors.

IV. Radiation Tests

A. *Test setup*

The test setup preparation is compliant with ESCC Basic Specification No. 25100 [7]. Each sample DUT is hosted in a daughter card, which is attached on a test motherboard.

The SEL test needs to be performed at the maximum voltage supply and at elevated temperature. The reason for this is that the SEL signature is a self-sustainable current flowing in the low impedance path of the triggered parasitic thyristor structure whose gain increases with temperature.

Each daughter card has a heating pad attached at its bottom using a thermal conductive adhesive for setting the temperature to a level higher than 75 °C in a closed-loop control. The front and back side of the daughter card are shown in Figure 4 and Figure 5 respectively.

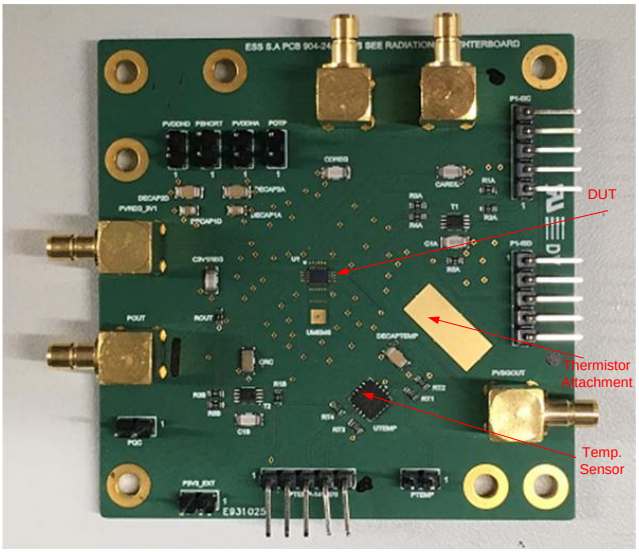

Figure 4: Daughter card front-side

The motherboard has a microcontroller, which reads the temperature indication continuously and adjusts the current flowing into the heating element using a power MOSFET. The exposed pad of the temperature sensor is connected to the ground node. Monitoring of temperature is also performed using a thermocouple attached very close to the DUT.

Figure 5: Heating pad attached at the back-side of the daughter card

The motherboard performs serial communication with the DUT, provides electrical connections to the feedthrough connectors from inside the vacuum chamber to the monitoring equipment cables and computer outside the chamber as shown in Figure 7

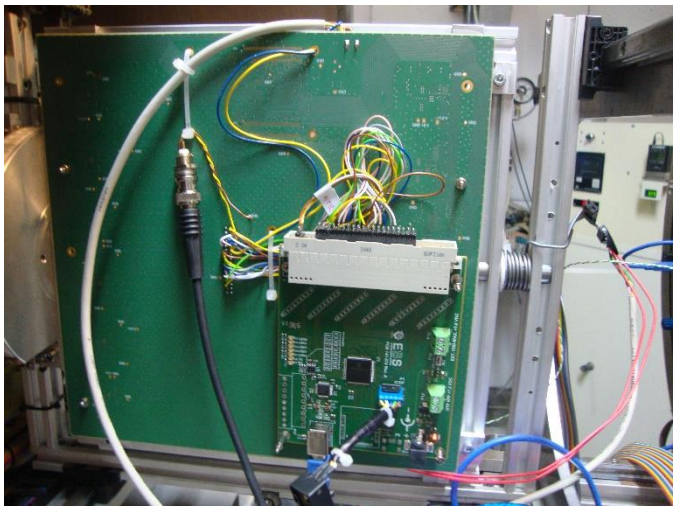

Figure 6: Motherboard in the irradiation chamber

The DC currents from VDDHD (Idd) and VDDHA (Icc) are monitored with two different Power Supply Units (PSUs). PSU-1 controls the power supply of the analog part of the ASIC (VDDHA) and PSU-2 controls the power supply of the digital part of the ASIC (VDDHD). Each PSU is connected to the monitoring PC via the serial interface and controlled via a LabView program. The current threshold for SEL detection in each ASIC DUT is adjusted from software with a default value of 10 mA. In case of a SEL and an overcurrent detection (>10 mA) in the PSU, the PSU is powered off and the SEL event is logged. The scheme is shown in Figure 8.

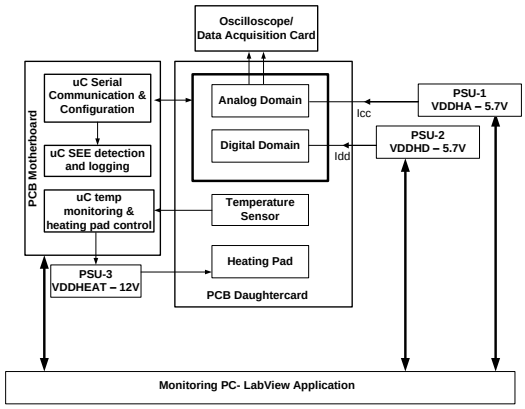

Figure 7: SEE test setup

The test software automatically powers on the PSUs again, configures the DUT and continues the test. The time for which the DUTs are not powered is the "dead time". The remaining time is the "active time" and is the amount of time the DUT is in a condition sensitive to detectable SEE. The test software provides the flexibility to monitor the increase of the currents of each PSU individually above a threshold and log them to the computer. A software snapshot is shown in Figure 8.

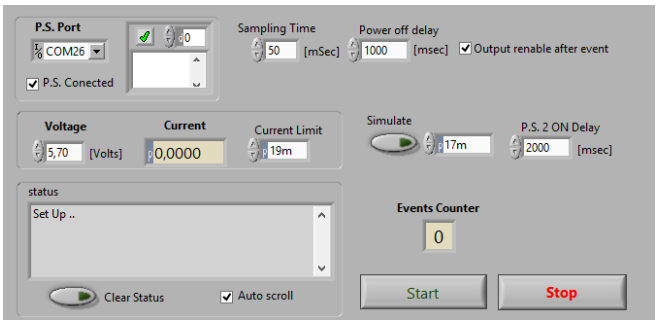

Figure 8: LabView program for SEE/SEL experiment

B. *Test results*

For the radiation tests the ion cocktail of During the experiment, no SEL event has been detected in the analog voltage supply (VDDHA) or digital supply (VDDHD).

Table 1 has been applied to the DUTs. Three ASICs have been tested for SEE/SEL in the HIF Université Catholique de Louvain (UCL), Centre de Recherches du Cyclotron, Louvain-la-Neuve, Belgium.

For the SEL tests a fluence of 10^7 ions/cm^2 has been used with a flux of 5000 to 15000 ions/cm^2·s. The test has been performed at 75 °C.

During the experiment, no SEL event has been detected in the analog voltage supply (VDDHA) or digital supply (VDDHD).

Table 1: Irradiation Steps

Ion	Energy (MeV)	LET (Si) (MeV·cm^2/mg)	Fluence (ions/cm^2)	Temp. (°C)	SEL
$^{13}C^{4+}$	131	1.3	10^7	75	No
$^{22}Ne^{7+}$	238	3.3	10^7	75	No
$^{40}Ar^{12+}$	379	10.0	10^7	75	No
$^{58}Ni^{18+}$	582	20.4	10^7	75	No
$^{84}Kr^{25+}$	769	32.4	10^7	75	No
$^{124}Xe^{35+}$	995	62.5	10^7	75	No

V. Conclusions

The design of radiation tolerant ASIC in a standard 0.18um CMOS process has been presented, which adopts radiation mitigation strategies for SEL. In order to prevent SEL, intervention at physical level was required. For the analog part a well-known solution was adopted. For the digital part, a new 3.3V digital library ESS180RH has been created based on custom layout, parasitic extraction, simulation of the cells and generation of appropriate timing and layout files.

The design was tested up to 62.5 MeV·cm^2/mg at the proper voltage and temperature conditions with the appropriate test hardware and software and no SEL event occurred proving the effectiveness of the mitigation strategy.

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DARE SET Simulation Flow Integrated in Virtuoso ADE L/XL Design Environment

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Abstract

One of the important steps when doing radiation hardening by design for mixed-signal and analog blocks is simulation of SET events. It is needed to find the SET sensitive nodes in a design and then adapt the design to bring the SET hardness in compliance with the specification. In order for an analog designer to do this efficiently the tools used should be integrated in the normal analog design flow. It should be flexible enough to screen for sensitive nodes in a design and later on focus on certain nodes. In analog design the timing of an event is important as a strike often only generates a non-compliant SET on the output when the circuit is in a certain state or transition. The timing may be dependent on the simulation corner and ideally the testbench should not need to be changed for this dependence. Additionally it should be avoided that a certain circuit has to be adapted to be able to inject an SET pulse in any node in its hierarchy.

In this paper the history of the SET simulation environment used in imec for DARE[1] is presented and the discussion of current state as used for the DARE65 project within imec.

I. SET Simulation Flow and its History

In this chapter the current SET simulation flow used in imec is discussed based on the history of the introduction of the different features. The history shows the different steps taken to fulfil the requirements of an efficient and user friendly SET simulation flow.

A. Ocean scripts

As already discussed in [2] at AMICSA 2016 our SET simulation flow originally started from Ocean scripts that did SET injection in all nodes on a netlist. This flow is still used at imec for example for the screening of a standard cell library for SET sensitivity. But for analog design this flow was not considered ideal. Ocean scripting and working on netlist level is not typically the level an analog designer will work. It also does not cooperate well with all the analysis capabilities provided by tools like Cadence Virtuoso ADE XL or Cadence Virtuoso ADE Assembler; a lot of manual intervention is needed to make that possible and own custom post-processing needed to view and summarize the results.

So development has been started on a SET flow more integrated in the Cadence GUI based analog design flow. This is described in the following paragraphs.

B. SET Striker Verilog-A model

The first step taken was to implement a device that can be instantiated in a circuit schematic and allows to perform SET injection during simulation.

All p-n junctions in a circuit are possible collection points for generated electrons and holes by particle strikes. The effect of the collected charges can be represented as a current injected from the n-side of the junction to the p-side of the junction. In Figure 1 an instantiation of the SETstriker cell that provides this functionality is shown in an example circuit. The SETstriker cell is implemented by a Verilog-A model that generates a double exponential current injection. The time constants of the double exponential curve are hard coded in the Verilog-A model and based on literature ([3],[4]).

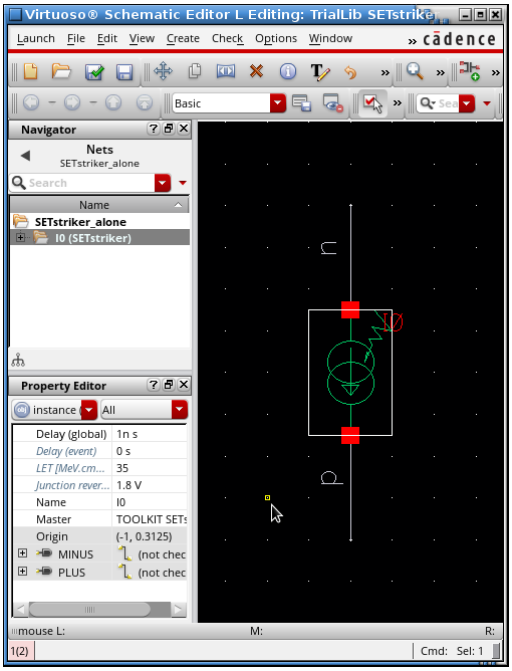

Figure 1: SETstriker Verilog-A element

The total charge Q injected over the time of an SET event is dependent on the energy of the particle that generates the charge and on the collection depth. As shown in Figure 1 the energy of the particle is a parameter of the cell. The collection depth is tuned by the voltage over the related junction. Other technology parameters affecting the collection depth are hard coded inside the Verilog-A model. The two other parameters for SETstriker cell are delays that allows to time the SET event. There is a global delay and an event specific delay. The first parameter is to be used to move all SET events to a certain time in the simulation and the second one to let each event happen one after the other.

C. *Use of Deepprobe*

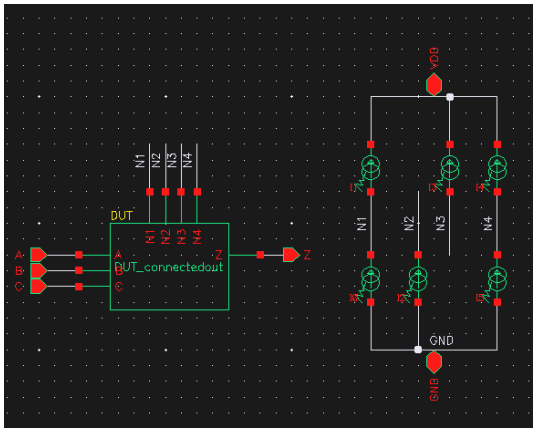

Figure 2: Testbench with DUT with internal nodes connected out

In Figure 2 an example test bench is given that shows how this SETstriker can be used for injection into a Device Under Test (DUT) to investigate its SET sensitivity. In this example N1 and N2 are connected to diffusion area of both a NMOS and PMOS, N2 of only a NMOS and N3 of only a PMOS. The nodes to be injected in the DUT have been connected out which means the design needs to be adapted to allow SET simulation. Especially when there are multiple levels of hierarchy or a lot of nodes in the design this becomes tedious. The deepprobe cell has been introduced to ease this. The schema from Figure 3 performs the same functionality as in Figure 2 but without the need to adapt the design of the DUT. The four instantiated deepprobes allow to connect to the nodes inside the DUT by a hierarchical name given as parameter. The deepprobe is a cell originally downloaded from the Cadence support website and is now available in the analogLib of the latest releases for Virtuoso.

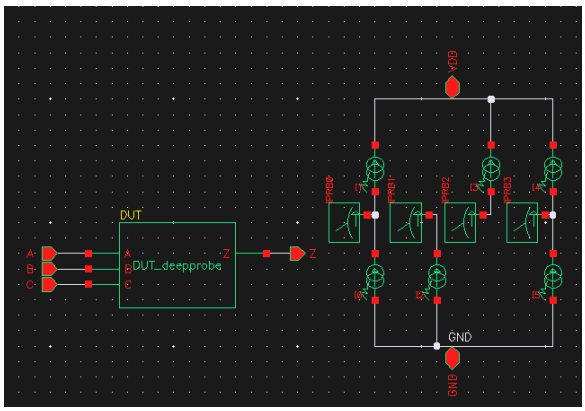

Figure 3: Test bench using deepprobes for injection

D. *Use Periodic SET Striker and Dual Deepprobe*

If a lot of nodes need to be investigated or one wants to focus later on only on a subset of the nodes this setup is still tedious. A SETstriker and a deepprobe needs to be instantiated for each node and the timing has to be set up. For reducing the simulated nodes set, instantiations need to be removed again and the timing of all SETstrikers needs to be updated. Two new cells have been introduced to make this flow more fluent: a periodic SETstriker and a period deepprobe switcher with two inputs. The periodic striker generates events with a specified period and allows to replace all SETstrikers with one in a schema. The periodic deepprobe allows to replace all deepprobes with one. A paremeter of the the deepprobe referes to a text view which list the nodes to connect to. The extension to two inputs of the deepprobe allows to combine the events generated on the diffusion area of both NMOS and PMOS transistor by taking always the n-type region as first node and the p-type region as second node. The cells have some extra outputs that allow to easily monitor the state of the device, e,g, it will show the number of the event and the time the event has started. With the event number the corresponding nodes can be looked up in the nodes list.

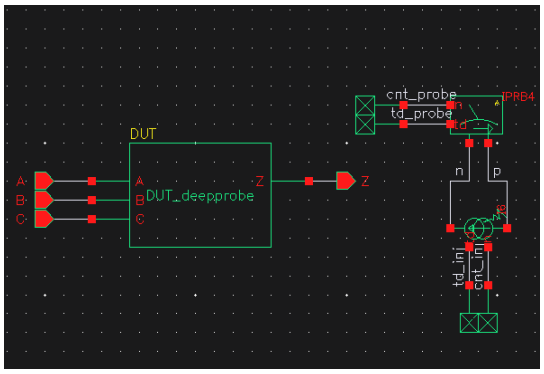

Figure 4: Testbench using periodic striker and deepprobe

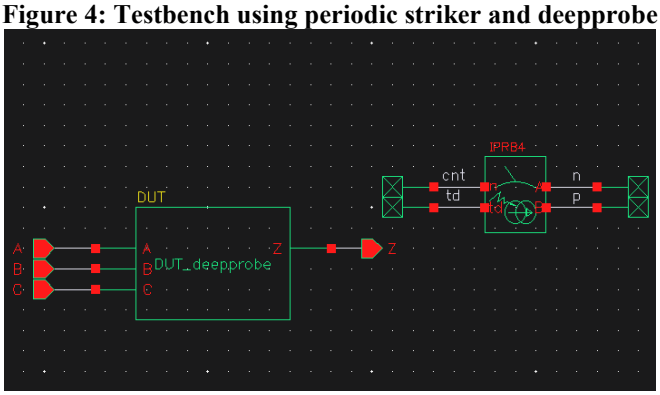

Figure 5: Test bench using combined periodic striker+deepprobe

An updated test bench with the same functionality is shown in Figure 4. Most of the time the periodic probe will be combined with a periodic SETstriker. So for this purpose a cell is provided that combines the two functionalities and is used in the test bench presented in Figure 5; again with the same functionality. The node list is Skill code in text view and has the following content for this test bench:

```
probes = '("Probes")
probes->list = '(
  ("/DUT/N1" "/GND")
  ("/VDD" "/DUT/N1")
  ("/DUT/N2" "/GND")
  ("/VDD" "/DUT/N3")
  ("/DUT/N4" "/GND")
  ("/VDD" "/DUT/N$")
)
```

This text file can be easily edited to add or remove nodes from simulation. So one can easily start with a broad screening of the nodes in the DUT and then later on focus on a small subset of the nodes by editing the file without any other changes needed in the test bench.

E. Using Triggered Striker and Deepprobe

Up to now the SET events generated on the nodes in a DUT have always be done after a fixed amount of time and repeated with a fixed period. Sometimes one would like to start generating events when the DUT has reached a certain state. For this purpose a SETstriker+dual deepprobe are provided that will generate an event triggered by a rising edge on an extra input and a configurable threshold value.

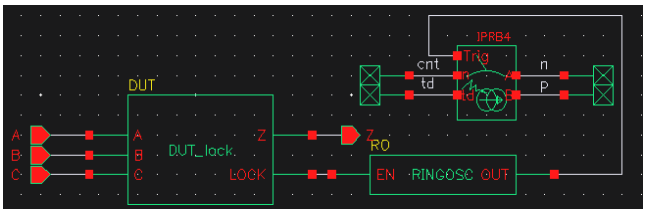

Figure 6: Test bench using combined triggered striker+deepprobe

In Figure 6 this is shown on a test bench where the DUT provides a lock signal – a signal that often is an output of a PLL. The lock signal is used in the test bench to enable an oscillator that drives the trigger for generating the SET events. In this way only events will be generated after the DUT is in lock state. In this example the combined SETstriker+deeppprobe cell with a trigger input is shown but for the separate SETstriker and the dual deepprobe also versions that work on a trigger signal are available.

F. Node Selection GUI Support

With the introduced cells a SET simulation can be performed easily in Virtuoso but generating the list of nodes can still be a labour intensive task and important nodes may be overlooked. For this reason a tool is provided that lists all SET generating junctions in a DUT and allows to select on which nodes to inject a SET.

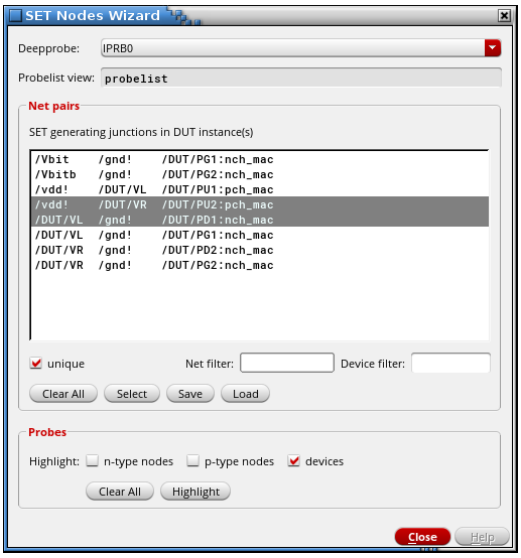

Figure 7: SET sensitive nodes selection and investigation

In Figure 7 the window of the tool is shown when applied to a classic 6T-SRAM cell. A 6T-SRAM cell – as the name indicates - contains 6 transistors: 2 NMOS pull-down transistors, 2 PMOS pull-up transistors and 2 NMOS pass gates. In the GUI a list is provided of all the event generating junctions. The first column lists the net connected to the n-type region of the device, the second column the one to the p-type and the third column the device that contains this junction. The net combinations one wants inject SET events into can be selected from the list and saved in a text view. In this case the two events on the internal nodes were selected that can cause a SEU on a 1 stored in the SRAM cell.

II. Status and Future Work

The current release version of the DARE180U Analog Design Kit (ADK) contains the single event SETstriker and the deepprobe; for DARE65T no ADK is released yet. The plan is to include the updated flow in the next release of both the DARE180U and DARE65T ADKs.

Part of the Verilog-A SETstriker model is based on literature and so not on exactly the same technology as used for DARE. Efforts are ongoing to verify and possibly improve the model. For both technologies TCAD effort is ongoing and for the DARE180U technology a SET test chip is available and waiting for testing.

III. Summary

In this paper the current SET simulation flow as used in imec for the DARE65 project is discussed. An overview of the evolution is given. The current flow allows an analog designer to investigate SET sensitivity and perform radiation hardened by design (RHBD). The flow is built on the Virtuoso design flow and integrates efficiently in a typical analog design flow. In the DARE65 a SET verification test chip is in the planning.

IV. Acknowledgements

This SET simulation and radiation hardened by design flow has been developed within the DARE180 and DARE65 ESA projects. Discussions with ESA experts and the users of our DARE technologies are a big inspiration for the improvements to the flow. Especially the guidance and feedback of Boris Glass and Richard Jansen have contributed to where we are now.

V. References

[1] Imec DARE website: http://dare.imec-int.com/en/home
[2] S. Verhaegen et.al. (2016, June).”Incorporating more in-depth radiation knowledge in the DARE180U analog design kit”. Presented at AMICSA 2016; https://indico.esa.int/indico/event/102/session/9/contribution/48
[3] Rajesh Garg, Sunil P. Khatri (2006) “Analysis and Design of Resilient VLSI Circuits: Mitigating Soft Errors and Process Variations”, Springer
[4] V. Ferlet-Cavrois (2006. December) “Statistical Analysis of the Charge Collected in SOI and Bulk Devices Under Heavy Ion and Proton Irradiation—Implications for Digital SETs”, IEEE Transactions on Nuclear Science, Vol. 53, No. 6

DARE180U New Analog IPs

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Abstract

This paper presents the new DARE180U analog IPs developed in the context of the ESA project: "Microcontroller for embedded space applications: Specification and design verification". This project has been performed in collaboration with Cobham-Gaisler. There are essentially 7 new IPs and 1 IP improved during this project:

- 11 bits Muxed SAR ADC (4/8 channels)
- Extended input range PLL (improvement of existing IP)
- Cristal oscillator
- Power On Reset
- 1.8V and 3.3V voltage monitor
- GPIO with local Power On Control
- High density DP SRAM

All these IPs are hardened against radiation and heavy ions as the rest of the DARE180U platform libraries. If not explicitly defined the hardening level is respectively 300 krad for TID and 60 MeV*cm2/mg for LET (SEL, SET).

I. High Density Dual Port SRAM (DARE180U_HDRAM)

This dual port SRAM uses only 1.8V straight transistor in order to reduce the memory cell area. All other hardening techniques against TID leakage and latch-up are kept. Furthermore, this dual port SRAM has been hardened against MBU on the same word:

- Address path hardened by drive strength.
- Clock path hardened by drive strength.
- Each bits of a same word are separated by 57µm

This memory block has a fixed size of 4096 words of 13 bits for a total area of 2150x590 µm2, let an area reduction of 50% compared to the ELT version.

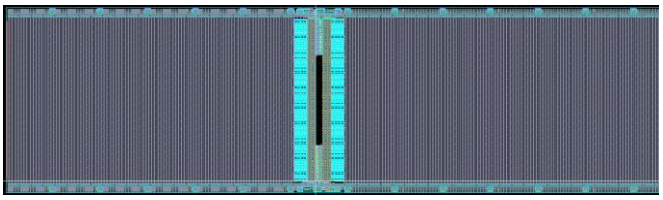

Figure 1: HDRAM layout

II. GPIO with Local POC (DARE180U_GPIO)

This general-purpose IO can be used as:

- Digital input (Schmitt trigger) with programmable pull-up/pull-down
- Digital output (4mA drive)
- Analog input (serial impedance of 50 Ohms)
- Analog output

When configured in digital input/output mode, this IO is completely SET free and uses only ELT layout for NMOS transistors to make it insensitive to total dose radiation effects.

Its local Power-On Control forces the IO output in high impedance mode as long as the core voltage is not turned-on. Practically, this high impedance mode will be maintained after the ramp-up of the core voltage thanks to the Power-On Reset IP placed in the core.

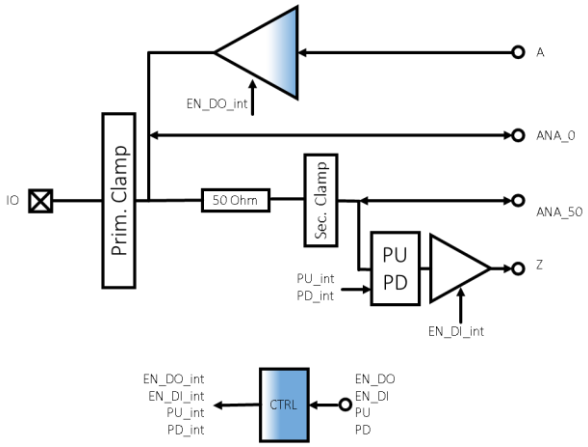

Figure 2: GPIO block diagram representation

III. Voltage Monitor (DARE180U_VMON)

This block monitors the value of the 3.3V and 1.8V power supplies. The detection threshold can be adjusted thanks to 3 bits of configuration from 1.6V till 1.77V for the 1.8V version and from 2.9V to 3.24V for the 3.3V version. To avoid false triggering due to noise on the supply, a filter is used to remove glitches shorter than ~20µs (see Figure 3 and Figure 4 for more detail on the working principle).

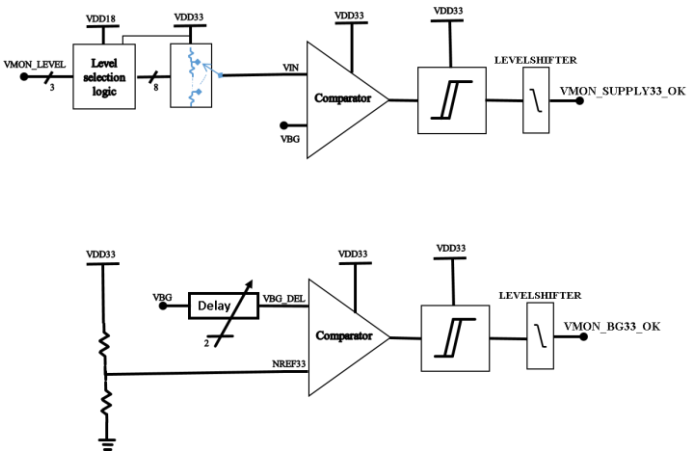

Figure 3: 3.3V Voltage Monitor diagram, with a crude VMON_BG33_OK flag generator

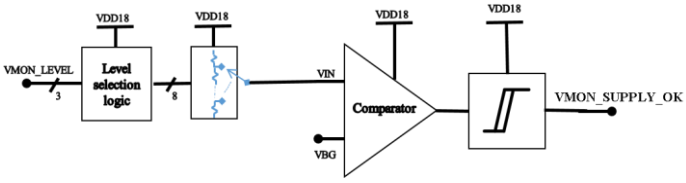

Figure 4: 1.8V Voltage Monitor Diagram

IV. Power-On Reset (DARE180U_POR)

The power-on reset block generates a long reset pulse during the power-ramp up and the power-ramp down of the core supply. The reset pulse duration can be adjusted thanks to an external capacitor. The typical pulse duration value is 235µs without external capacitor and 150ms with an external capacitor of 220nF. Considering the importance of the reset signal, this IP is obviously also SET free till 60 MeV*cm2/mg.

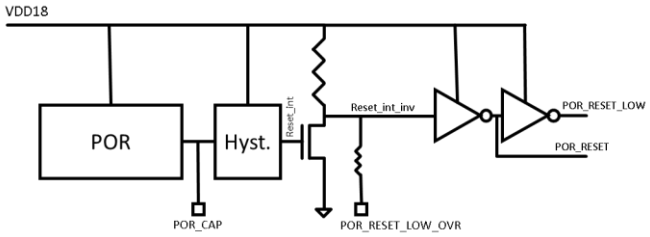

Figure 5: Power- On Reset Diagram

V. Crystal Oscillator (DARE180U_XO)

The crystal oscillator delivers a stable CMOS level clock signal, using an external crystal as input which may range from 5 MHz to 25 MHz. The oscillator is hardened against TID radiation but also against SET: at 60MeV*cm2/mg, no false clock edges shall appear and the maximum period error is about 1.1ns and 3.8ns when running at 25 MHz and 5 MHz, respectively.

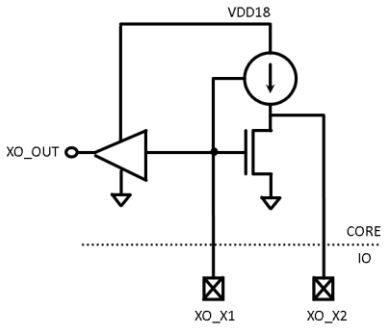

Figure 6: Cristal Oscillator Diagram

VI. Extended Input Range PLL (DARE180U_PLL_EXT)

The Phase-Locked Loop (PLL) IP generates an output clock frequency that is an integer multiple of the input signal frequency. The ratio between the input frequency and the VCO frequency can be programmed to 8, 16, 20, 32, 40 and 80. The VCO of this PLL has been optimized from the radiation hardening point of view when running at 400MHz. At this VCO oscillation frequency, an SET (60MeV*cm2/mg) will cause no false edges and the PLL output phase error will not exceed 160ps (or 600ps, when running at 280MHz). In absence of SET the PLL output signal shows a jitter of 600fs in typical conditions when VCO frequency is 400MHz.The power-on reset block generates a long reset pulse during the power-ramp up and the power-ramp

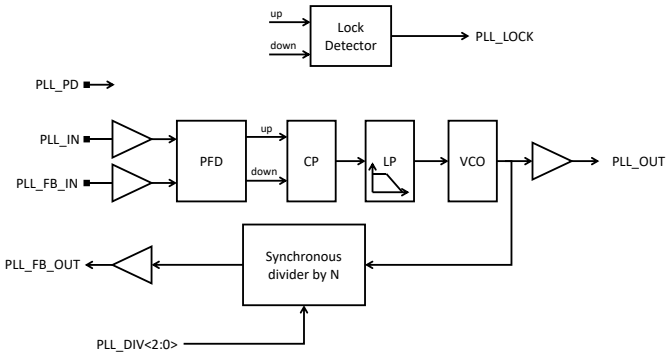

Figure 7: Extended PLL diagram

VII. 11-bit SAR ADC (DARE180U_ADC)

This IP is composed of mainly 2 blocks:

- An 8:2 analog mux combined with an auto zeroed-amplifier (0dB, 6dB and 12dB).
- A SAR ADC configurable in differential or single-ended mode (11-bit interface, ENOB WC of 10 bits at 300kS/s) with an internal voltage reference (external capacitor free).

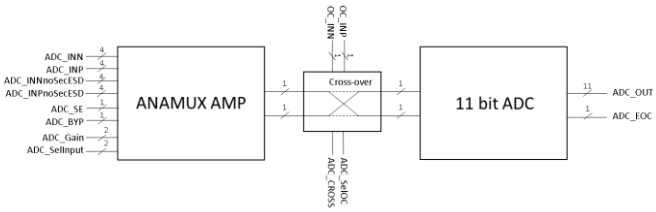

Figure 8: 11-bit SAR ADC diagram

All the digital is hardened against SET and SEU:

- Only radiation hardened flip-flops (HIT) are used.
- Data out bits are SET free by means of a Muller-C filter.
- Clock paths hardened by drive strength.
- Signals driving the switches connecting the capacitors to the voltage reference are not SET free up to 60 MeV*cm2/mg. However, any SET on these signals will be filtered thanks to the limited analog bandwidth of the capacitor bank.

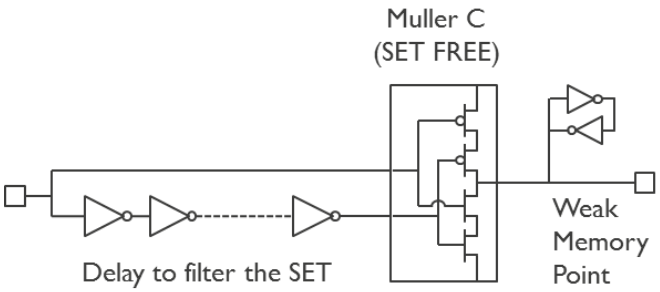

Figure 9: Muller-C SET filter diagram

The capacitor matrix and their switches are insensitive to SEU (i.e. permanent capacitor charge error) except on the capacitor bank side connected to the comparator. Indeed, if during the conversion a charge is injected when the switches connecting the capacitors to the voltage references are on, this charge is stored in the capacitor bank. However, the sensitive junction area of these switches in differential mode is 2*120µm2, meaning that only few events on the total duration of a space mission.

The comparator itself is not completely immune to SET but its cross-section is quite low thanks to its auto-zeroing and represents only few events during one complete space mission (sensitive area of 80µm2 when 2mVdifferential (i.e. 1 LSB) at the comparator input @0.1 MeV*cm2/mg => ~50 event/year with 100 mils Al shielding).

VIII. ACKNOWLEDGMENT

We would like to acknowledge our partner for this project Cobam-Gaisler and in particularly Fredrik Johansson and Roger Malmberg.

DARE180U Platform Improvements in Release 5.6

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Abstract

DARE180U, formerly named DARE180, is a mixed-signal ASIC design platform intended for radiation hardened applications up to 1 Mrad implemented in the commercial UMC L180 MM/RF 1.8V/3.3V, Single Poly 6 Metal (1P6M), P-Sub/Twin-Well CMOS technology. Over the years, DARE180U has been adopted by several partners around the world as a cost-efficient and flexible solution for space applications. Recently, hundreds of chips implemented with this platform have been launched in a commercial geostationary mission, granting the technology TRL-9 qualification status.

Release 5.6 is a major step forward in the DARE180U solution as it brings together extensive knowledge acquired in the past years from various application designs and test chips. This paper presents the updates in this release including general platform improvements and new additions to existing libraries and IP.

I. Introduction

Deep submicron commercial technologies have been qualified for several years as a cost-efficient and flexible solution for mixed-signal space applications enabled by thin gate oxide radiation properties in combination with special design and layout techniques [1].

The DARE180U platform provides a mixed-signal design solution in the commercial UMC 0.18 µm technology that has been validated in several flight models [2][3] and successfully employed in satellite missions that granted it highest technology readiness level status [4].

Over the years, DARE180U libraries and IP have undergone constant updates following requests from an increasing number of partners. Before version 5.6, a major improvement had been made in the ESA funded DARE+ project, where new blocks were added to fully support mixed-signal designs. DARE+ project also introduced the first DARE180U SRAM compiler and included extensive TID and SEE radiation tests.

For version 5.6, DARE180U libraries have further combined design experience from recent commercial projects along with a deeper knowledge over the radiation behaviour of devices measured on DARE+ test chips. In addition to reliability improvements, version 5.6 also includes new features that expand its application range, particularly for mixed-signal products.

II. Platform Updates

A. New ELT Modelling

Previous versions of DARE180U libraries relied on the classical CERN model for ELT devices that computes equivalent W/L based on enclosed gate dimensions [5]. Although this model gives a good approximation for MOS transistor driveability, gate capacitance is largely underestimated due to simplified BSIM3 modelling which derives gate capacitance from the W*L product and assumes that gate-drain and gate-source area overlaps are symmetric. In reality, gate area in a minimum size ELT transistor turns out to be 30% higher than the value computed with equivalent W and this ratio increases for larger transistors [6].

Test measurements in DARE+ project supported by the European Space Agency have been used to fine-tune the ELT simulation model to obtain more realistic characterization results. I-V measurements have validated the accuracy of CERN formula for NMOS transistors and provided a correction factor for PMOS transistors which were found to have about 5% weaker drive than calculated equivalent W/L. In this fine-tuned model, calculation of gate channel and gate overlap capacitances has also been adapted to consider geometrical aspects of enclosed gates instead of equivalent W and L dimensions [6].

This new simulation model is provided as part of the latest DARE180U ADK which has been used for verification and characterization of all libraries in release 5.6.

B. Full-Custom Design Support

Radiation hardening reliability using the DARE180U platform depends not only on design techniques employed in each library cell but also on the way top-level design combines all building blocks together, especially within digital core blocks and I/O rings. For this reason, top-level implementation is carried out by the design team at imec for guaranteed reliability.

Nevertheless, in an effort to assist DARE180U users designing their own IP blocks, full-custom views have been included in the release 5.6. These views include encrypted netlists for Spectre simulation, black-box abstracts and netlists for top-level layout verification. Cell replacement and final layout verification with regard to radiation hardening is performed at imec.

III. Library Improvements

A. Standard Cell Core Library

1) Layout Optimization

Radiation hardening layout techniques, such as enclosed transistors (ELTs) and guard-rings, cause considerable area overhead on digital core designs. In release 5.6, DARE180U standard cell layouts have been fully reviewed to minimize area and maximize P&R efficiency as well as to optimize radiation hardening performance.

More compact cell layouts have been obtained for several cells through better transistor ordering and more efficient dimensioning of ELTs. However, core area in large designs has shown little reduction using these new layouts, as shown in Table 1. Cell pins and internal routing on higher metal layers have been rearranged and aligned to the routing grid in order to reduce top-level routing congestion and parasitics.

Table 1: Core area comparison

Chip Design	Area v.5.5 [mm^2]	Area v.5.6 [mm^2]	Ratio [%]
Chip A	40.146	39.803	-0.85%
Chip B	20.994	20.904	-0.43%
Chip C	14.819	14.634	-1.25%

Layout improvements have also considered optimization of SET behaviour by means of reduced diffusion sensitive area. Enclosed transistors have been reordered to connect large outer diffusion areas to less critical nodes wherever possible. Large ELTs have been split in additional fingers and/or reshaped to less squared aspect ratios, which provide a better trade-off between drain/source area (i.e. sensitive area) and equivalent transistor width. Changes in circuit topologies have also been made in selected cells to improve LET threshold of critical nodes by resizing transistors, reducing internal stages and/or removing long transistor stacks.

Further layout improvements have been made to boost electrical behaviour and overall radiation reliability, such as the increase of tap contacts and guard-rings. Diffusion contacts around ELTs have been rearranged and increased to enhance current flow through drain/source nodes and provide better correlation between characterization results and actual electrical behaviour. Figure 1 depicts different layout changes described above.

2) Triplication Support

A triple majority voter cell has been added to the core library to support triple modular redundancy (TMR) implementation.

In certain digital blocks, TMR implementations using non-SEE hardened core cells may prove more area and/or power efficient than the usual DARE180U design approach based on SET hardened-by-drive-strength paths for asynchronous signals combined with SEU hardened sequential cells

3) Characterization

The core library has been recharacterized using the new ELT models in an attempt to deliver more realistic timing results. In addition, fine-tuned characterization settings have been employed to improve synthesis efficiency by reducing interpolation errors.

Table 2 shows a performance comparison between version 5.6 and previous release that indicates the effects of the new ELT models on performance, particularly because of increased input gate capacitance. A greater degradation on rise delay has also been observed due to the correction factor applied on equivalent W/L calculation for PMOS transistors.

B. I/O Library

Previous analog and digital I/O libraries have been combined in a single library with extended support for multi-domain I/O ring implementations. New I/O cells have been created in addition to a whole new set of analog I/O cells featuring 1.8V ESD protections for the implementation of 1.8V analog I/O domains. As well, several improvements have been done on layouts to enhance ESD behaviour and electromigration reliability.

C. Bond Pad Library

A new bond pad cell library has been added to the DARE180U platform featuring a larger set of bond pad opening size choices. As well, special double bond pad cells tailored for selected DARE180U IPs are now available for chips implementing large pad pitches. All bond pad structures have been optimized in this version to provide minimal parasitic capacitance.

D. Mixed-Signal IP

Existing DARE180U IP, such as PLL and LVDS blocks, have also been updated to attend new specification requirements and to fix existing issues reported in previous application chips. As well, new IPs implemented at imec have been added to the platform, including SAR ADC, crystal oscillator, power-on reset generator, voltage monitors, among others [7].

IV. SRAM Compiler

The DARE180U SRAM compiler can generate both single and dual-port SRAM blocks ranging from 256 bits to 256 Kbits with different bit interleaving options. Memory bit cells employ enclosed transistors to reach the high TID specifications of the DARE180U platform. MBU insensitivity can be achieved by using blocks with reasonable bit interleaving distances in combination with external error detection and correction circuits.

In this new release, the existing DARE180U SRAM compiler has been reviewed to deliver full-custom views and more accurate characterization data based on the new ELT models.

V. Further Work

In the roadmap for the DARE180U platform, new features are planned to further extend its application range, particularly for the I/O library with the implementation of power-on control, general purpose I/O cells and full 1.8V digital I/O cells.

VI. Acknowledgements

The authors would like to thank the European Space Agency for their continuous support on the DARE180U platform.

VII. References

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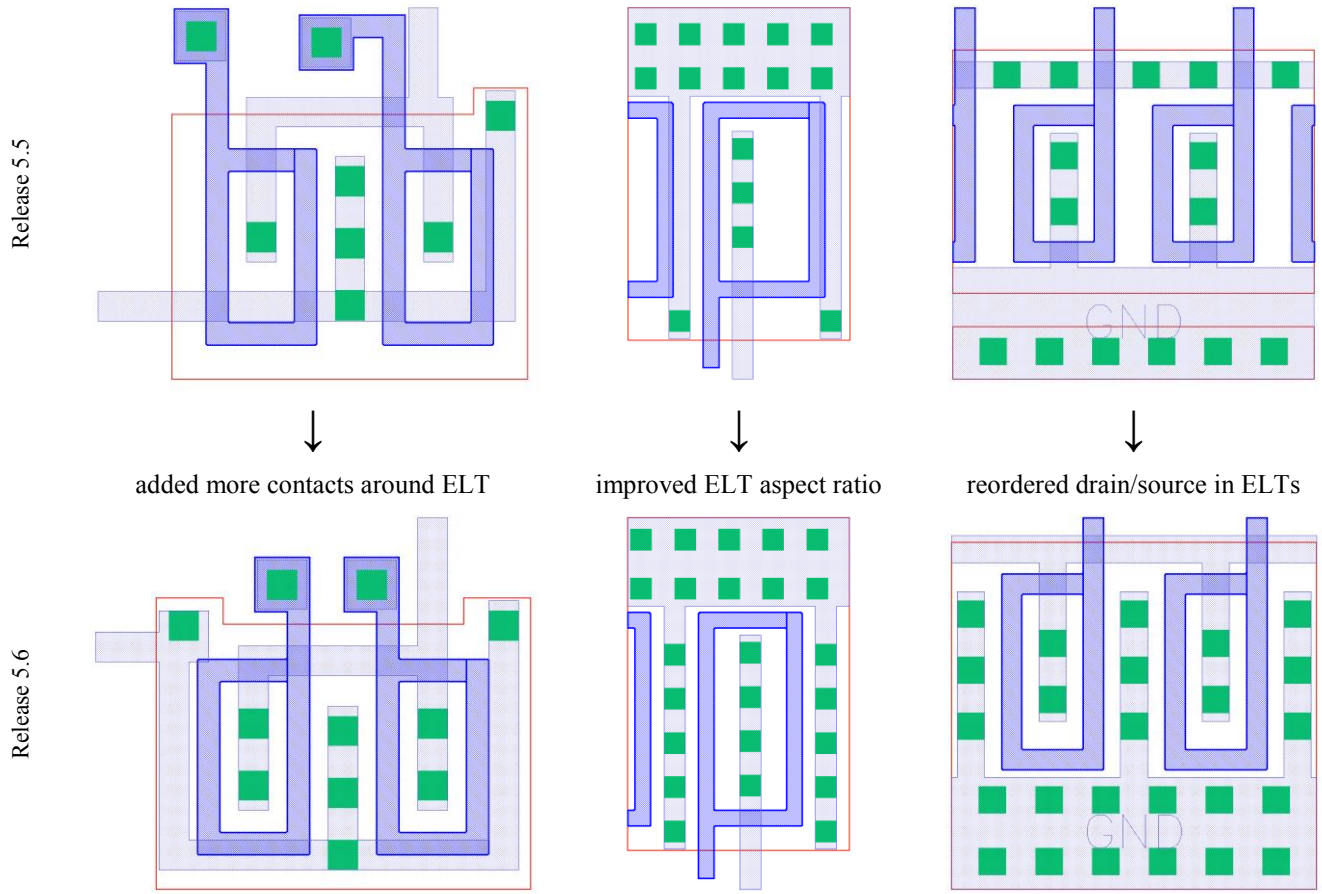

Figure 1: Core library ELT layout improvements in release 5.6 (bottom row)

Table 2: Core performance comparison

Corner	Timing Figure	Version 5.5	Version 5.6	Ratio
WCMIL (ff, 125°C, 1.62V)	FO4 rise delay	140 ps	154 ps	+ 9.1%
	FO4 fall delay	126 ps	135 ps	+ 6.7%
	128-gate ring oscillator frequency	29 MHz	27 MHz	- 7.4%
TYP (tt, 25°C, 1.8V)	FO4 rise delay	94 ps	104 ps	+ 9.6%
	FO4 fall delay	80 ps	85 ps	+ 5.9%
	128-gate ring oscillator frequency	45 MHz	41 MHz	- 9.8%
BCMIL (ss, -55°C, 1.98V)	FO4 rise delay	70 ps	77 ps	+ 9.1%
	FO4 fall delay	55 ps	59 ps	+ 6.8%
	128-gate ring oscillator frequency	62 MHz	58 MHz	- 6.9%

ATMX150RHA Circuit Design Platform

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Abstract

The ATMX150RHA proposed by Microchip is a highly adaptable ASIC offering addressing design either for digital, analog or mixed signal products.

The ATMX150RHA is based on a 150nm SOI Microchip proprietary process technology, fabricated by UMC foundry.

This ASIC offer is largely based on ATC18RHA heritage extensively used to design digital ASICs for space applications. Additional features to address analog and mixed signal design needs have been included in design kit.

As already done for digital design perimeter, Microchip is aiming to extend qualification domain to analog or mixed signal ASIC usage, through proposal of pre-qualified analog IP catalogue and a strategy built around a standard evaluation circuit and a generic test vehicle platform dedicated to analog IPs validation.

Preliminary test results of some of these IPs, including over radiation, are detailed in this presentation.

I. Design Kit Contents

Depending on the design flow used by the customer, libraries information are provided on different format. The design kit target to provide behavioural, physical and timing models, whatever design flow used.

A. Digital On Top Design Flow

A Design Kit is provided, containing physical models, behavioural models and timing models for IOs, standard cells and analog IPs, in order to be used in with digital design tools.

Already proven with ATC18RHA, the same methodology was reused for the ATMX150RHA.

For each library, standard cells, IOs and analog IPs, are delivered:

- Timing models (.lib/.db files)
- Behavioural models (Verilog, vital)
- Physical models (LEF and Milkyway)

B. Analog On Top Design Flow

The ATMX150RHA is a derivative of a process technology extensively used by Microchip automotive group for analog design.

In an Analog on Top design flow, development is based on PDK, and usage of libraries, provided in Cadence database format (OpenAccess). Simulation of these libraries are performed with transistors models included in PDK (Spectre, Hspice and Eldo)

The Cadence libraries for Analog on Top design flow contains, for standard cells and IOs:

- Symbol
- Schematic
- Layout

Regarding analog IPs, the libraries are provided with:

- Symbol
- Layout black box
- Encrypted netlist

Allowing simulation at transistor level on a whole circuits, with Microchip Libraries.

C. Mixed Signal Design Flow

Mixed signal circuit can be addressed either using analog or digital on top design flows.

Digital macros have to be designed with digital design tools, and then imported in Analog design tools, in case of Analog on Top flow.

In a Digital on Top design flow, analog IPs can be used directly in Digital design tools thanks to behavioural, physical and timing models.

II. Technology Qualification Extension to Analog and Mixed Signal Usage

Microchip ATMX150RHA is qualified for a digital domain up to a NAND2 equivalent 22Mgate, both QML and ESCC referential.

In order to extend current qualification domain to analog mixed signal usage, Microchip has decided to use its internal qualification process, based on a Standard Evaluation Circuit and an Analog Test Vehicle generic platform.

On one side, the Standard Evaluation Circuit is quarterly fabricated, has defined by standards [1, 2], and is used for the technology monitoring.

On the other side, the Analog Test Vehicles embeds a set of analog IPs, and are qualified through a Microchip internal qualification flow, as standards did not define yet a qualification process regarding analog and mixed signal circuit design.

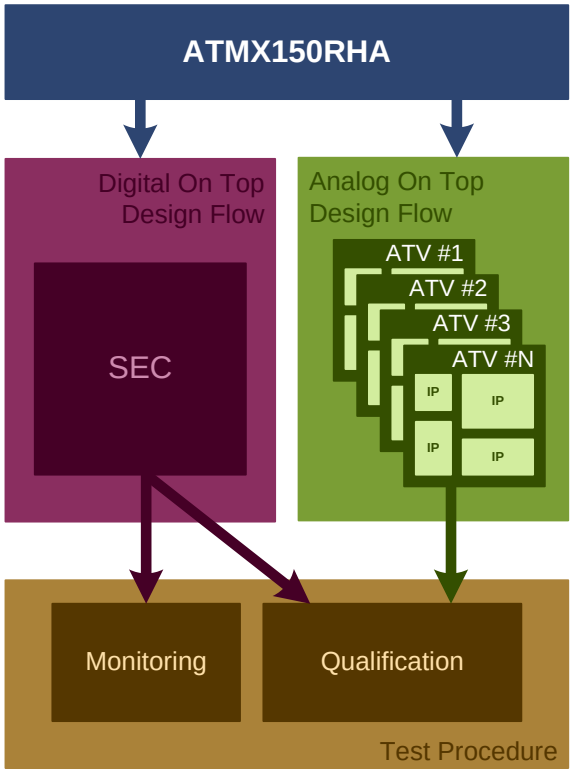

Figure 1: ATMX150RHA Qualification Flow

A. *Standard Evaluation Circuit*

The Standard Evaluation Circuit is developed through a Digital on Top design flow. The design supports digital qualification domain up to 22Mgates, and embeds additional analog features.

A set of representative analog IPs have been implemented:

- Linear Voltage regulator
- Bandgap Voltage reference
- Internal oscillator
- Phase locked loop
- Analog multiplexer

Additionally, Microchip embeds a monitoring macros based around simple analog elements, design around whole components available through the PDK. These specific monitoring cells are based around:

- 27 ring oscillators design with different devices oxide thickness, types and geometries
- 2 bandgap voltage reference, design with NPN or PNP bipolar transistors
- 6 differential amplifiers, design using different topologies, devices oxide thickness and type
- 14 elementary devices used as power elements

B. *Analog Test Vehicle*

In addition to the SEC, a generic test vehicle frame, to reduce cost and increase flexibility, has been developed by Microchip.

This platform is used to test and qualify analog IPs, in a standalone configuration.

When new IPs are available, a new design of test vehicle is done, while Standard Evaluation Circuit is not updated.

III. ATMX150RHA Analog IPs

Several analog IPs were developed in the frame of the ITT7794 and also for internal needs using the ATMX150RHA process technology, in order to establish a qualified analog IPs catalogue to serve the ASIC offer.

All these IPs were hardened according well documented techniques [3] and using technology characteristics.

The ATMX150RHA technology allows usage of deep trench oxide, in order to isolate NMOS from PMOS, and avoid SEL. Deep wells below low voltage area is also processed, to reduce the gain of the parasitic thyristor and decrease SEL sensitivity.

ATMX150RHA PDK includes enclosed layout Pcells concerning thick oxide nmos transistor, to reduce TID variation of these devices. These devices topology have been characterized and spice model is included in PDK.

Analog sensitive nodes have been hardened mainly using redundancy and averaging techniques.

Digital sensitive nodes were hardened inserting dummy transistors [4].

A. *Library and Analog IPs Catalogue*

A catalogue of qualified analog IPs is under construction, in order to enhance Microchip ASIC offer around the ATMX150RHA. This offer already contains qualified IOs, standard cells and PLL to address digital circuit requirements.

Table 1: Analog IPs catalogue

IP Name	Description	Current Status
IO18253350RHA	IO pads library	Field release
SCLIB	1.8V Standard cells	
PLL400MRHA	40-400MHz PLL	
REG200RHA	LDO Voltage regulator 1.8V 200mA	
BG1V2RHA	1.2V Bandgap Voltage Reference	Ongoing Characterization
MUX8RHA	8-Channel multiplexer	
OSCRC10MRHA	4/8/10/12 MHz Internal oscillator	
OSCRC32KRHA	32kHz internal oscillator	
OSCXT32KRHA	32kHz XTAL oscillator	
OSCXT20MRHA	20MHz XTAL oscillator	
POR18RHA	Power-on-reset	
IORHA	Programmable IO pads	
REGD600RHA	Fully integrated DCDC 1.8V 600mA	Ongoing development
REGA20RHA	Fully integrated low noise LDO 1.8V 20mA	
ADC12RHA	ADC 12 bits 1Msps	
IOHVRHA	High voltage programmable IO pads	
DAC12RHA	DAC 12bits 2Msps	Planned

B. Rad Hard Analog IPs Test Results

Radiation testing sessions were performed in TAMU (Texas, USA) facilities, regarding single event, and exposed to TRAD (Toulouse, France) cobalt source, regarding total ionizing dose.

Test conditions applied to analog IPs radiation testing are described below:

- Total Ionizing Dose was tested up to 150krad(Si) @300rad/h and 25°C
- Single Event Transient was tested up to 65MeV.cm²/mg @25°C ambient temperature and minimum supply
- Single Event Latch Up was tested up to 65 MeV.cm²/mg @125°C ambient temperature and maximum supply

1) Low Dropout Voltage Regulator (REG200RHA)

The REG200RHA is a radiation hardened linear voltage regulator, embedding its own voltage reference, and including power on reset and power fail detector.

It operates from 5.5V down to 3V and provides a fixed 1.8V output voltage while sourcing up to 200mA of load current.

Test results, in the table below, report a greater than expected variation on V_{out} voltage value over TID. This was analysed as a bipolar NPN transistor sensitivity.

Table 2: REG200RHA test results

	Description	Min.	Typ.	Max.	Unit
V_{in}	Supply Voltage	3.0	3.3	5.5	V
Temp.	Junction Temperature	-55	27	145	°C
C_{load}	Decoupling cap.		470		nF
V_{out}	Output voltage	1.75	1.8	1.82	V
I_{vdd}	Current consumption			450	µA
$\Delta V_{OUT(\Delta VIN)}$	Line regulation			1	%
	Transient line reg. @1V/µs			2	%
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation			1	%
	Transient load reg. @100mA/µs			2	%
V_{POR}	POR Threshold	1.57	1.6	1.63	V
V_{PFDf}	Falling PFD Threshold	1.61	1.64	1.67	V
V_{PFDr}	Rising PFD Threshold	1.66	1.69	1.67	V
V_{out}TID	Output voltage variation			50	mV
V_{por} TID	POR Threshold variation	to be tested			
V_{pfd} TID	PFD Threshold variation	to be tested			
V_{out} SET	Output voltage event	no event observed			
V_{por}SET	POR Threshold event	no event observed			
V_{pfd} SET	PFD Threshold event	no event observed			
SEL	Latch up events	no event observed			

2) RC Oscillator 4/8/10/12 MHz (OSCRC10MRHA)

The OSCRC10MRHA is a radiation hardened, programmable RC oscillator providing a 4/8/10 or 12MHz typical frequency clock signal.

Characterization results, summarized below, did not report any sensitivity to radiation, for both TID and single event.

Table 3: OSCRC10MRHA test results

	Description	Min.	Typ.	Max.	Unit
V_{dd}	Supply Voltage	1.65	1.8	1.95	V
Temp.	Junction Temperature	-55	27	145	°C
F	Output frequency	3.9	4.02	4.14	MHz
		7.95	8.1	8.28	
		9.84	10.1	10.23	
		11.94	12.2	12.44	
DC	Duty Cycle	48	50	52	%
I_{vdd}	Current consumption			640	µA
F TID	Output frequency variation			1	%
F SET	Output frequency events	no event observed			
SEL	Latch up events	no event observed			

3) Bandgap Voltage Reference (BG1V2RHA)

The BG1V2RHA is a radiation hardened bandgap voltage reference which delivers a 1.215V voltage value.

This is a trim less voltage reference, achieving an 80ppm/°C maximum temperature variation over -55°C to 145°C range.

This design was developed around a PNP bipolar architecture. This bipolar device demonstrates a lower sensitivity to TID than the NPN one.

Table 4: BG1V2RHA test results

	Description	Min.	Typ.	Max.	Unit
V_{dd}	Supply Voltage	3.0	3.3	3.6	V
Temp.	Junction Temperature	-55	27	145	°C
V_{bg}	Output voltage	1.209	1.223	1.233	V
I_{vdd}	Current consumption			50	µA
T_{co}	Temp. Coefficient			80	ppm/°C
V_{bg}TID	Output voltage variation			2	mV
V_{bg}SET	Output voltage events	to be tested			
SEL	Latch up events	no event observed			

IV. Conclusion

The ATMX150RHA offer aims to cover qualification of digital, analog and mixed signal ASICs.

To extend current digital qualification domain, a strategy has been developed by Microchip, in order to address customer needs about analog and mixed signal increasing demands.

The analog IPs catalogue is under development, and first silicon results have demonstrated that hardening methodology implemented through technology, design and layout are suitable for space applications.

V. References

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Microchip ATMX150RHA Rad-Hard CMOS 150nm cell-based ASIC family Radiation Characterization Test Report Total Dose (TID) and Single Event Effects (SEE)

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Abstract

Leader of Microcontroller, Mixed-Signal and ASICs solutions for 30 years, Microchip has developed a large ASICs offer based on 0.8µm to 150nm technologies.

The ATMX150RHA ASICs offer is based on 150nm SOI proprietary technology with a Rad-Hard process and standard cell Library. This technology is powered with a supply voltage of 1.8V for core and 3.3V for periphery.

The ATMX150RHA will be qualified through ESCC and DLA standards for ASICs solutions of up to 22 million routable gates.

Mixed-signal challenge has been addressed through a fully electrical and radiation characterization of elementary devices, using different test chips: Standard Evaluation Circuit (SEC) & Analog Test Vehicle dedicated to:

- Digital blocks: hardened standard-cells, hardened Flip-Flops & compiled memories
- Analog IPs: Voltage regulator & reference, clock synthesizer & signal conditioning

A large choice of devices is available as MOS 1.8V, 3.3V, 5V, 15V and LDMOS 25V&45V, developed and simulated in the range of -55°C to 145°C junction temperature.

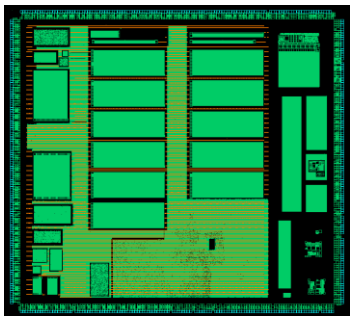
This paper presents the current radiation overview of the ATMX150RHA devices contained in the PDK. The following items are covered: Single Event Latch-up (SEL), Single Event Transient (SET) & Single Event Upset (SEU), Single Event Gate Rupture (SEGR) & Single Event Burn-out (SEB) for HV devices and finally Total Ionizing Dose (TID).

I. INTRODUCTION

This report is devoted to the radiation characterization of ATMX150RHA, and gives a summary of the main radiation results obtained on elementary devices. The quality assurance grade is given for each device, and the associated electrical rules and recommendations are given for space applications.

II. ATMX150RHA TEST VEHICLE

The radiation capability of the ATMX150RHA has been determined using a dedicated test vehicle (002OP, 168mm²). This test vehicle contains a set of memory blocks (compiled memories with and without EDAC), shift registers chains and a PLL.
A total number of equivalent NAND2 gates of 11 million is used.



The different memory blocks included in the test vehicle are given in table 1.

Type	Compiled		Synthesized	
	Standard	SEU Hardened	Standard	SEU Hardened
SRAM	16k32mux16 (x3) 12k39mux16	12k39mux16 with EDAC	128x32 16x32	128x32 16x32
DPRAM	2k8mux16 6k39mux16	6k39mux16 with EDAC	64x32 16x32	64x32 16x32
TPRAM	1k16mux4		128x32	128x32

Table 1:Memories available in the ATMX150RHA test vehicle

A set of register chains is as well implemented. As shown in the figure1, each chain is composed of two identical sub-chains with a XOR to compare their outputs.

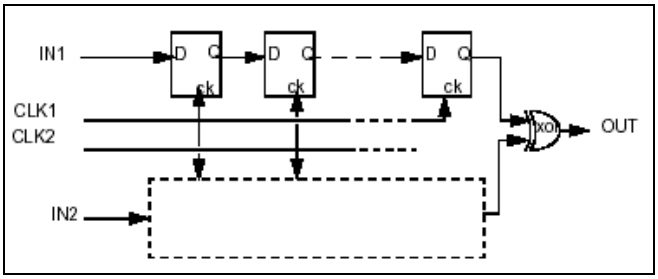


Figure 1: register chains implementation

In standard operation, whatever the data IN pattern, the XOR output shall be '0'. If a single event upset (SEU) occurs in one flip-flop, then the XOR output will change. The clock separation allows to test separately the two subchains and the XOR itself.

Nine chains of 1024 stages each are implemented with the following flip-flops (one chain for each type of DFF):

- standard DFFs (sdbrb1&2, dfnrb1&2)
- SEU hardened DFFs (hsdbrb1&2 hdfnrb1&2)
- A TMR (Triple Modular Redundancy) triplet using dfnrb1 cells

In addition, the test vehicle includes a PLL with a hardened feedback divider (PLL18RHAF500M) and IO33 buffers.

III. Single Event Latch-up

The ATMX150RHA technology, using a Partially Depleted SOI is naturally SEL immune by implementation of Deep-trench capability. Nevertheless, Microchip has developed a high density processed solution for digital and compiled memories to keep SEL immunity without using Deep Trenches.

During the SEL test, each individual DUT power supply is monitored to detect any current increase above a given threshold. The bias voltage is set to the maximum Vcc; 1.95V for core and 3.6V for IOs. The junction temperature is set to 125°C, and is controlled by the I(V) measurement of an input diode within the DUT.

The SEL tests have been performed at HIF UCL, Louvain La Neuve, Belgium, at high temperature (junction temperature of 125°C) and high voltages (1.95V for core and 3.6V for IOs).

No SEL has occurred on 3 parts in a static mode up to a LET of 78.2 MeV.cm²/mg (range = 32µm) with a fluence of 1E+7#/cm². These results enable to validate the SEL level at 78.2MeV.cm²/mg on this technology.

IV. Single Event Effect

This paragraph shows the SEU results of the compiled memories and the DFF followed by an analysis synthesis (Weibull and associated Soft Error Rates).

1) Standard compiled memories

The following test results have been obtained for the various types of compiled memories available in the ATMX150RHA library. The curves of figure 2 to figure 9 present the SEU/MBU cross sections for LET obtained on 3 different DUT parts.

(a)SRAM blocks

The Single Bit Upset (SBU) SRAM threshold LET (LET_{th}) is 1 MeV.cm²/mg for both the SRAMs (16k32 and 12k39). The SBU saturated cross section of the 16k32 block is equal to 3.61E-2 cm²/device (fig. 2) and 2.85E-2 cm²/device for the 12k39 SRAM block (fig. 3).

The maximum MBU's cross section of the 16k32 SRAM block is inferior to 1.74E-3 cm²/device with a LETth close to 2MeV.cm²/mg.
The maximum MBU's cross section of the 12k39 SRAM block is equal to 2.84E-3 cm²/device with a LETth close to 2MeV.cm²/mg.

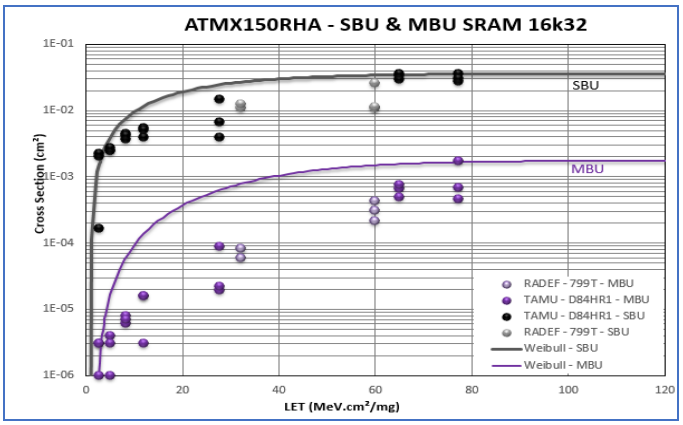


Figure 2: SBU and MBU cross sections (cm²/dev) = f(LET) - 16k32mux16 SRAM – 02FU 3 parts used

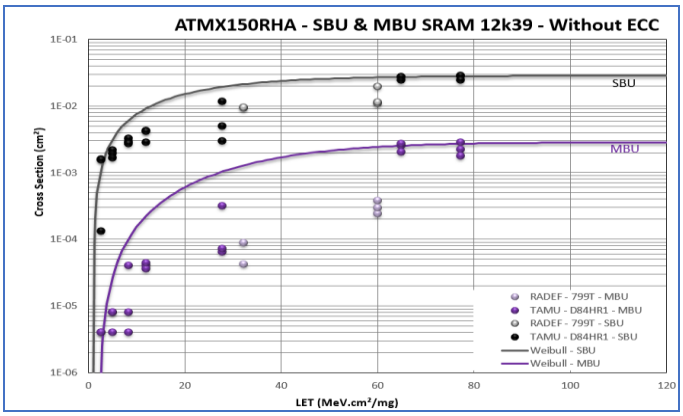


Figure 3: SBU and MBU cross sections (cm2/dev) = f(LET) - 12k39mux16 SRAM – 02FU – 3 parts used

(b)DPRAM blocks

The maximum SBU cross section of the 2k8 DPRAM is 1.15E-3 cm²/device while the maximum SBU cross section of the 6k39 DPRAM block is 1.95E-2 cm²/device (fig. 4 and 5). The LETth of both DPRAM blocks is 1MeV.cm²/mg.

About the MBU, only 1 event appears on the 2k8 DPRAM block at 60 MeV.cm²/mg.
The maximum MBU cross section of the 6k39 DPRAM is 2.43E-3 cm²/device, and the MBU LETth is close to 2MeV.cm²/mg.

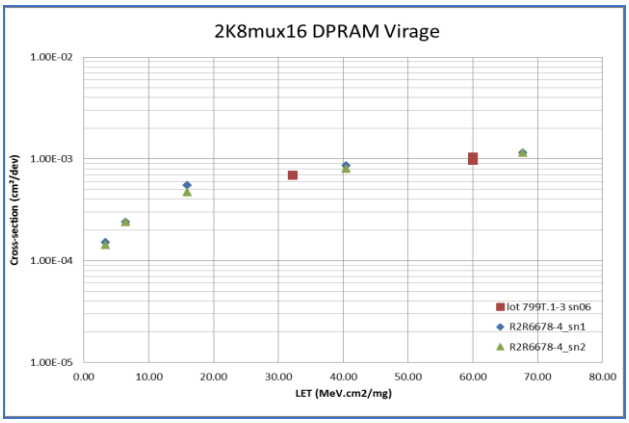


Figure 4: SBU cross section (cm2/dev) = f(LET) - 2k8mux16 DPRAM – 02FU – 3 parts used

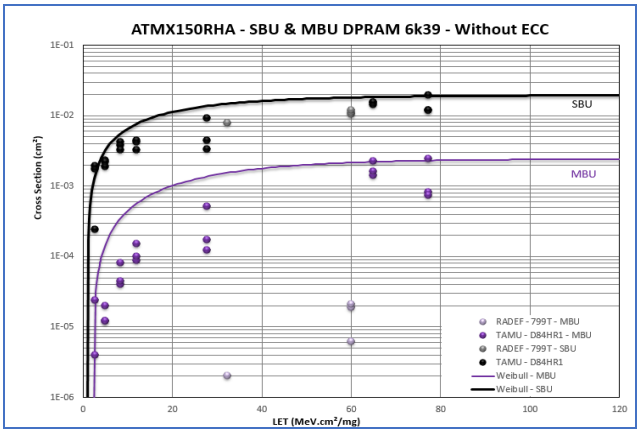


Figure 5: SBU and MBU cross sections (cm2/dev) = f(LET) - 6k39mux16 DPRAM –02FU – 3 parts used

(c)TPRAM blocks

The 1k16 TPRAM block shows a maximum cross section of 5.5E-4 cm^2/device, and a LET_{th} close to 1 MeV.cm^2/mg (figure 6).

No MBU is noticed on the TPRAM.

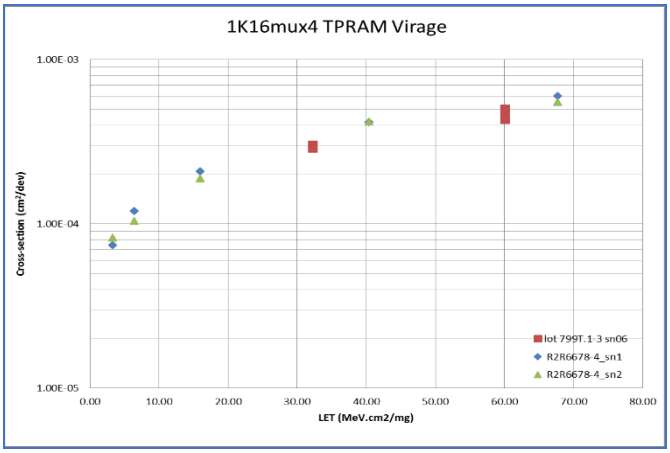


Figure 6: SBU cross section (cm2/dev) = f(LET) - 1k16mux16 TPRAM – 02FU – 3 parts used

2) Hardened compiled memories

Some SRAM and DPRAM memories are hardened by use of Error Correction Code with a 7-bit hamming code (2 errors detected, one error corrected). The results are presented in figures 7 and 8.

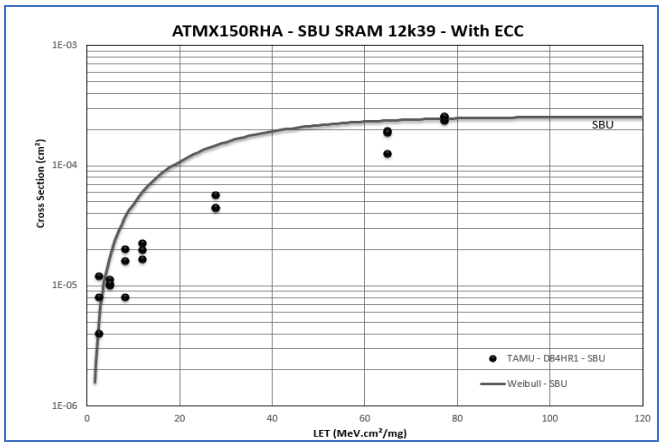


Figure 7: SBU cross section (cm2/dev) = f(LET) - 12k39mux16 SRAM with ECC – 02FU – 3 parts used

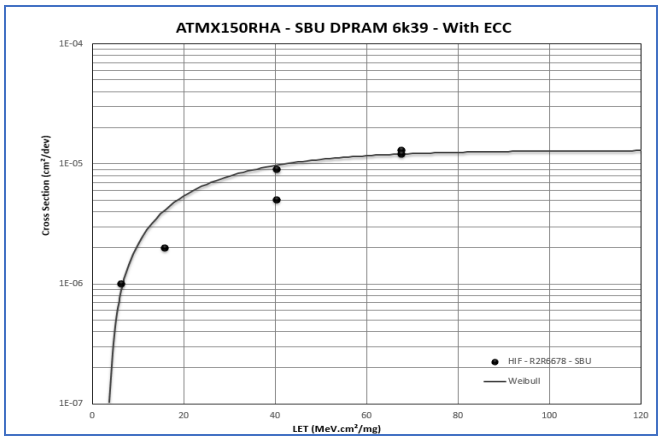


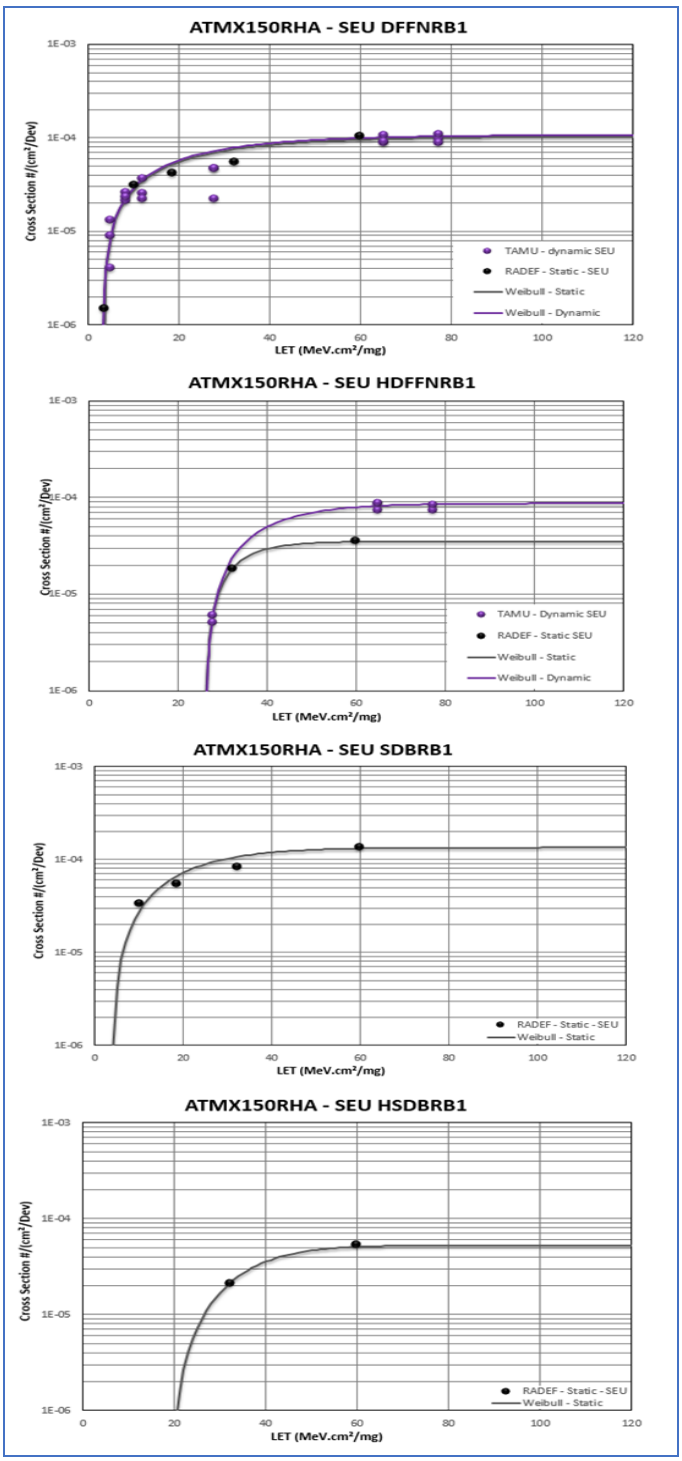
Figure 8: SBU Cross section (cm2/dev) = f(LET) - 6k39mux16 DPRAM with ECC – 02FU – 3 parts used

With ECC, the SEU cross section is reduced of:

- 2 decades for SRAM 12k39
  (from 2.85E-2 to 2.7E-4 cm^2/device).
- 3 decades for DPRAM 6k39
  (from 1.95E-2 to 1.2E-5 cm^2/device).

3) D Flip-Flops

The following graphs present the test results for four different standard D Flip-Flops compared to their corresponding hardened version. The cross sections per device (chain of 1024 DFF) are depicted on figure 9.



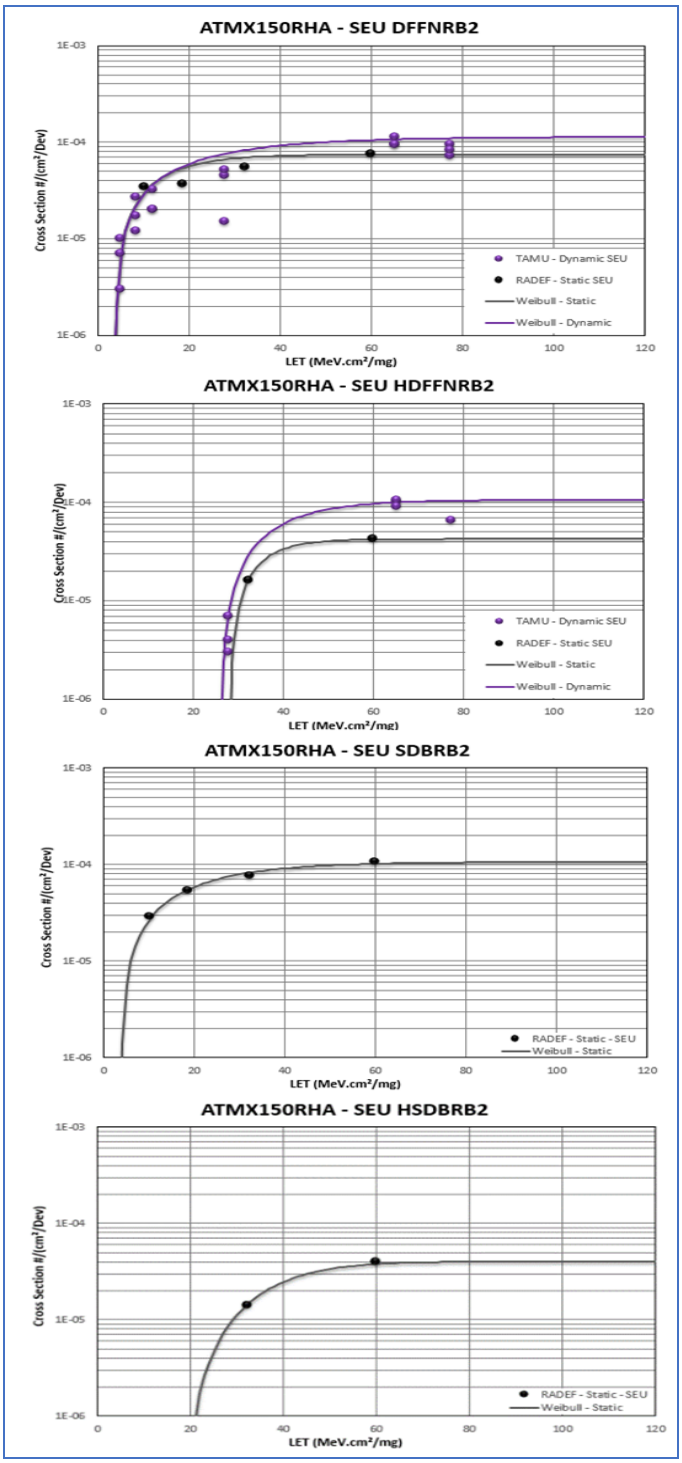


Figure 9: SEU cross sections of shift registers in cm²/device - a device is a chain of 1024 DFF

Only shift registers without hardening show events from 3MeV.mg/cm2 with a cross section up to 1.34E-4 cm² @ 60MeV.cm2/mg.

With the hardened DFF, the LET threshold is upper than 18.5MeV.cm²/mg, and the saturated cross-section is lower than 1.06E-4 cm^2.

4) SEU analysis for Memories and DFF

(a)LET threshold and cross section

The tables 2 & 3 summarize the LET threshold, cross section and W and S Weibull parameters derived from the SEE test results obtained for the various tested elements.

Memory type	LET threshold (MeV.cm²/mg)	SEU Xs (cm²/dev)	Weibull param.	
			W	S
SRAM16k32	1	$3.61E^{-2}$	24	1.2
SRAM12k39	1	$2.85E^{-2}$	24	1.2
DPRAM6k39	1	$1.95E^{-2}$	22	1.0
DPRAM2k8	1	$1.15E^{-3}$	25	0.9
TPRAM 1k16	1	$5.55E^{-4}$	30	0.8
SRAM12k39 with ECC	1	$2.56E^{-4}$	30	1.3
DPRAM6k39 with ECC	3.3	$1.30E^{-5}$	28	1.2
Memory type	**LET threshold (MeV.cm²/mg)**	**MBU Xs (cm²/dev)**	**Weibull param.**	
			W	**S**
SRAM16k32	2	$1.74E^{-3}$	40	1.8
SRAM12k39	2	$2.84E^{-3}$	40	1.8
DPRAM6k39	2	$2.43E^{-3}$	34	1.4

Table 2:Summary of the SBU/MBU LET threshold and cross section for the memories

DFF type	LET threshold (MeV.cm²/mg)	SEU Xs (cm²/dev)	Weibull param.	
			W	S
DFFNRB1	3.0	$1.08E^{-4}$	22	1.0
DFFNRB2	3.6	$1.14E^{-4}$	22	1.0
SEU hard. DFFNRB1	26	$8.70E^{-5}$	16	1.2
SEU hard. DFFNRB2	26	$1.06E^{-4}$	16	1.2
Scan Std DFF SDBRB1	3.6	$1.34E^{-4}$	20	1.3
Scan Std DFF SDBRB2	3.6	$1.06E^{-4}$	20	1.1
Scan SEU hard. DFF SDBRB1	18.5	$5.25E^{-5}$	20	1.7
Scan SEU hard. DFF SDBRB2	18.5	$4.00E^{-5}$	22	1.7
TMR - std DFFs	NA	0	NA	NA
PLL(*)	1	NA	NA	NA

Table 3:Summary of the LET threshold and cross section for the DFF – a device is a chain of 1024

(b)Soft Error Rate estimation

SEU error rate calculation has been made using OMERE 4.2 for some examples of orbits and conditions. The calculated error rates are presented in tables 4 to 13.

Environment conditions:
Estimation of error rate in space (SER protons estimated by PROFIT) using OMERE.
Solar Min, Z=1 to 92, Aluminium shielding of 1g/cm2.

The Weibull parameters (table 2 & 3) allow to simulate other space conditions and evaluate the probability of errors for a dedicated space mission.

Orbit	SRAM16k32	SRAM12k39
	SER/dev/day	SER/dev/day
GEO (35870Km)	$4.59E^{-01}$	$3.47E^{-01}$
ISS LEO (51°, 400Km)	$2.38E^{-02}$	$1.79E^{-02}$
LEO POL (98°, 800Km)	$1.91E^{-01}$	$1.46E^{-01}$
MEO (63°, 1000Km, 26768Km)	$4.42E^{-01}$	$3.36E^{-01}$

Table 4:Estimation of SBU error rate for SRAM.

Orbit	DPRAM6k39	DPRAM2k8
	SER/dev/day	SER/dev/day
GEO (35870Km)	$4.22E^{-01}$	$2.64E^{-02}$
ISS LEO (51°, 400Km)	$2.25E^{-02}$	$1.42E^{-03}$
LEO POL (98°, 800Km)	$1.60E^{-01}$	$9.79E^{-03}$
MEO (63°, 1000Km, 26768Km)	$3.99E^{-01}$	$2.49E^{-02}$

Table 5:Estimation of SBU error for DPRAM.

Orbit	TPRAM1k16
	SER/dev/day
GEO (35870Km)	$1.11E^{-02}$
ISS LEO (51°, 400Km)	$5.63E^{-04}$
LEO POL (98°, 800Km)	$4.21E^{-03}$
MEO (63°, 1000Km, 26768Km)	$1.05E^{-02}$

Table 6:Estimation of SBU error rate for TPRAM.

Orbit	DPRAM6k39 With ECC	SRAM12k39 With ECC
	SER/dev/day	SER/dev/day
GEO (35870Km)	$2.27E^{-05}$	$6.99E^{-04}$
ISS LEO (51°, 400Km)	$1.91E^{-06}$	$4.66E^{-05}$
LEO POL (98°, 800Km)	$2.14E^{-05}$	$5.36E^{-04}$
MEO (63°, 1000Km, 26768Km)	$2.75E^{-05}$	$7.95E^{-04}$

Table 7:Estimation of SBU error rate for DPRAM/SRAM with ECC.

Orbit	MBU SRAM16k32	MBU SRAM12k39
	SER/dev/day	SER/dev/day
GEO (35870km)	$1.16E^{-03}$	$2.06E^{-03}$
ISS LEO (51°, 400km)	$9.31E^{-05}$	$1.56E^{-04}$
LEO POL (98°, 800km)	$1.03E^{-03}$	$1.72E^{-03}$
MEO (63°, 1000km, 26768km)	$1.37E^{-03}$	$2.39E^{-03}$

Table 8:Estimation of MBU error rate per device for SRAM.

Orbit	MBU - DPRAM6k39
	SER/dev/day
GEO (35870km)	$5.10E^{-03}$
ISS LEO (51°, 400km)	$3.16E^{-04}$
LEO POL (98°, 800km)	$3.53E^{-03}$
MEO (63°, 1000km, 26768km)	$5.59E^{-03}$

Table 9:Estimation of MBU error rate per device for DPRAM.

Orbit	DFF DFFNRB1	DFF DFNRB2
	SER/FF/day	SER/FF/day
GEO (35870Km)	$7.81E^{-07}$	$6.82E^{-07}$
ISS LEO (51°, 400Km)	$3.68E^{-08}$	$3.38E^{-08}$
LEO POL (98°, 800Km)	$4.00E^{-07}$	$3.71E^{-07}$
MEO (63°, 1000Km, 26768Km)	$7.95E^{-07}$	$7.02E^{-07}$

Table 10: Estimation of SEU error rate per FF for Standard DFF (drives 1, 2).

Orbit	DFF SDBRB1	DFF SDBRB2
	SER/FF/day	SER/FF/day
GEO (35870Km)	$6.40E^{-07}$	$6.12E^{-07}$
ISS LEO (51°, 400Km)	$3.31E^{-08}$	$3.11E^{-08}$
LEO POL (98°, 800Km)	$3.58E^{-07}$	$3.40E^{-07}$
MEO (63°, 1000Km, 26768Km)	$6.63E^{-07}$	$6.33E^{-07}$

Table 11: Estimation of SEU error rate per FF for Standard Scan DFF (drives 1, 2).

Orbit	DFF H-DFFNRB1	DFF H-DFNRB2
	SER/FF/day	SER/FF/day
GEO (35870Km)	$3.75E^{-09}$	$5.63E^{-09}$
ISS LEO (51°, 400Km)	$1.14E^{-10}$	$1.72E^{-10}$
LEO POL (98°, 800Km)	$9.56E^{-10}$	$1.44E^{-09}$
MEO (63°, 1000Km, 26768Km)	$3.34E^{-09}$	$5.00E^{-09}$

Table 12: Estimation of SEU error rate per FF for Hardened DFF (drives 1, 2).

Orbit	DFF H-SDBRB1	DFF H-SDBRB2
	SER/FF/day	SER/FF/day
GEO (35870km)	$2.50E^{-09}$	$1.18E^{-09}$
ISS LEO (51°, 400km)	$7.63E^{-11}$	$3.56E^{-11}$
LEO POL (98°, 800km)	$6.38E^{-10}$	$3.00E^{-10}$
MEO (63°, 1000km, 26768km)	$2.23E^{-09}$	$1.04E^{-09}$

Table 13: Estimation of SEU error rate per FF for Hardened Scan DFF (drives 1, 2).

5) Assessment of SET/SEU by simulations

The high Single Event Transient (SET) soft error rate of integrated technologies becomes a major concern. It is the reason why the SET pulse width measurements or calculations are necessary to determinate the SET circuit sensitivity and optimize the radiation hardening. Thus, the measurement and modelling of the widths of transient voltage pulses are critical for the prediction and mitigation of soft errors.

(a)RAPTOR tool

The RAdiation Prediction TOols on Rhbd (RAPTOR) is a platform able to model the SET pulse width and assess the sensitivity of circuits to SET/SEU by considering the topology of the layout, the power supply, the logical states, the logic masking, the narrowing and/or broadening of the SET pulse widths.

This platform is a suite of tools including the software MUSCA developed and supported by the ONERA, and a list of MICROCHIP® proprietary tools developed in the framework of this project. The challenge was to integrate MUSCA® into a MICROCHIP® design flow and propose a user-friendly platform usable by all the designers.

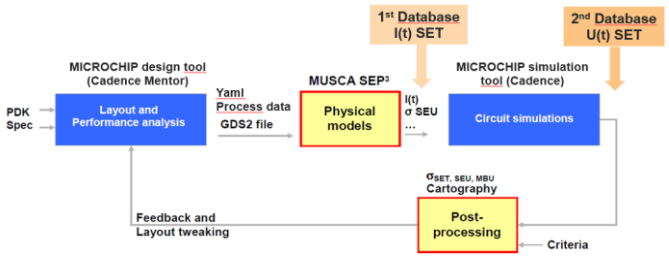


Figure 10: Integration of RAPTOR tool in the design flow

The tool has been successfully validated on standard cells (combinatory cells and sequential), and complex circuits such as clock trees. The platform is now integrated in the design flow, and each new digital IP or standard Cells is assessed to SET/SEU by using RAPTOR.

The heavy ion SEU cross sections are extracted from dynamic and static ground tests. The figure 11 presents respectively the experimental SEU cross sections versus LET and the RAPTOR results obtained for the four logic states of the DFF cell.

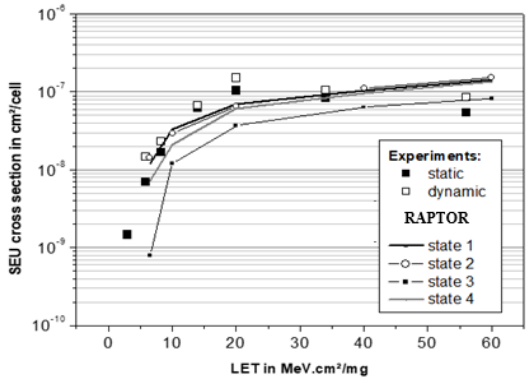


Figure 11: Heavy Ion SEU Cross section versus LET (Static/dynamic exp. and RAPTOR calculations, Delay Flip-Flop cell

The predicted SEU cross sections are relatively close to the measurements from all LET values beyond 3 MeV.cm²/mg (threshold and saturation value). Moreover, the impact of the logical state of the cell is significant for the threshold and the saturation. Results indicate that the logical state 3 is less sensitive than the other states

The results are processed and reformatted to facilitate their analysis and to quickly determine the effectiveness of the hardening. RAPTOR generates three types of output files:

- The SET/SEU cross section which defines the sensitive area of the circuit Vs LET
- The SET pulse widths distribution (the number of SETs as a function of the SET duration

- The mapping of the SET/SEU sensitivity on the layout of the circuit

The adding value of RAPTOR is its ability to assess easily, and in a short time the radiation sensitivity of a circuit, IP or standard cell. The effort deployed on the user-friendly interface is a plus for the analysis. Thus, RAPTOR is a key tool to improve the customer support on the radiation hardening.

V. SEGR&SEB OF LDMOS

The ATMX150RHA high voltage laterally diffused LDMOS have been evaluated versus the SEGR and SEB through several SEE sessions. The SEE tests have been performed on 2 types of LDMOS devices, i.e., 25V & 45V. These high voltages supplies are supported by their drains, because of their diffused configuration, while the gate, identical to those of 3.3V devices is limited to 3.6V. As an example, LDNMOS device is shown on figures 12 and 13.

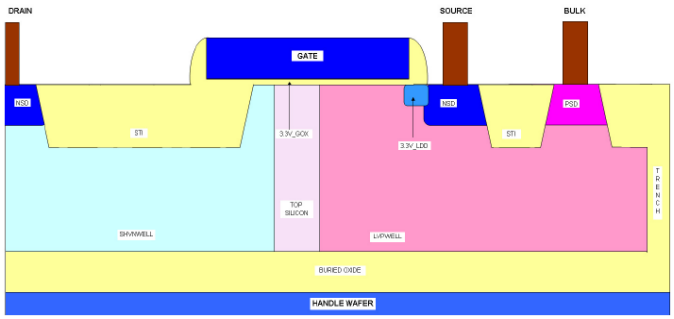


Figure 12:LDNMOS Schematic cross section

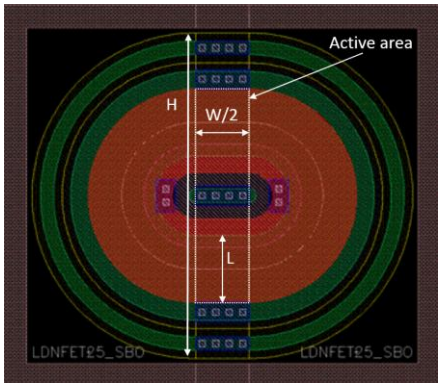


Figure 13:LDNMOS layout view

Post Rad Safe Operating Area (SOA) have been introduced on LDNMOS devices after SEGR to limit the domain of use versus V_{ds} and LET thus avoiding the destruction on Heavy Ion.

No limitation has been observed on LDPMOS 25 & 45V.

The only limitation of the use of this device depends of drain/ source supply (Vds) for the whole gate/source supply (Vgs) of the technology.

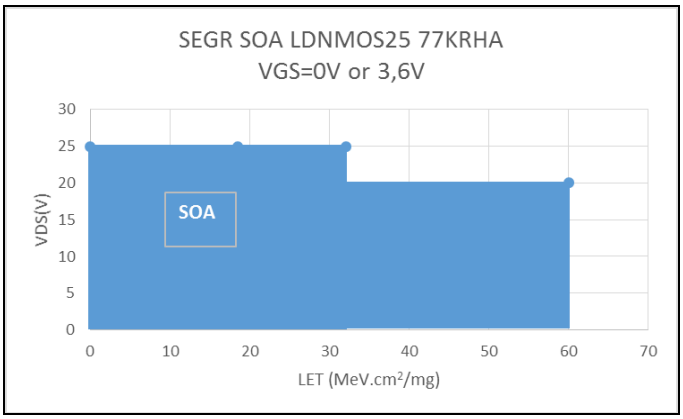


Figure 14:SEE Safe Operating Area of LDNMOS25

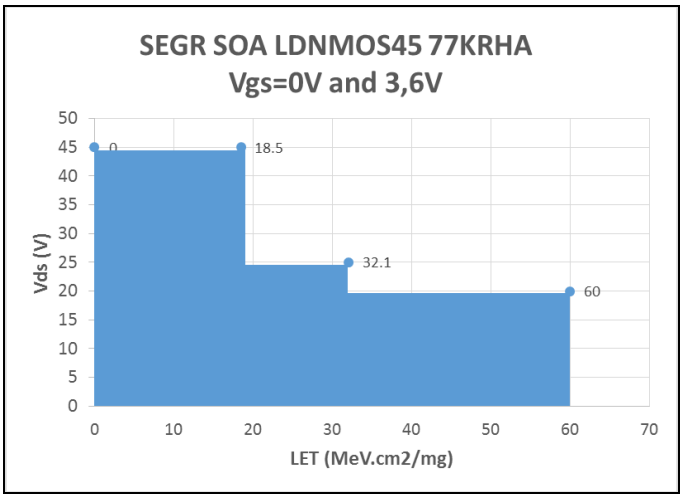


Figure 15:SEE Safe Operating Area of LDNMOS45

The SEB characterization have demonstrated the robustness of the LDMOS 25V and 45V versus Heavy Ions. No SEB encountered up to 60 MeV.cm2/mg at different Vds/Vgs worst case conditions.

VI. TOTAL IONIZING DOSE

A Total Ionizing Dose test has been performed on this test vehicle in accordance with 1019.5 MIL STD 883 test method. The test is performed using a Co_{60} source on 22 parts from 2 different diffusion lots; 11 parts and one additional control part per lot (Lot number D7NOG.1-1 and D7N0F.1-4A). During the irradiation, the parts are supplied in static conditions at fixed maximum bias: 1.95V for the core and 3.6V for I/Os. The irradiation is performed at room temperature with a dose rate of 300rad/h. For this irradiation session on test vehicle, a total dose of 300krad(Si) has been tested. Electrical tests are performed before irradiation and after 50, 100, 150, 200, 250 and 300 krad(Si) of cumulated dose. Then, an annealing of 24 hours at room temperature followed by an annealing under bias during 168h at 100°C are performed and characterized by a final electrical test.

All parts pass the whole electrical functional and parametric tests up to 300krad(Si).

At 300krad(Si), the dynamic parameters are unchanged and no leakage current is measured. I/O buffers and Core Standby current show a good immunity at the total dose. Only the standby supply currents exhibit a slight drift on one Si-lot but they largely remain in the specification (fig.16).

After the annealing 168h@100°C, all the parts are still functional and the standby supply currents do not exhibit parametric drifts any more. No rebound effect is observed.

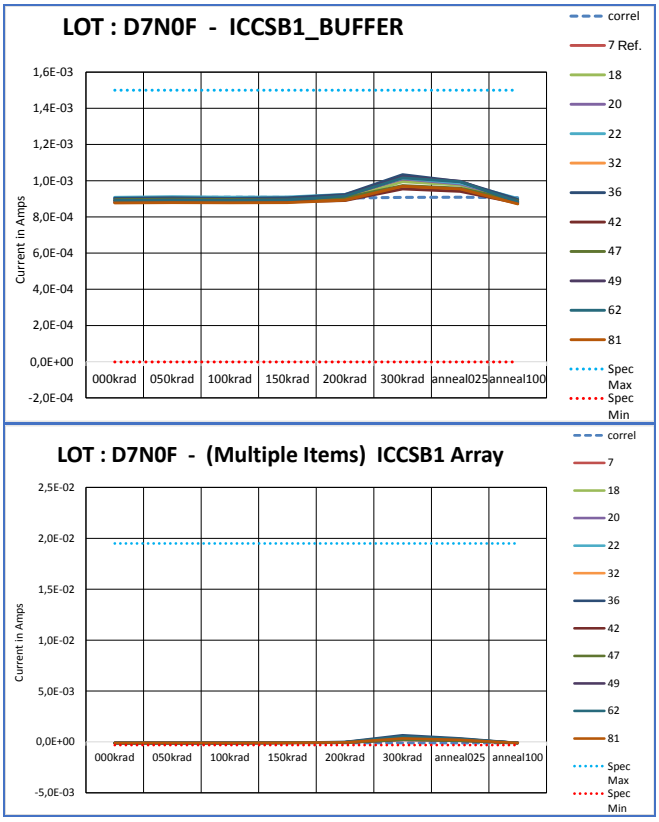


Figure 16:evolution of standby supply currents during irradiation, for the buffer(above) and core&memories(below)

No drift on input leakages IIH, and IIL and no drift on VOL, VOH is measured during irradiation and after annealing on the 3.3V I/Os, as shown on the figure 17.

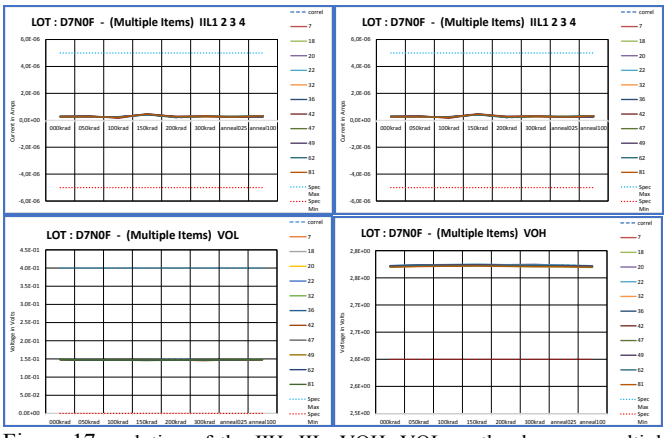


Figure 17:evolution of the IIH, IIL, VOH, VOL vs the dose, on multiple 3.3V I/O.

Finally, no evolution vs the dose has been encountered on Coldsparing leakage current (fig 18).

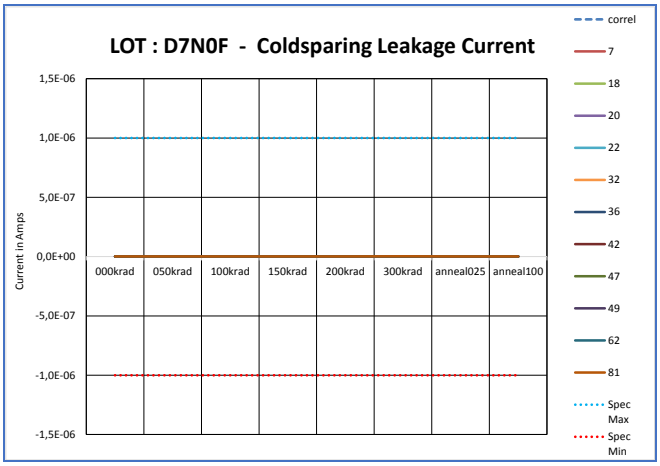


Figure 18: evolution of the Colsparing leakage current versus the dose.

The ATMX150RHA test vehicle has been tested successfully up to a total dose of 300 krad(Si). This test shows the very good immunity of the ATMX150RHA ASIC family against total dose and demonstrates the capability of this technology to maintain the QML-RHA level of R (100krad(Si)).

The ATMX150RHA technology is RHA level R for low voltage devices.

Complementary dose tests have been performed for the evaluation at elementary device level of the 1.8V and 3.3V MOS and of the HV devices as 5V MOS and LDMOS. They are presented in this paper.

A. 1.8V MOS devices

1) Linear LV Nmos devices

(a)Threshold Voltage

Because of their thin gate oxide the V_{th} shift of the LV Nmos is inferior to 10mV after 300krad(Si) whatever the dimensions (table 14).

		Width/Length (W/L)			
Level (krad(Si))	ΔVt (mV)	10/0.18	10/10	0.24/10	0.24/2
100	Avg.	0.2	1.0	-4.8	-3.2
	Max	0.6	1.6	-6.2	-4.3
300	Avg.	-0.5	-0.8	-7.4	-3.6
	Max	-0.9	-1.0	-10.1	-8.6

Table 14:ΔVt for NMOS 1.8V after 100 and after 300krad(Si)

A very low width dependence can be noticed with total dose: the Vt drift increases when the width decreases.

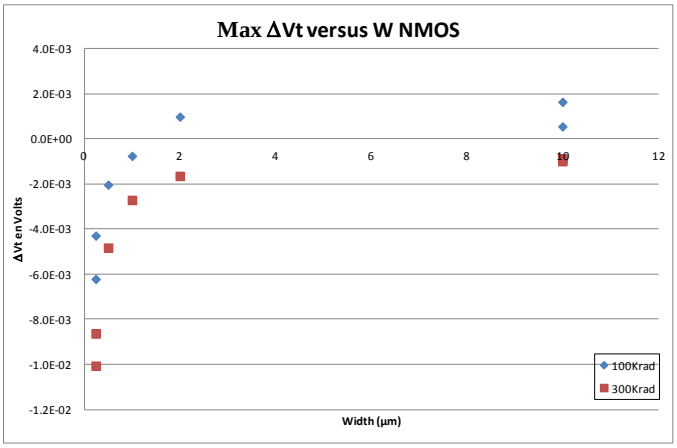


Figure 19: Max Vt drift vs. NMOS width after 100 and 300 krads(Si).

The Vth drift on Nmos remains negligible (fig. 20).

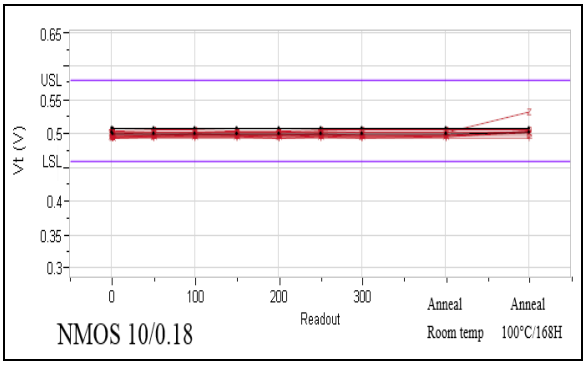


Figure 20: Threshold voltage drift versus Total dose on NMOS 1.8V

(b) Subthreshold leakage current (Ioff)

No drift appears on NMOS short device in term of leakage current. Only a very slight increase can be observed on long devices but this drift is inferior to ½ decade at 300 krad(Si). This drift is totally recovered after annealing.

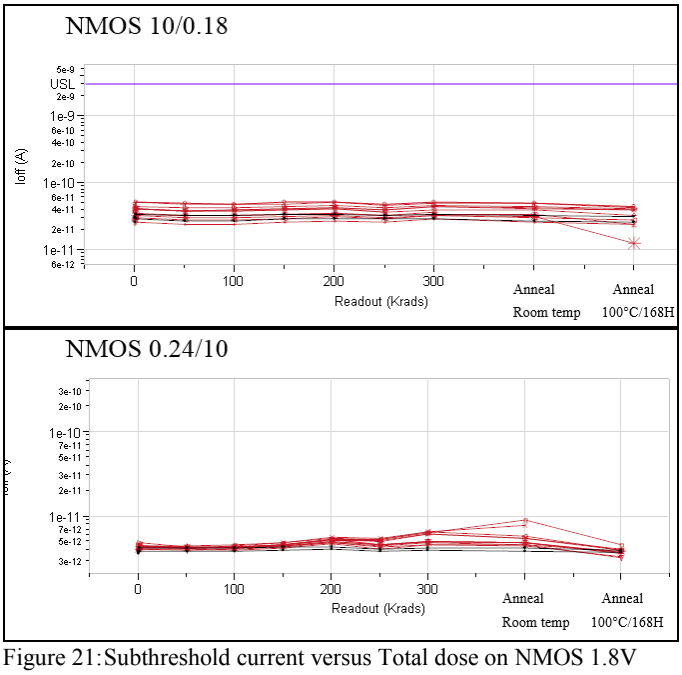


Figure 21: Subthreshold current versus Total dose on NMOS 1.8V

(c) Input/Output characteristics of NMOS 1.8V

The effect of the radiation is also studied on elementary devices through the electrical characteristics compared before and after irradiation (300krad(Si)). For each 1.8V N/P MOS devices studied on total dose, the output and input I(V) curves are measured.

For all graphs:

- Blue curves before irradiation, red curves after 100 krad(Si), Green curves after 300 krad(Si)
- Id(Vg) for Vd = 0.1V (-0.1V for PMOS)
- Id(Vd) for Vg=Vcc typ (-Vcc typ for PMOS)

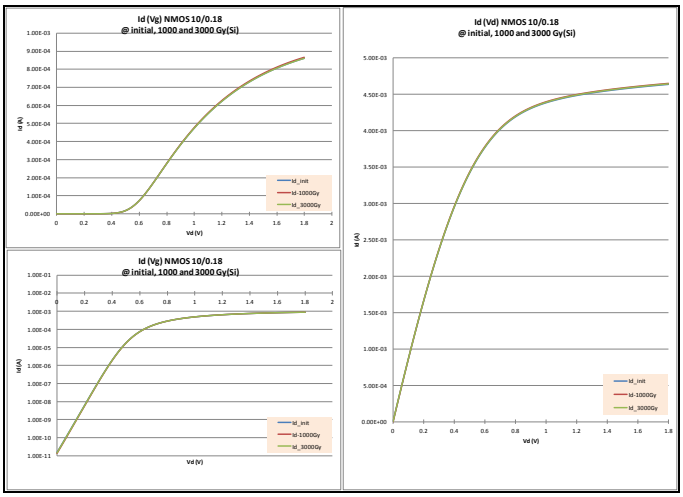


Figure 22: In and Output characteristics for NMOS 1.8V 10/0.18.

The input and output characteristics on large and short devices do not show any major difference before and after irradiation. The threshold voltages and the slopes are not affected by the radiation up to 300 krad(Si), neither saturation current. NMOS 1.8V devices show a very good immunity versus the dose.

A difference exists only for narrow / long devices with a rise of the saturation current versus the dose but still inferior to 5%.

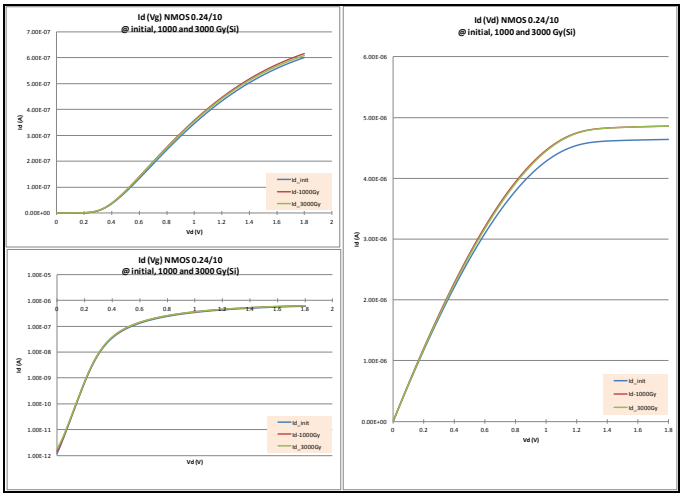


Figure 23: In and Output characteristics for NMOS 1.8V 0.24/10

2) Linear LV Pmos devices

Considering the TID mechanism, PMOS devices are better immune with dose than NMOS. Their absolute threshold voltages increase with dose, then no leakage current appears and the other parameters remain stable.

(a) Threshold Voltage

On PMOS 1.8V devices, the shift of threshold Voltage after a total dose of 300 krad(Si) irradiation is negligible. See on the table 3 below, the ΔVt at 100, 300 krad(Si).

		Wdth/Length (W/L)		
Level (krad(Si))	**ΔVt (mV)**	**PMOS 10/0.18**	**PMOS 10/10**	**PMOS 0.24/10**
100	Average	-7	-6	-12
	Max	-9	-7	-15
300	Average	-7	-7	-15
	Max	-8	-8	-20

Table 15:ΔVt for PMOS 1.8V transistors after 100, 300 krad(Si).

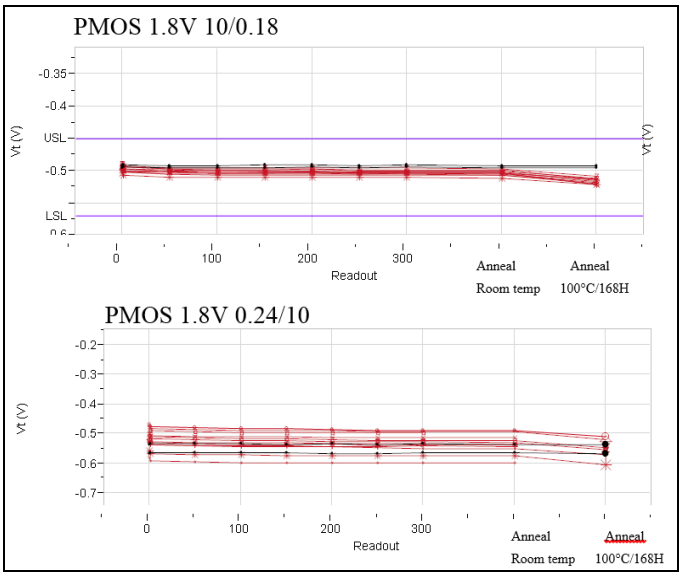


Figure 24:PMOS 1.8V threshold voltage vs. Total dose

(b)Subthreshold leakage current (Ioff)

On PMOS 1.8V, the leakage currents remain constant up to 300 krad(Si) and totally recover after annealing.

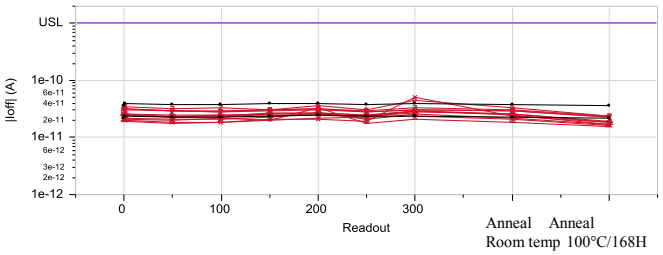


Figure 25:PMOS 1.8V 10/0.18 Subthreshold leakage current vs. Total dose.

(c)Input characteristic for PMOS 1.8V

The irradiation does not affect the characteristics of PMOS whatever the dimensions.

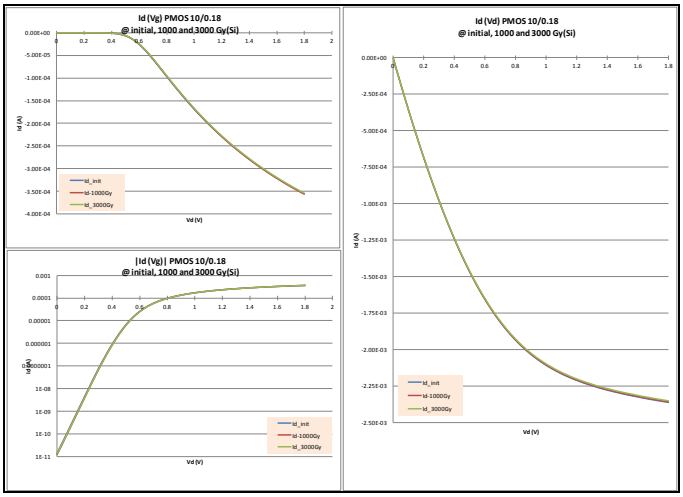


Figure 26:In and Output characteristics for PMOS 1.8V 10/0.18

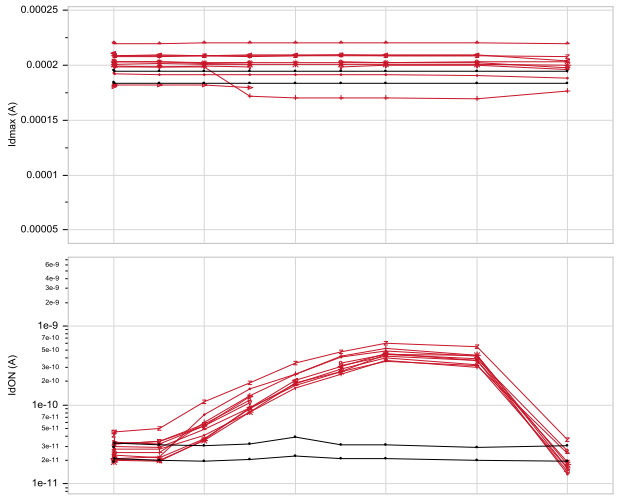
3) Inverter 1.8V

3 parameters have been analysed:

- ID MAX current: Max current measured during the switch of the inverters from IN=0 to IN=1; characterize the current peak passing through the inverter.
- ID ON: leakage current when IN=1; characterize the leakage current in the PMOS device and between N+ and P+ Drain/Source of the inverter (parasitic transistor).
- ID OFF: leakage current when IN=0, Characterize the leakage current in the NMOS device and between N+ and P+ Drain/Source of the inverter (parasitic transistor).

As already shown, the leakage current of the devices N and P MOS 1.8V is low and does not rise with total dose. Only the parasitic devices bring a drift of the leakage currents. On the Inverter 1.8V, we can verify this point: both parameters ID_ON and ID_OFF have the same behaviour with 2 decades growing with the cumulated dose (Fig. 27).

The switch current (called ID_max) remains stable after irradiation and anneals.



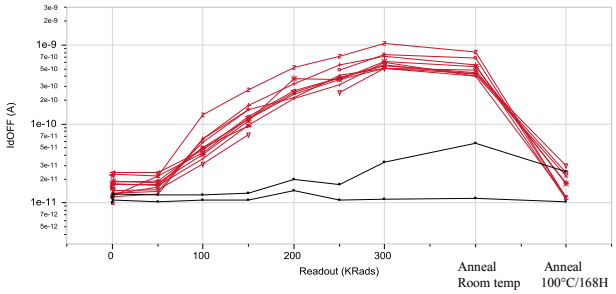


Figure 27:Inverter 1.8V currents vs. Total dose

4) Ring oscillator 1.8V

The frequency of a ring oscillator 1.8V has been analysed for different conditions of bias (see figures 28):

- 6 Parts with IN=0 (Green)
- 6 Parts with IN=1 (Green)
- 3 ref parts with IN=0 (not irradiated – Red)
- 3 ref parts with IN=1 (not irradiated- Red))
- 2 ref parts not biased and not irradiated (Black)

Results do not show any effects of total dose on the frequency up to 300krad(Si) neither after annealing.

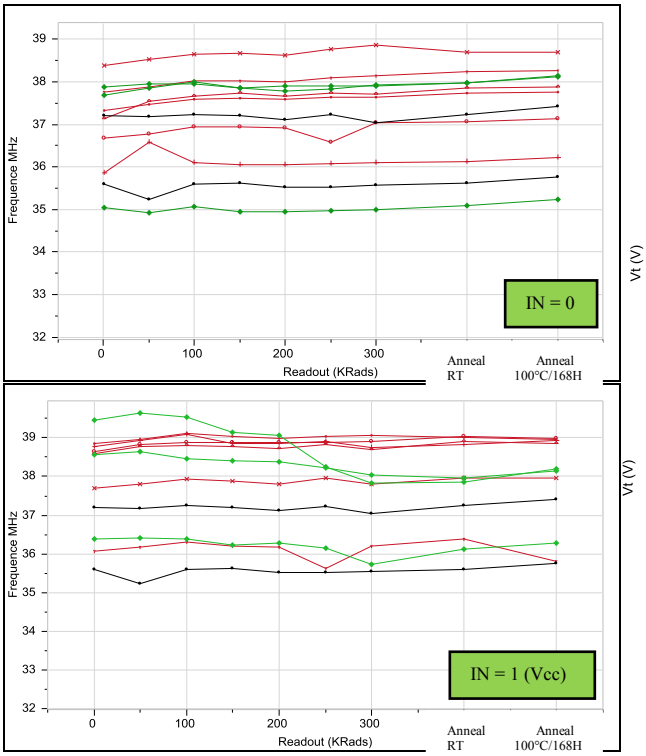


Figure 28:Ring Oscillator 1.8V Frequency vs. Total dose

B. 3.3V MOS devices

1) ELT 3.3V NMOS devices

The 3.3V NMOS device available in the ATMX150RHA PDK is a ring device (so called ELT). In this chapter, it is compared to the linear one not allowed for Aerospace applications.

(a)Threshold Voltage

NMOS 3.3V ELT and linear devices show a very slight positive shift of threshold Voltage under total dose after 300krad(Si) with a slow rebound effect (see table16 and figure29).

Level Krad(Si)	ΔVt (mV)	Width/Length (W/L) NMOS ELT 10/0.36	NMOS ELT 0.88/10	NMOS Linear 0.88/10
100	Average	+5	+5	+4
	Max	+7	+10	+8
300	Average	+11	+15	+12
	Max	+15	+20	+18

Table 16:ΔVt for NMOS 3.3V transistors after 100, 300 krad(Si) irradiation and after Anneal 100°C

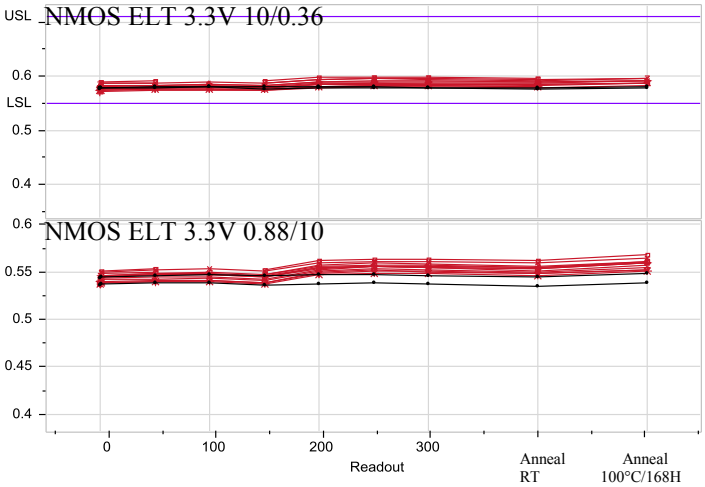
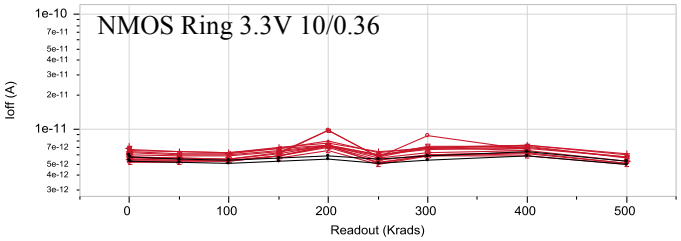


Figure 29:NMOS 3.3V threshold voltage vs. Total dose

(b)Subthreshold leakage current (Ioff)

A slight leakage increase is observed on linear devices (inferior to ½ decade after 300 krad(Si)). This leakage current is fully cancelled with ring layout.



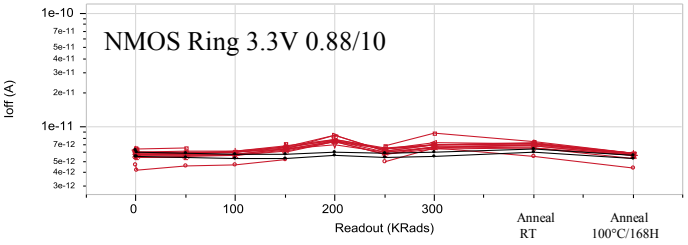


Figure 30: NMOS 3.3V ELT Subthreshold current vs. Total dose

(c)Input/Output characteristics of NMOS 3.3V

For each 3.3V NMOS devices studied versus the total dose, the output and input I(V) curves are measured.

For all graphs:

- Blue for the curves before irradiation, red for the curves at 100 krad(Si), Green for the curves at 300 krad(Si)
- Id(Vg) for Vd = 0.1V (-0.1V for PMOS)
- Id(Vd) for Vg=Vcc typ (-Vcc typ for PMOS)

The behaviour of NMOS 3.3V with ring layout is very similar between initial and after 100 and 300 krad(Si) irradiation.

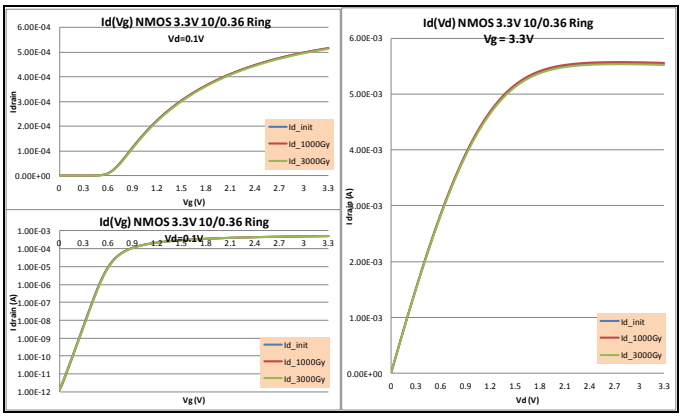


Figure 31: Input and Output characteristics for NMOS 3.3V 10/0.36 Ring

The NMOS 3.3V ELT allows to avoid the subthreshold leakage current which appears usually with the cumulated dose. The Id(Vg) curve in log scale (figure 32) highlight the improvement brought by ELT layout compared to linear one.

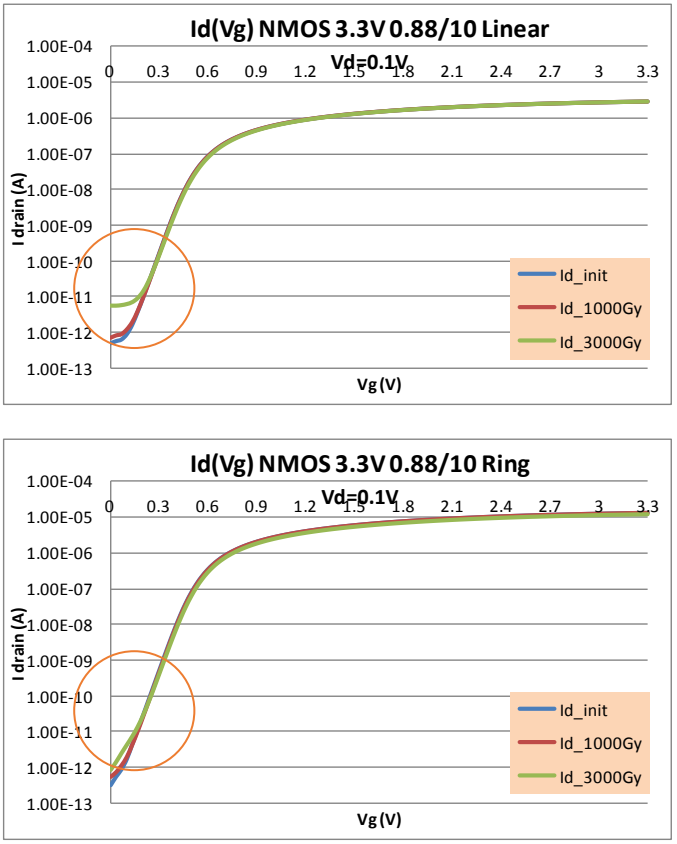


Figure 32: ELT effect on subthreshold leakage current on NMOS 3.3V (top: linear devices, bottom: ELT devices)

2) PMOS 3.3V devices

For each 3.3V PMOS devices studied versus the total dose, the output and input I(V) curves are measured.

(a)Input/Output characteristics of PMOS 3.3V

In the same way as PMOS 1.8V, the electrical characteristics of PMOS 3.3V devices do not show any difference after irradiation.

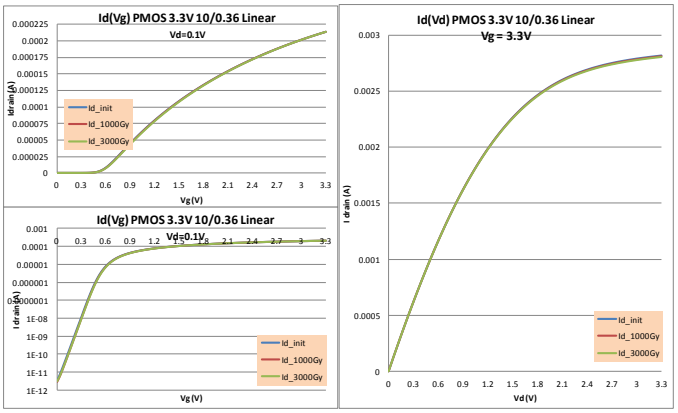


Figure 33: In and Output characteristics for PMOS 3.3V 10/0.36

C. 5V MOS devices

1) 5V NMOS devices

(a) Threshold Voltage

As expected by theory and because the 5V devices are processed with a 250Å-oxide (commonly used for 15V devices), this device is influenced by the cumulated dose. This drift on Vth depends mainly of:

- the oxide thickness
- the electrical field in the oxide during irradiation

It is commonly expected to have more than 400 mV / 100krad(Si) of drift on Vt Nmos with a maximum electrical field (Vcc max = 15V) on this oxide thickness. For the Nmos 5V using the 250Å oxide this drift is reduced due to the voltage limitation of Vcc max = 5.5V.

According to the theory and the experiments this drift is inferior to 40mV/100 krad(Si) for the short device and close to 110mV/100 krad(Si) for the narrowest one.
The ELT does not enable to reduce this Vth drift (fig. 34). This result shows that this effect is a mainly active area effect; not due to the parasitic devices along the trench edge.

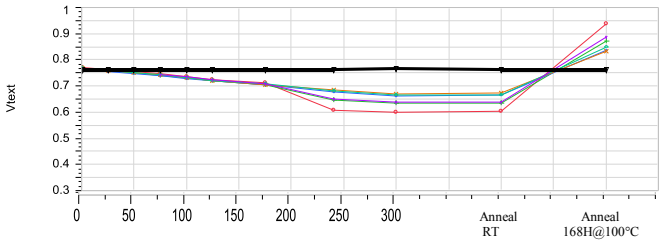


Figure 34: Nmos 5V – ELT 20/1: Vt drift (V) vs Dose (krad(Si))

(b) Subthreshold leakage current

In contrast with what we explained about the Vth, the ring layout reduced drastically the leakage current effect brought by the parasitic transistor (fig. 35).

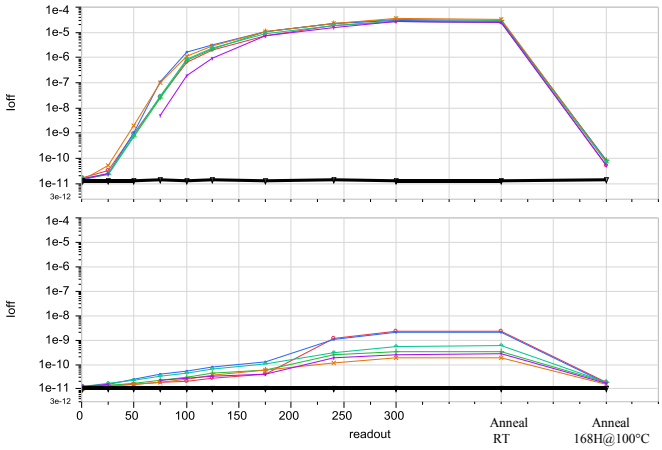


Figure 35: Nmos 5V – 20/1 short device: Subthreshold leakage (A) current vs Dose (krad(Si)) - top: linear, bottom: ELT

Ring layout has a major effect on leakage current with a large reduction observed of 4 decades with ring layout at 100 and 300 krads(Si).
The leakage current fully recovers after annealing but rebound effect is noticed on threshold Voltage (Vth) on both layout.

The ELT remains mandatory to reduce drastically leakage current.

(c) Saturation current

Lastly saturation current remains constant with the dose a very slight drift can be observed (Fig. 36) but still under specification limit.

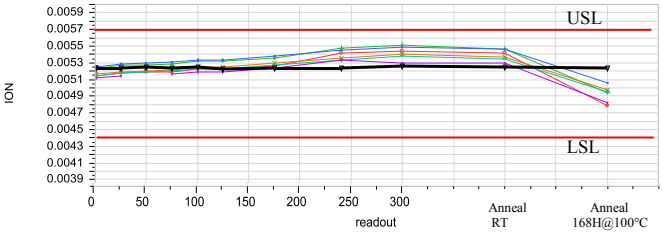


Figure 36: Nmos 5V – 20/1 ELT: Saturation current (A) vs Dose (krad(Si))

The same behavior is observed whatever the dimensions.

ELT Nmos 5V devices are the option to reach the compliance of 50 krads(Si):

- The drift on Vth remains under specification limit after 75 krad(Si)).
- The drift on subthreshold leakage current is less than one decade at 75 krads (Si).

2) 5V PMOS devices

The 5V Pmos keep a good behaviour with the cumulated dose and the ring layout does not bring any improvement:
On linear devices, no drift appears on transconductance (Gm) and subthreshold leakage current (Ioff). Only threshold voltage (Vt) and Saturation current (Ion) show a slight drift (inferior to 10% after 300krads(Si)) without recovery after annealing.

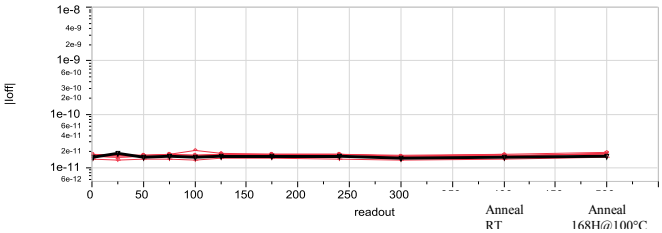


Figure 37: Pmos 5V – linear 20/20 Large device

The 5V devices under dose show an expected behaviour regarding to the 250Å-oxide use.
Linear Pmos devices keep a relatively good behaviour with the dose; no effect on transconductance nor subthreshold leakage current and reduced effect on threshold voltage and saturation current.

Nmos transistor is the most sensitive compared to the Pmos transistor. By consequence, “ELT” layout is implemented for 5V Nmos to limit the impact of the cumulated dose on the leakage current.

D.LDMOS devices

The ATMX150RHA high voltage laterally diffused LDMOS have been evaluated versus the cumulated dose through several TID sessions. The TID tests have been performed on 2 types of LDMOS devices, i.e., 25V & 45V. These high voltages supplies are supported by their drains, because of their diffused configuration, while the gate, identical to those of 3.3V devices is limited to 3.6V. As an example, LDNMOS device is shown on figures 10 and 11.

A first evaluation session shows the functionality conservation up to 300krad(Si) but a significant drift of Rds_{on} and I_{on} parameters, depending of supply conditions during the irradiation. The following sessions enabled the full characterization up to 90krad(Si) cumulated dose with the development of post rad spice models at 30krads(Si) at worst case conditions.

1) LDNMOS 25V

Several dimensions of LDNMOS 25V have been tested (4 different W with fixed L) at worst case supply condition during the irradiation i.e. 3.6V on the gate.
The following results are related to characterization after 30krads(Si) cumulated dose; results used for extraction of post rad spice models.

(a) Experimental data for Electrical Model @ 30krad(Si)

The figure 38 present the Id(Vg) and Id(Vd) characteristics of a LDNMOS25 W=400um after 30krads(Si), compared to the initial measurements.

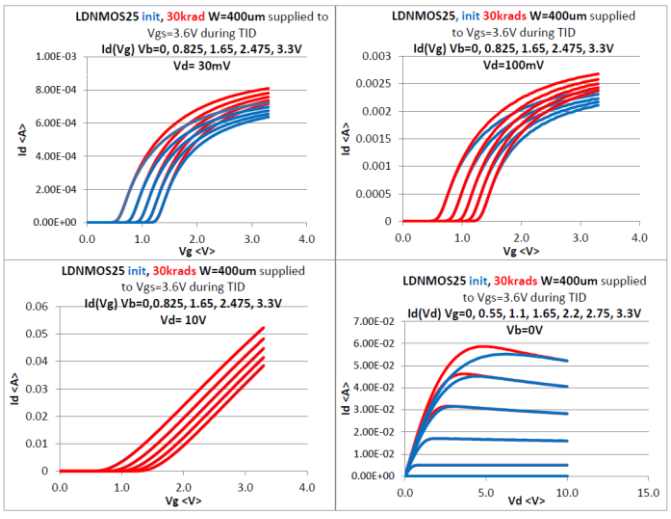


Figure 38:Id(Vgs) and Id(Vds) @ 30krad(Si) for LDNMOS25V - W=400µm

2) LDPMOS 25V

Several dimensions of LPNMOS 25V have been tested (4 different W with fixed L) at worst case supply condition during the irradiation i.e. -25V on the drain.
The following results are related to characterization after 30krads(Si) cumulated dose; results used for extraction of post rad spice models.

(a) Experimental data for Electrical Model @ 30krad(Si)

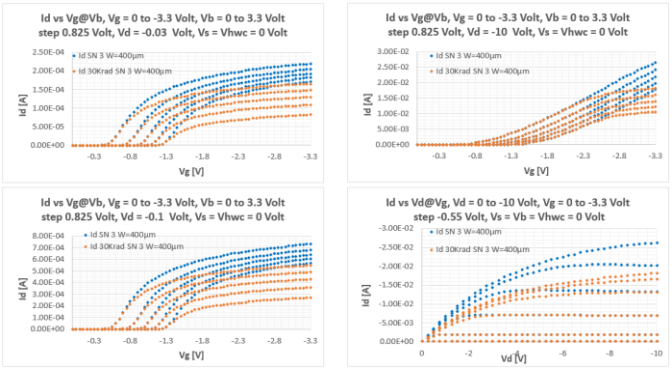


Figure 39:Id(Vgs) and Id(Vds) @ 30Krad(Si) for LDPMOS25V - W=400µm

3) LDNMOS 45V

Several dimensions of LDNMOS 45V have been tested (4 different W with fixed L) at worst case supply condition during the irradiation i.e. 3.6V on the gate.
The following results are related to characterization after 30krads(Si) cumulated dose; results used for extraction of post rad spice models.

(a)Experimental data for Electrical Model @ 30krad(Si)

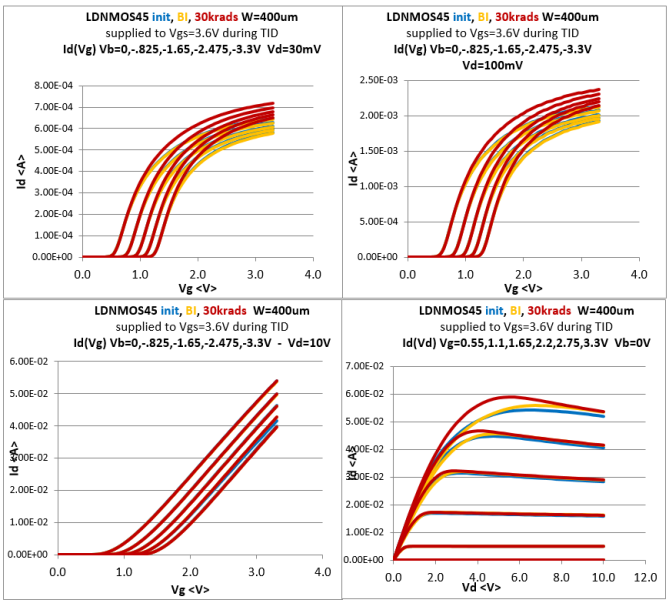


Figure 40:Id(Vgs) and Id(Vds) @ 30krad(Si) for LDNMOS45V - W=400µm

4) LDPMOS 45V

Several dimensions of LDPMOS 45V have been tested (4 different W with fixed L) at worst case supply condition during the irradiation i.e. -45V on the drain.
The following results are related to characterization after 30krads(Si) cumulated dose; results used for extraction of post rad spice models.

(a)Experimental data for Electrical Model @ 30krad(Si)

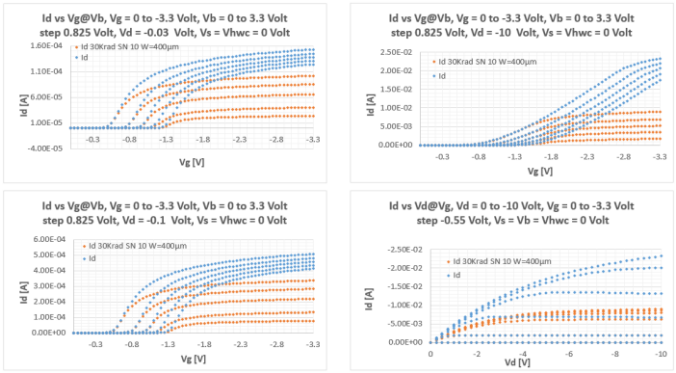


Figure 41:Id(Vgs) and Id(Vds) @ 30krad(Si) for LDNMOS45V - W=400µm

VII. CONCLUSION

The ATMX150RHA has been tested according to JESD57/ESCC25100 and to 1019.5 MIL STD 883 test method.

The digital ATMX150RHA test vehicle has been tested successfully up to a total dose of 300 krad(Si), without rebound effect.

Different evaluations at device level have been done showing the TID capability of the technology for the different domain of the devices.

The heavy ions SEE test results have demonstrated the large capability of the ATMX150RHA:

- the latch-up immunity of the ATMX150RHA ASIC family at maximum temperature (threshold LET higher than 78 MeV/mg/cm2).
- the efficiency of the SEU hardening techniques used for ATMX150RHA SEU hardened DFF (a LET threshold upper than 18.5 MeV/mg/cm2)
- the very good SEU hardening results obtained for the compiled memories when used with error correction code.
- the sensitivity of the standard DFF to SEU (LET threshold of 3.0 MeV/mg/cm2).
- No SEU event was observed in any run with TMR hardening.
- No SEB on LDMOS 25 and 45V
- No SEGR on LDPMOS 25 and 45V and SOA on LDNMOS

Based on these results the ATMX150RHA features meet the radiation performance required for space applications.

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Session C

Radiation Effects on analogue and mixed-signal ICs

Static Linearity Test for Radiation Effects Characterization of an 18-bit SAR Serial IO COTS ADC: Analog Devices AD7982

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Abstract

This paper reports the testing results of a Successive-Approximation-Register (SAR) ADC of 18-bits with Serial Input/Output digital interface. We compare the results of using a standard approach with a new test methodology for SAR static linearity testing. The available test time in between radiation steps is limited in order to avoid annealing. The presented method strongly reduces the amount of output code samples, which implies not only higher test speed but also lower test cost.

I. Introduction

The Differential Non-Linearity (DNL) and the Integral Non-Linearity (INL) are both some of the most important static parameters that must be known to insure the correct operation of an ADC in a certain application. The Histogram Method [1] is one of the standardized method to obtain the static performance of the ADC, achieving a very precise result independently of the type of its transfer function. But the high cost of its application, due to large number of samples that must be acquired (that increases, in general, in an exponential way with the converter resolution) and the requirement of a sufficiently linear input source, makes the Histogram Method expensive and time-consuming for the test of high-resolution ADCs, especially in the Space Industry area where today time and cost are key elements that demand for solutions that allow rapid and simple adaptation of commercial components to be used in space systems, the Commercial Off-The Shelf (COTS) components.

Many works have been proposed to solve the mentioned histogram test drawbacks. Some works are based on the use of spectral processing [2]-[6], where the number of samples to be taken, and the test time, is drastically reduced, but they require a high purity sinusoidal input. Other works [7]-[10] suggest methods for relaxing the input signal generator linearity, using two related nonlinear stimuli. In [7] the non-linearity inserted by the stimulus is identified and removed (SEIR) exciting the ADC with two identical non-linear ramps with a voltage offset between them. [8] includes modifications for a test environment where time drifts are not negligible. In [10] the authors introduce a simple and general algorithm based on SEIR but independent of the test signal waveform and adapted to a non-stationary test set-up.

This paper shows the non-linearity results obtained by the application of a modified test methodology based on [11] to the commercial 18-bit SAR AD7982 converter of Analog Devices [12]. It uses a segmented non-parametric integral non-linearity model that dramatically reduces test data and achieves better precision than the standard histogram test.

Section II presents the used algorithm. Section III describes de ADC DUT to be tested. Section IV depicts the measurement setup. Section V displays the experiments results and comparison with a standard method. Section VI provides the conclusions. Finally, section VII expresses the acknowledgements.

II. Test Methodologies

A. Sinewave Histogram Test

The sinusoidal Histogram Method [1] consists in stimulating the ADC with a pure sinusoidal signal that slightly saturate the output. The digital output codes are then accumulated in code bins forming a histogram, each bin corresponding with an output code. The accumulation in the code bins are then compared with the expected occurrences of an ideal ADC of the same resolution when excited with a sinusoidal. The difference indicates the non-linearities of the converter.

B. Improved Efficiency Algorithm

The improved algorithm [11] exploits three main factors: 1) the amount of truly independent error sources contributing to linearity errors is much lower than the number of code bins to be tested; 2) all sampled codes are valid to estimate the ADC parameters. Noise is rejected by the algorithm itself; 3) Integral Non-Linearity accept a mathematical segment model, i.e. INL curve is a collection more or less complex of rectilinear segments without continuity restrictions between them. This way, DNL is a discrete collection of positive and negative spikes corresponding to the discontinuity jumps between segments.

The methodology is especially appropriate for high resolution high linearity ADCs as SAR, Pipeline and Cyclic ADCs, which present such a kind of segmented non-linearity error. In actual high-resolution ADCs, segmentation pattern of INL can be practically described using a few (2 to 5) levels of

segmentation model. Algorithm [11] used here, only apply a three level model.

Consider the r-bit binary word of output code, Z, of our ADC under test is written as:

$$\begin{aligned} Z &\equiv \{b_{17}, b_{16}, ..., b_3, b_2, b_1, b_0\} \\ &\equiv \underbrace{\{b_{17}, b_{16}, ..., b_{11}, b_{10}\}}_{Z_M} \| \underbrace{\{b_9, b_8, ..., b_4, b_3\}}_{Z_I} \| \underbrace{\{b_2, b_1, b_0\}}_{Z_L} \end{aligned} \quad (1)$$

where a resolution of r=18 bits is used to exemplify the model, and the symbol '||' represents the bit-word concatenation operation.

Code Z is expressed in terms of three subcodes. A Most significant code, Z_M, an Intermediate significant code, Z_I, and a Least significative code, Z_L, with respectively resolution of r_M=8, r_I=7, r_L=3 bits $(r = r_M + r_I + r_L)$.

Segmentation model of INL assumes that the curve $INL(Z)$ has the following functional form:

$$INL(Z) = f_M(Z_M) + f_I(Z_I) + f_L(Z_L), \quad Z \in [1, 2^r - 1] \quad (2)$$

i.e. the INL is the sum of three functions which depend each one on one subcode of partition in (1).

This model implies that:

- $f_M(.)$ is a discrete function of $(2^{r_M} - 1)$ values, corresponding to all different values of Z_M excepting 0 (INL(0) is undefined);
- $f_I(.)$ is a discrete function of $(2^{r_I} - 1)$ values, and
- $f_L(.)$ is a discrete function of $(2^{r_L} - 1)$ values.

Therefore, in the case of (1), INL results in a discrete function of $(2^r - 1) = 262143$ values but determined only by 255+127+7=389 parameters, those that define the sub-functions in (2).

Algorithm in [11] provides an identification method to extract the values of sub-functions in (2). In this work, we use the same procedure but extended to take into account all levels of signal up to ADC saturation.

III. Device Under Test

The Device Under Test (DUT) is a commercial 18-bit Serial IO Analog to Digital Converter AD7982 of Analog Devices [12]. This converter is a Successive Approximation Register (SAR) type with no missing codes, maximum |INL| = 2.0LSB and DNL=-0.85LSB to +1.5LSB. It has a differential input range of 10Vpp and no pipeline delay. This device uses a serial peripheral interface which is SPI/QSPI/MICROWIRE/DSP compatible. The chosen package to be tested is the 3mmx3mm 10-Lead LFCSP.

This component in particular is to be qualified for its use in the Juice Icy Moons Explorer (JUICE) mission of the ESA. This kind of high resolution ADCs with serial interface is considered to be in line with the future trend of mixed-signal philosophy for space [13]. Not only by the reduction of cost implied by the use of COTS components, but also because the serial IO allows for simply swapping pin-to-pin compatible ADCs of different characteristics such as resolution, linearity, etc.

IV. Measurements Setup

The setup consists on a PCB board, a programmable power supply, an Applicos ATX7006 Analog ATE [14] and a PC, see Fig. 1.

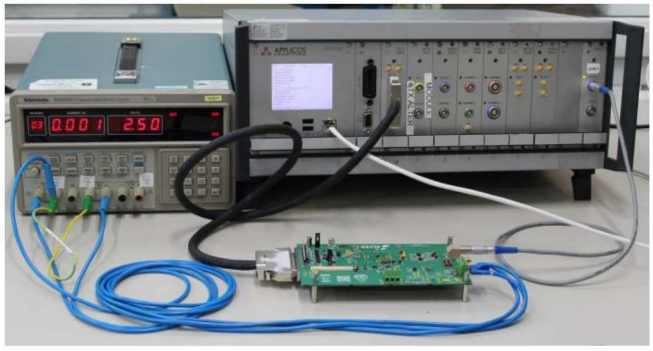

Fig. 1. Setup photograph

A. Hardware

The precision analog signal generation and digital codes capture are performed via an analog ATE which is connected to the DUT through a PCB board.

1) PCB Board

The board has been developed custom made for this application. It includes a reference, a signal conditioning circuit and power supply circuitry, see Fig 2.

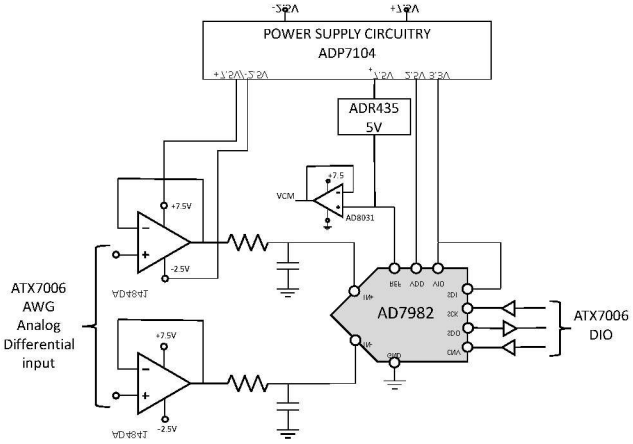

Fig. 2. Simplified Board Block Diagram

The configuration for the DUT is fully differential, and it can be inserted by soldering or with a socket in order to make comparative analysis, see Fig. 3 and 4.

The reference of the ADC is provided by a high precision ultralow noise with temperature drift curvature correction and extra implanted FET (XFET) 5.0V reference (ADR435B). Additionally, the reference source is capable of sourcing up to 30mA and sinking -20mA.

The signal conditioning circuit includes two unity gain stable, low noise ($2.1nV/\sqrt{Hz}$), low distortion and rail-to-rail output op amps (ADA4841). Both amplifiers are set at midscale

by the use of a reference voltage divider (590Ω) buffered by a rail-to-rail, high speed and fast settling amplifier (AD8031).

The power supplies are decoupled at the insertion in the test board and at each device. A single ground plane is applied to minimize the effect of high frequency noise interference.

The analog signal source is provided via a LEMO serie B connector to interface with the connection cable coming from ATX7006 Arbitrary Wave Generator (AWG).

The digital input/output is connected using a 68 SCSI connector with the Digital Input/Ouput (DIO) module of the analog ATE. The connection is made in single-ended low speed mode.

The DUT is not capable of driving the load implied by the SCSI connector and cable of the ATE digital interface. Therefore, the serial communication from the ADC to the digital capture circuitry of the ATE is performed via a digital buffer (SN74LVC126).

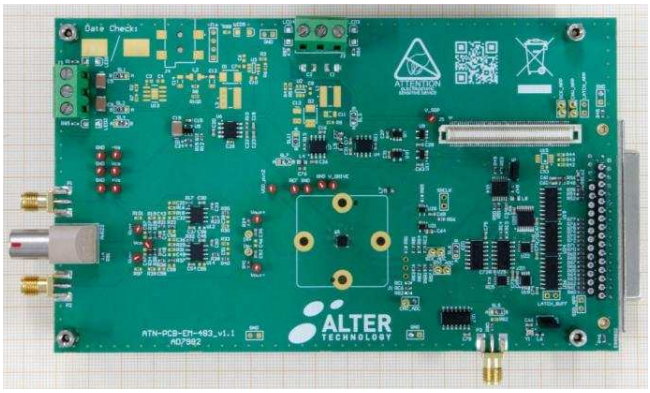

Fig. 3. PCB Board photograph with solded DUT

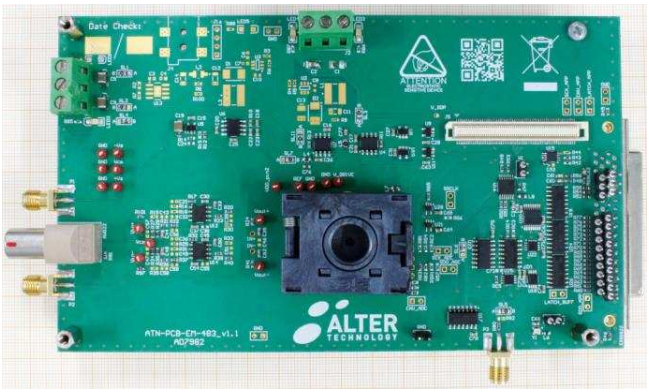

Fig. 4. PCB Board photograph with socket

2) Analog Generator and Digital Capture: ATE Applicos ATX7006

As already mentioned, the test setup included in this work contains as the input analog generator and digital signal capture the Applicos ATX7006 ATE test system, see Fig. 5, a fully integrated data converter test solution with very high accuracy, low noise and fast sampling features.

Generator and digitizer modules cover the range from low speed high accuracy testing to high speed medium accuracy testing. Auxiliary modules also provide linear reference and supply voltages, low jitter clocks and digital IO.

The ATX-series chassis use a well-considered grounding scheme that includes isolating noise on the backplane ground from the analog hardware.

A fully synchronization exists between wave generators and the digital capture module. The test signal was generated using the AWG22 module which is a 22-bit Arbitrary Waveform Generator (AWG), which includes output impedance lower than 1Ω and non-linearity of maximum ±3ppm of range. The update rate is DC-2Msps with a bandwidth of DC-500kHz. Analog signal of 1kHz comes out filtered by a 4-pole 12-kHz Butterworth LP filter integrated in AWG.

The capture of the digital data is performed by the digital module DIO with a depth of 4Mx24-bits serial words. The data capture rate is DC-50MHz. The capture of the digital data is fully synchronized with the analog source via pattern generator that controls both the analog generation and digital capture timings.

Fig. 5. Applicos ATX7006 front view

B. Software

The software has been developed in Visual Studio C#. The software communicates with the driver via Ethernet to obtain custom made behavior from a set of optional commands.

In this case, the software indicates the ATE to generate slightly saturated sinusoid excitations. The ATE has a limitation of 4Mwords to be capture in every register. To overcome this, the capture process is repeated to obtain a longer data set. However, these excitations are changed in phase, which is not directly allowed by the provided software. This avoid obtaining the same points of the equivalent sinusoid but repeated due to the full synchronization analog-to-digital of the system and coherent sampling. After the measurements have been run, the digital captured data of 4M words each register are retrieved and stored in a PC. Later, these results have been mathematically processed with Matlab.

V. EXPERIMENTS

In the experiments, a set of 36 registers of 4MSamples has been taken. The sinusoidal histogram test has been computed using all the registers, which implies an amount of 151 million of samples. In comparison, in the improved model it has only been used 1 register, which implies 4 million of samples. We can observe in Fig. 6 and 7 that despite of using a much lower number of samples, the improved model results are more adjusted and contain a less noisy behavior.

Fig. 8 shows a comparative of the methods under the same conditions, both using a single register of 4 million of samples.

It is noticeable that the noise averaging of the non-parametric segmented model is superior.

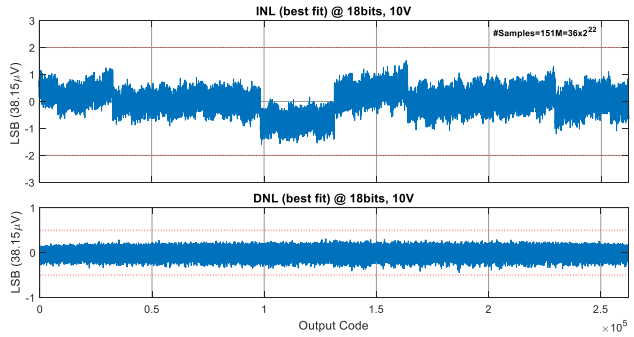

Fig. 6. Linearity test results of histogram method using 151MSamples

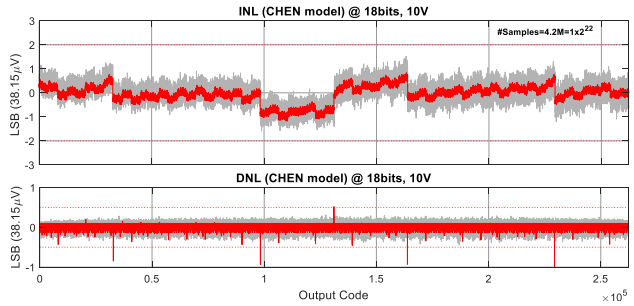

Fig. 7. Linearity test results of improved method using 4.2MSamples

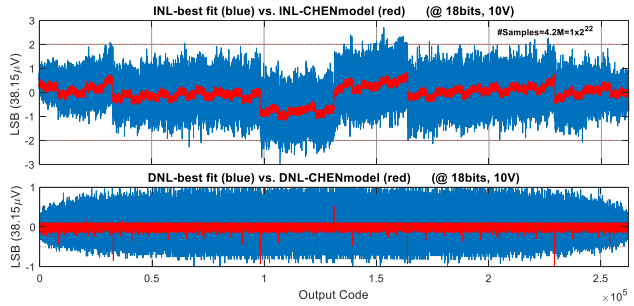

Fig. 8. Comparative of linearity test methods using 4.2MSamples

In Fig. 9 is shown the difference between different INLs when obtained with the two methods. The subtracted INLs has been obtained with two different configurations when filtering the digital power supply. We can observe that the stability against slight experiment conditions changes is better in the improved model than in the standard histogram method, as the difference between the INLs is more defined.

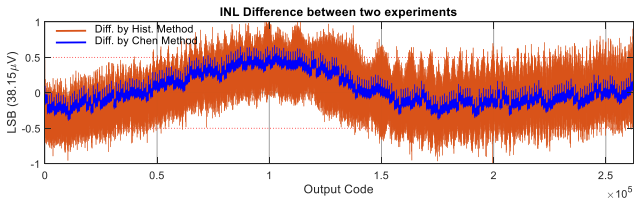

Fig. 9. Comparative of results difference using two different configurations

Fig. 10 shows the obtained INLs with both a solded DUT (orange line) and the use of a socket (blue line). It is noticeable that the improved algorithm is not fixed and can detect strong changes in the circuitry as a change in its linearity. The use of sockets can imply a great impact when testing this kind of components due to the support circuitry needed [15].

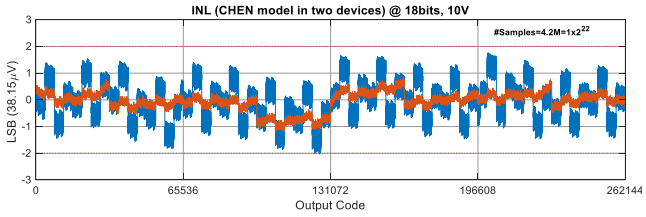

Fig. 10. Comparative of INL results of improved method with a without socket

VI. Conclusions

In high resolution ADCs, performing linearity test using the standard histogram method implies obtaining a large number of samples per code in order to average the measurement noise. This leads to long test time which involve high test costs. Space applications nowadays are trending to the use of COTS devices for cost saving purposes. This is aligned with a reduction in the cost of testing such COTS components. The present work has shown that it is possible to reduce the cost of the linearity test reducing the number of necessary samples. This is done by improving the noise averaging efficiency by using the very accurate input signal information dismissed in the accumulation of the histogram, redistribute the contribution of noise average to all samples and taking care of the high dependence behavior of segmented architectures of some types of high resolution ADCs.

VII. Acknowledgements

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Single Event Effects Analysis in Readout Integrated Circuits at Cryogenic Temperatures

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Abstract

This work presents the analyses of single event transients and functional interrupts measured on two designs of readout integrated circuit under a heavy ions beam cooled down at cryogenic temperatures. The analysis of the multiplicity of SETs in the pixel arrays is completed by means of the SEE prediction tool, MUSCA SEP3.

I. Introduction

Complementary metal oxide semiconductor (CMOS) technology is widely used in image sensors and infrared detector onboard launchers or satellites [1]. Actually, many optical applications, like Earth or space observation, the guidance system in a spacecraft are particularly critical. Photonic imager technology has been developed for various wavelengths from ultraviolet, through visible, to infrared. For IR detectors, the MCT material (AgCdTe) is used for the detection circuit. The detection circuit is hybrided on a CMOS circuit which performs the transfer and the control of the IR detector. The CMOS technology used in the readout circuit (ROIC) improves the integration of electronics function and reduce the dark current. A readout circuit is composed by vertical decoders, multiplexers, sequencer, and various logics and sequential cells.

However, these digital CMOS functions of image sensors are known to be sensitive to single event effects (SEE), such as single event transient (SET) or Single Event Functional Interrupt (SEFI) [2]. SETs can be induced by various ionizing particles, i.e., especially heavy ions and protons for the space environment space.

The first goal of this paper is to present the impact or not of cryogenic temperatures on SET and SEFI induced by heavy ions on two different readout circuits of IR image sensors developed by Sofradir.

The second goal is to analyze the multiplicity of SETs and to determine the origin of such events by the mean of the prediction tool MUSCA SEP3 (MUti-SCAle Single Event Phenomena Prediction Platform) [2][4]. Such analyze is relevant with the aim to anticipate the SEE sensitivity trends and propose new radiation tests protocol for IR detectors.

II. Radiation test of ROIC under heavy ions at cryogenic temperatures

A. Irradiation test setup

The irradiation test campaigns were performed at UCL (Université Catholique de Louvain - Belgium) with the heavy ion test facility. The CYClotron of Louvain la NEuve (CYCLONE) proposes different heavy ions species which are split in two "Ion cocktails", named M/Q= 5 and M/Q 3.3. The heavy ion species are summarized in Table 1 and Table 2. It has been confirmed (by SRIM simulations) that the penetration depth of the ions is enough to reach the sensitivity areas through the device layers.

Table 1: UCL ions cocktail M/Q=5

Ion	Energie (MeV)	Range (µm(Si))	LET (MeV.cm²/mg)
$^{15}N^{3+}$	60	59	3.3
$^{20}Ne^{4+}$	78	45	6.4
$^{40}Ar^{8+}$	151	40	15.9
$^{84}Kr^{17+}$	305	39	40.4
$^{124}Xe^{25+}$	420	37	67.7

Table 2 : UCL ions cocktail M/Q=3.3

Ion	Energie (MeV)	Range (µm(Si))	LET (MeV.cm²/mg)
$^{13}C^{4+}$	131	292	1.1
$^{22}Ne^{7+}$	235	216	3
$^{40}Ar^{12+}$	372	117	10.2
$^{58}Ni^{18+}$	567	100	20.4
$^{83}Kr^{25+}$	756	92	32.6

During all the testing measurements, the temperature of the chip was monitored and regulated by a cryostat to a range of temperature from 50K to 300K. During the complete irradiation campaign a GUARD (Graphical Universal

Autorange Delatcher) device has been used on the DUT's power in order to detect Single Event Latchup (SEL) and to prevent its destruction [4]. The global views of the experimental setups used during this irradiation campaign are shown in Figure 1:. The chamber has the shape of a barrel stretched vertically; its internal dimensions are 71 cm in height, 54 cm in width and 76 cm in depth. One side flange is used to support the board frame (25 x 25 cm²) and user connectors. The chamber is equipped with a vacuum system. In the case of the campaign the DUT is in a cryostat connected to the vacuum chamber in order to allow for cooling the temperature of the chip during the irradiation test.

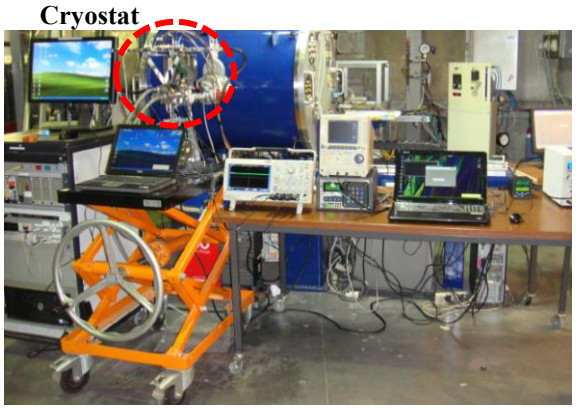
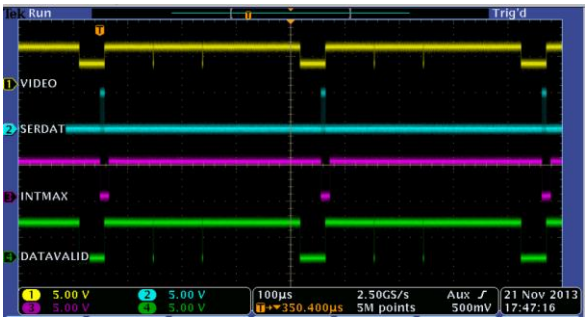
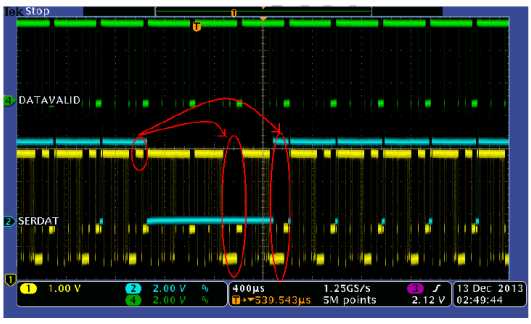


Figure 1: Global view of the SEE experimental setup of ROIC tested at UCL heavy ion facility in Louvain La Neuve, Belgium



(a)



(b)

Figure 2: (a) Reference levels of monitored signals, (b) Detection of SEFI observed on DATAVALID signal (green line), VIDEO signal (yellow line)) and its consequence on the SERDAT signal,(serial link, (blue line)) of the ROIC during heavy ion irradiation

B. Description of the device under test

The DUT during this irradiation test campaign was a readout integrated circuit. Three samples of each readout integrated circuit (ROIC) type have been characterized in order to evaluate the device variability. The complete tested ROIC were designed and developed by Sofradir in the 0.25µm CMOS technology.

The first ROIC (called A) is designed for infrared detectors (IR), and the second ROIC (called B) is designed for near infrared detectors (NIR). Each ROIC controls three pixel arrays corresponding to three spectral bands. From design point of view, the main difference between the two ROICs is the size of the three bands. The total number of pixel for each ROIC is the same, but the number of columns and lines is different. For confidential reasons, the detailed pixel pitch and the characteristics of each spectral band will not be presented.

The different single events planned to be analysed during the irradiation campaign were based on the monitoring of two main signals of the ROIC: (a) the VIDEO signal (yellow line in Figure 2:) issued from the pixel selection table, (b) the DATAVALID signal of the ROIC.

Different signatures of SET were measured on the pixel tables during the test campaign. Two metrics were used to classify the SET events as illustrated in Figure 3: (a) the duration of SETs, (b) the multiplicity of SETs.

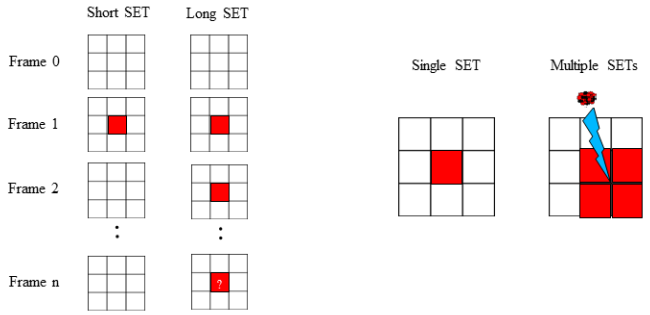


Figure 3: Classification of measured SETs: (a) as a function of its duration, (b) as a function of its multiplicity

Large and short SETs were defined as a function of the event duration observed on the VIDEO signal. If the SET event was observed during only one video frame, the SET event was called short SET. If the SET even was observed during two video frames of more, the SET event was called long SET.

Alongside, the multiplicity of SET was measured on the pixel table. The knowledge of SET multiplicity is very interesting to deduce the initial location of the event induced by the heavy ion on the ROIC (pixel table / row decoder …). This point will be presented and discussed in the next sections.

III. SINGLE EVENT EFFECTS RESULTS

A. Presentation of simple experimental SET data

Figure 4: and Figure 5: present the large SET cross sections measured on one sample of the readout devices "A" and "B", respectively the samples A1 and B1. The total large SET cross section (black triangles), the large multiple SET (red squares) and the large single SET (blue diamonds) have been measured for a heavy ion with a LET of about 32MeV.cm^2/mg and for a range of temperatures from 50K up to 293K. The large multiple SETs cross sections are one decade lower than the large single SETs cross. Error bars were calculated and plotted for each cross section value. The statistical errors are very low because of the large events counts.

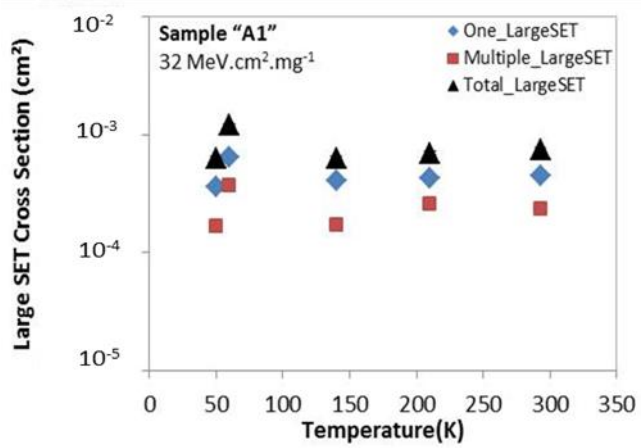


Figure 4: Large SET experimental cross sections measured on the sample "A1" during the test campaign under heavy ion (32 MeV.cm^2/mg), as a function of temperature from 50K to 293K.

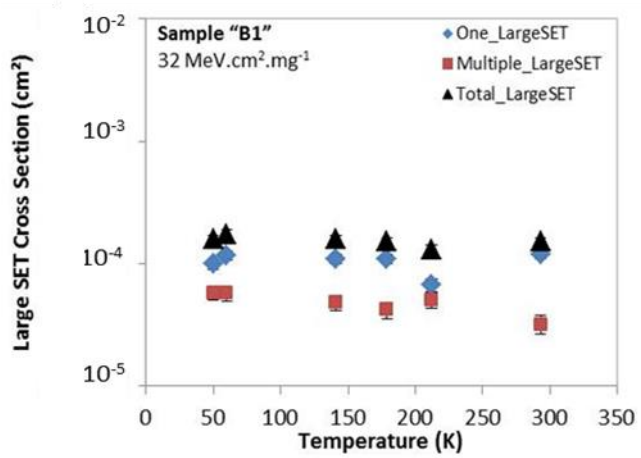


Figure 5: Large SET experimental cross sections measured on the sample "B1" during the test campaign under heavy ion (32 MeV.cm^2/mg), as a function of temperature from 50K to 293K.

Fig. 3 and Fig. 4 present the short SET cross sections measured on one sample of the readout devices "A" and "B", respectively the samples A1 and B1. The total short SET cross section (black triangles), the short multiple SETs (red squares) and the short single SETs (blue diamonds) have been calculated for a heavy ion with a LET of about 32MeV.cm^2/mg and for a range of temperatures from 50K up to 293K. Note that short multiple SETs have been detected only for sample ''A1'' at 55K. This point is discussed in section III.B. Total SETs cross sections are very close to short single SETs cross sections. It means that, the occurrence probability of complex short SET events is very low. As previously, error bars were calculated and plotted for each value of cross section. The statistical errors are very low because of the large events counts.

The results highlight a limited temperature dependence of large and short SETs susceptibilities for the two ROICs. This trend is in good agreement with a previous work done on D-Flip Flop CMOS device, i.e., for temperatures down to 77 K [4]. This limited impact temperature has been highlighted in CMOS gates due to two reasons: (a) saturation of carrier mobility and (b) transistors threshold voltage [4].

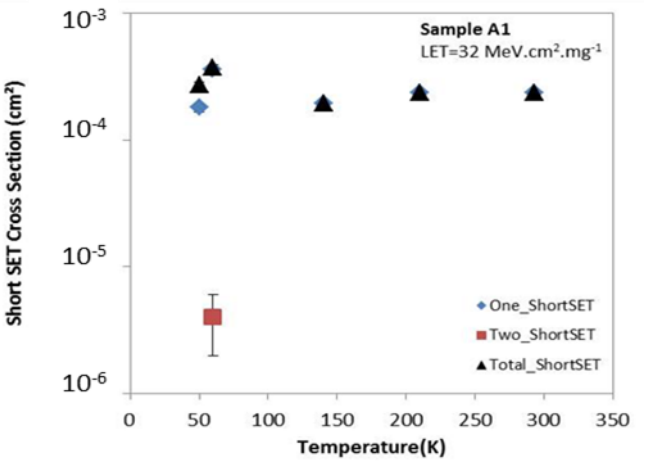


Figure 6: Short SET experimental cross sections measured on the sample "A1" during the test campaign under heavy ion (32 MeV.cm^2/mg), as a function of temperature from 50K to 293K.

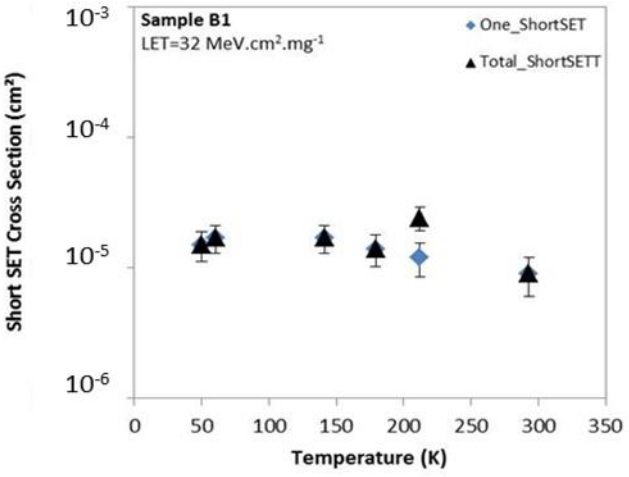


Figure 7: Short SET experimental cross sections measured on the sample "B1" during the test campaign under heavy ion (32 MeV.cm^2/mg), as a function of temperature from 50K to 293K.

B. Discussion of the multiplicity of simple SET

Figure 8: presents a histogram of large SET events depending on their multiplicity. Each bar of the histogram represents the number of large SET events on the sample "A1" during test campaign at 60K. It has been irradiated at a fluence $1.10^6.cm^{-2}$ with a heavy ion LET of about $32MeV.cm^2/mg$. As mentioned, the ROIC A contains three pixel arrays. The dimensions of the first array are 224 x 4 pixels (line x column). The second array is based on 224 x 4 pixels. The third array is based on 448 x 4 pixels. In this histogram, the single large SET events are the main events observed. The number of double large SET (120) is lower by a factor of three than the simple large SET numbers (369). The figure highlights the low probability to observe more than two events on the neighbourhood of a pixel. But the event with the seven multiple events during a single video frame seem to be not due to the strike of a heavy ion on the pixel arrays. In this histogram the category of events higher than 224 (the lower column size of pixel tables) is considered as complex SET events.

Finally, in order to confirm the hypothesis of the origin of the multiplicity of short and large SET an analysis has been performed by the mean of simulation based on the Monte Carlo SEE prediction tool, MUSCA SEP3 [2][4].

SEE prediction tools are used to analyse experimental data and confirm the hypotheses of the SEE experimental trends. Based on the design parameters of the pixel table provided by Sofradir, the SET sensitivity of the ROIC has been calculated by the mean of the tool MUSCA SEP3 [2][4]. The tool uses a Monte Carlo approach coupled in a sequential modeling all the physical and electrical processes, from the device down to the semiconductor target. The following steps are considered: (a) the modeling of the radiation constraint, (b) the transport mechanisms of radiation particles (in this work heavy ions) through the layer stack (BEOL) [**Error! Reference source not found.**], (c) the generation of electron-hole pairs in the silicon, (d) the mechanisms of charges transport and collection, (e) the circuit feedback.

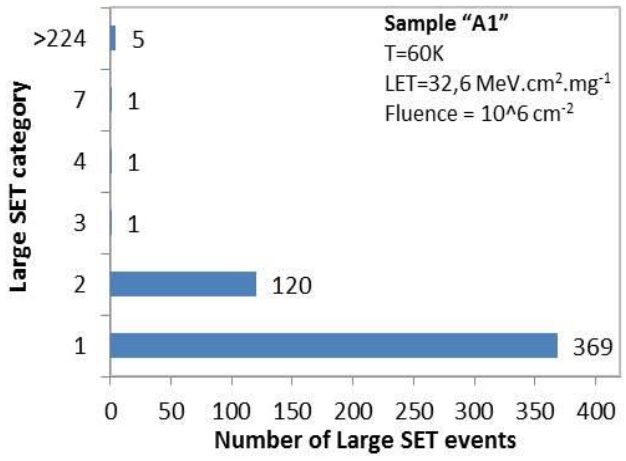


Figure 8: Number of Large SET events in each categories measured on the sample "A1" during the test campaign at 60K under heavy ion beam, fluence=10^6 $.cm^{-2}$, LET=$32MeV.cm^2/mg$.

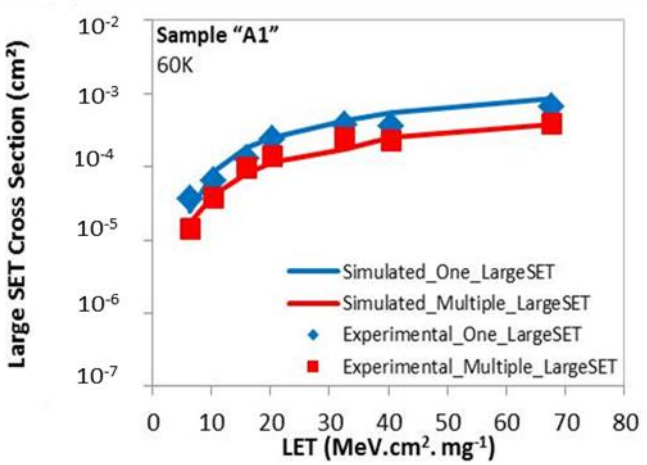


Figure 9: Comparison of large SET experimental cross section and simulations results from MUSCA SEP3 for the ROIC "A1", as a function of LET at 60K.

Figure 9: presents the SET cross sections calculated for sample "A1" under heavy ions. The multiplicity of the SET events is highlighted and it confirms that only two SET could be induced by a single particle in the pixel table for this technology. It means that the origin of events higher than four is due to events on the readout circuit, such as in a DFF of a line or column decoders of the pixel table.

Here, the analysis of short and large SETs of the pixel selection table (named simple SET) was presented. In the next section, the analysis of complex SET will be discussed.

C. Presentation of complex experimental SET data

Here is presented complex large SET which has been defined as a SET event with a multiplicity higher than the length of a line and/or column of the pixel selection table. The comparison between simple (black squares) and complex (red dots) SET measured on the pixel array is presented in Figure 10:.

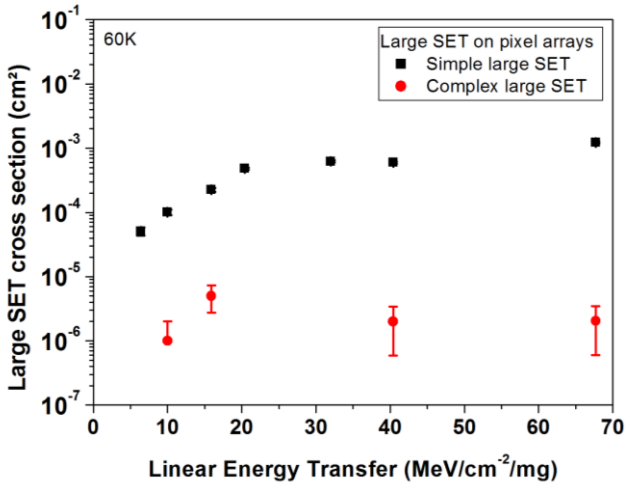


Figure 10: Comparison of simple (black squares) and complex (red dots) large SET obtained on pixel array of ROIC B as a function of LET during heavy ion irradiation at 60K

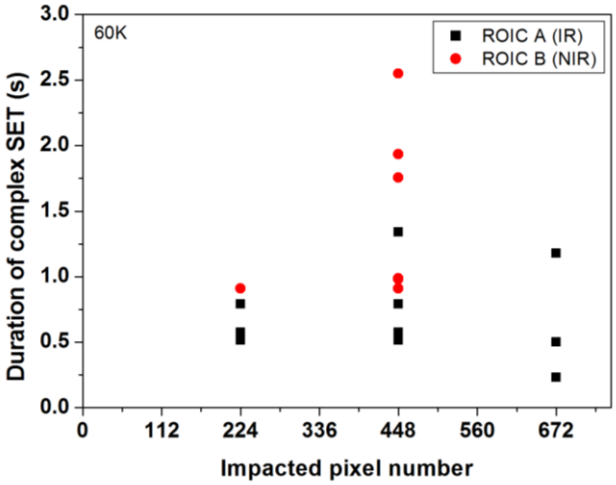


Figure 11: Duration of complex SET as a function the number of impacted pixel on ROIC A (black squares) and ROIC B (red dots) during heavy ion irradiation at 60K.

The occurrence of complex large SET is lower by a factor of about 2 orders of magnitude for all the investigated LET range. Even if the cross section of complex large SET is low, because of the critical impact of such complex SET, it is necessary to analyse these categories of event.

Figure 11: shows the characteristics (in terms of duration and impacted pixels) of complex large SETs observed on the ROIC A and ROIC B at 60K for heavy ions with a LET from 6.6 up to 67.7 MeV.cm^2/mg. The event signatures must be identified as a function of the number of pixels affected by a complex long SET event. Three categories of error signature can be identified. The three event signatures correspond to multiples of number of lines of pixel arrays of the ROICs. The events have the same large SET signature which consists in a succession of 112, 224 or 448 large SETs during a single video frame. These complex large SETs correspond to a change of the level of all pixels of a column of the third pixel array of the ROIC B. These events can induce very long durations of video signal inoperability. Note that, the Video signal recovers its reference level without any on/off cycle.

This kind of complex large SET signature must been attributed to an event (such as SEU) on the vertical decoder of pixel arrays.

D. SEFI sensitivity of ROIC

In this section, two categories of SEFI are shown: SEFI on the VIDEO frame and SEFI on a multiplexer used in the control of the phase of the VIDEO signal.

Error! Reference source not found. shows the SEFI cross sections of the ROIC A obtained under heavy ions with LETs from 3.3 MeV/cm^{-2}/mg up to 67.7 MeV.cm^2/mg at 60K. Note that same trend have been observed by ROIC B. The error bars correspond to statistic error of the measurements. A SEFI event corresponds to a change of state of the *VIDEO* signal during a frame. The SEFI sensitivity of the two ROIC designs seems to be quite equivalent. It is interesting to note that the changes of state of the VIDEO signal request a power cycle (on/off) of the device in order to recover the reference pixel level. This kind of event should be due to an event on the configuration register used in the ROIC circuit. The other point which needs to be highlighted is the constant SEFI sensitivity as a function of the LET (Liner Energy Transfer). The LET threshold is about 6.6 MeV.cm^2/mg. Note that the statistic is really poor.

Error! Reference source not found. shows the SEFI cross section obtained under heavy ions with LETs from 3.3 MeV/cm^{-2}/mg up to 67.7 MeV.cm^2/mg for the design of ROIC A (black squares) and ROIC B (red dots). As previously, the error bars correspond to statistic error of the measurements. The SEFI event corresponds to a failure of the multiplexer or its configuration register. A wide variability of this SEFI type has been observed on the samples of the two ROIC; higher than one decade in some case. It seems that the design of the multiplexer and its configuration register is more sensitive to SEFIs for the ROIC B (NIR detector) than the ROIC A (IR detector). This difference is highlighted by the LET threshold which is increased by a factor of 2. The LET threshold of the ROIC A reaches 10 MeV.cm^2/mg.

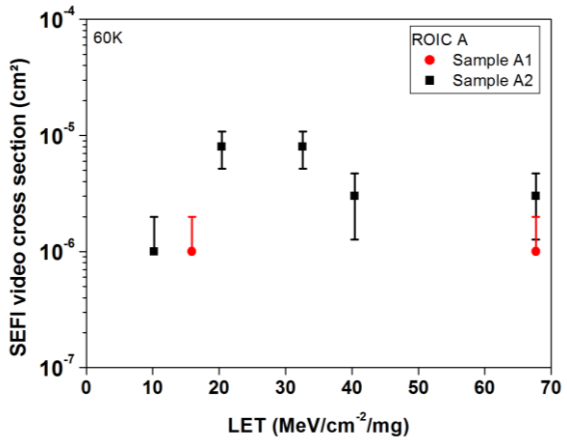


Figure 12: SEFI video cross section of two samples, A1 (red dots) and A2 (black squares) of the ROIC A design during heavy ion irradiation at 60K

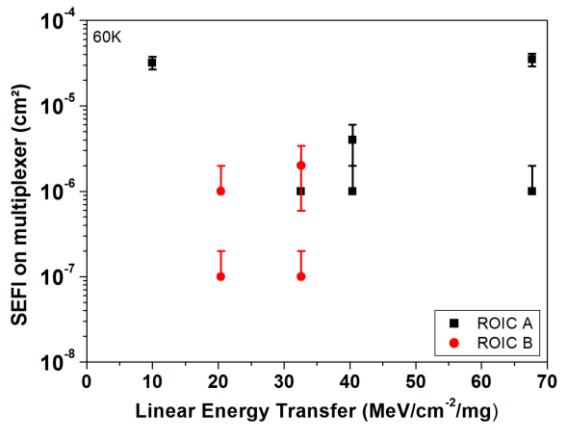


Figure 13: SEFI cross section of multiplexer of ROIC A (black squares) and ROIC B (red dots) under heavy ion irradiation at 60K

Figure 14: shows the effect of the temperature on the SEFI video cross section obtained for two samples of the ROIC A design, the sample A1 (black squares) and the sample A2 (red dots) for a heavy ion beam with a LET of about 67.7 MeV.cm^2/mg. As previously, the error bars correspond to statistic error of the measurements. No temperature dependence can be observed. This point is also confirmed for other LETs and design B of the ROIC.

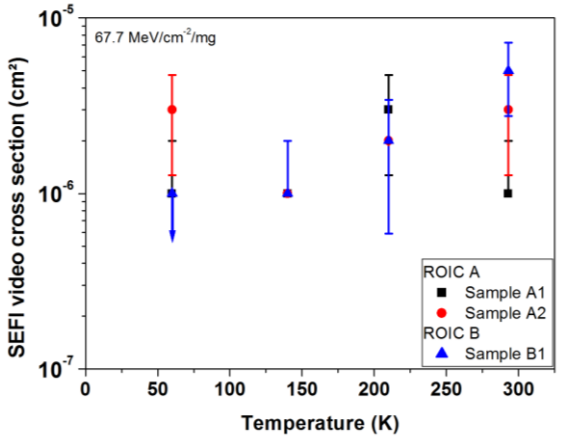


Figure 14: Effect of temperature of the SEFI cross section of ROIC A (black squares, red dots) and ROIC B (blue triangles) under heavy ion irradiation at 60K

Experimental data confirmed the very limited impact of the cryogenic temperature on SEE occurrence on the two ROICs [7][8]. These results are consistent with previous simulation results on elementary gates (DFF) [4][5].

IV. Conclusion

This work presented the analyses of single event transients and functional interrupts measured on two designs of readout integrated circuit under a heavy ions beam cooled down at cryogenic temperatures. The analysis of the multiplicity of SETs in the pixel arrays was completed by means of the SEE prediction tool, MUSCA SEP3. Experimental data confirmed the very limited impact of the cryogenic temperature on SEE occurrence on the two ROICs. These results are consistent with previous simulation results on elementary gates (DFF). It appears that for this technology used by Sofradir for their ROIC of IR detectors, the future irradiation test campaigns should be realized at room temperature. This allows for reducing the complexity of such irradiation tests during the development of IR detector for a space mission.

V. References

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Validation of a High Resolution ADC for Space Applications

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Abstract

We present the test results of a radiation hardened, high resolution ADC for space applications. The ADC is a low-noise, low sampling rate, radiation hardened device optimized to operate in the frequency range DC to 40kHz. The ADC is implemented in the 150nm CMOS-SOI process of Atmel® following a rigorous design flow and radiation hardening strategy. The ADC features a fully differential analog input voltage interface with an input range of ±3.3V. A sampling rate of a up to 240kSps is possible thanks to the selectable Over-sampling Ratio which can be as high as 2048x. At low sampling rates, the ADC can achieve a very high SNR of up to 108dB over the entire dynamic range, which is translated to an ENOB of 18 bit in terms of noise performance. The static and dynamic performance of the device has been tested in a radiation environment of up to 300krad Total Dose and a maximum LET of 88 MeV/mg/cm^2 using heavy-ions exhibiting no hard fail, no serious performance degradation or latch up.

I. INTRODUCTION

The Analogue-to-Digital Converter (ADC) presented herein is a single channel, low-noise, radiation hardened device, adequate for sampling signals ranging from DC to 40kHz, and is the continuation of the work presented in [1]. The ADC converts the input voltage into a 24-bit digital word using an SPI-like serial interface. The system architecture is based on a 2nd order, discrete-time (switched capacitor), Sigma-Delta modulator, which provides superior noise and linearity performance. The first integrator features the *Correlated Double Sampling* (CDS) technique to minimize flicker noise and perform auto-zeroing function [2]. The modulator is followed by a decimation filter which reduces the sampling frequency by a factor of the selected Over-Sampling Ratio (OSR) to the nominal output sampling rate f_s. Sampling rates as high as 240 kSps can be supported with the appropriate combination of the clock frequency f_{MCLK} and OSR values. The ADC supports both differential and single-ended operation using separate supplies for the analogue and digital parts and operates on a single, externally provided system clock (MCLK).

In terms of applications, the device is well suited for high accuracy instrumentation, measurement and control applications mainly found in space scientific missions where high dynamic range and low frequency operation is required.

A. *System architecture*

The system block diagram is shown in Figure 1.

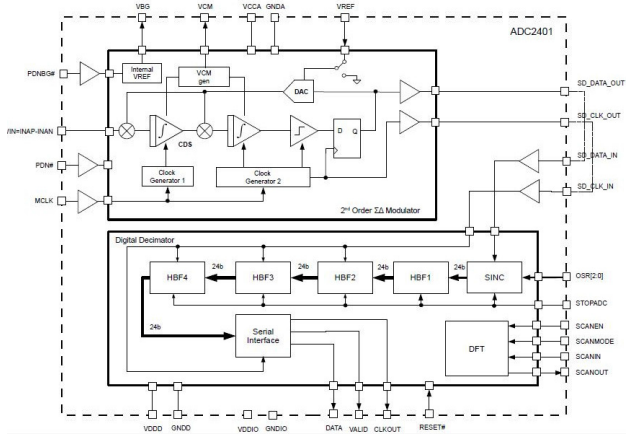

Figure 1: System block diagram

The differential analog voltage signal is applied at INAP, INAN inputs. The difference VIN=INAP-INAN is modulated by the ΣΔ modulator working at a maximum nominal frequency of 12MHz. The modulator requires two reference voltages; VCM sets the output common mode voltage of the amplifiers implementing the integrators to obtain a balanced swing and maximize the dynamic range. The second one (VREF) is used for sampling.

Two clock generator blocks generate all the required clock phases by taking an externally provided clock as an input (MCLK). Next, the ΣΔ modulated signal (SIGMA) is driven along with the clock to the digital part. There is only one

clock domain for the entire system and the digital part is clocked from the same clock used to latch the ΣΔ signal in the analog part, being effectively a replica of the main system clock. That clocking scheme eliminates the synchronization problem between the sampling of the analogue signal and the decimation of the ΣΔ output in the digital part. The decimator is implemented with a SINC filter offering four selectable over-sampling ratios from 64x to 2048x through the dedicated OSR[2:0] inputs followed by four half-band filters. Each sample is outputted in 24-bit word format through a simple serial interface along with the clock.

B. *Radiation Hardening*

The digital part is hardened through the global insertion of TMR logic with voting scheme in all the Finite State Machines (FSMs) and counters, a synchronous reset and the use of rad-hard proven standard cells during synthesis, including latches and flip-flops. The analog part is hardened using relaxed layout rules, guard rings and extensive use of enclosed layout transistors (ELT). The layout is almost totally immune to Single Event Latch-up (SEL) thanks to the deep trench isolation option of the process (DTI). Hardening against Single-Event Transient effects (SET) is achieved by placing capacitors of the appropriate size to every sensitive analogue node.

II. ELECTRICAL VALIDATION

The static and dynamic performances of the device were extracted across the specified ambient temperature range of -55°C ≤ *Ta* ≤ +125°C and supply voltage range of 3.3V±10%, 1.8V±10% for the analogue and digital part respectively.

A. *Power consumption*

The power consumption was measured for various OSR and up to the maximum attained clock frequency as depicted in Figure 2.

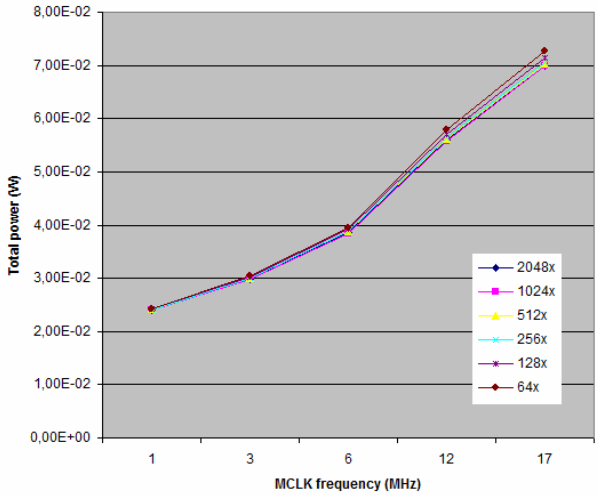

Figure 2: Total power consumption (conditions typ.)

B. *AC performance*

A representative Power Spectral Density (PSD) plot obtained at f_s=488Sps is provided in Figure 3.

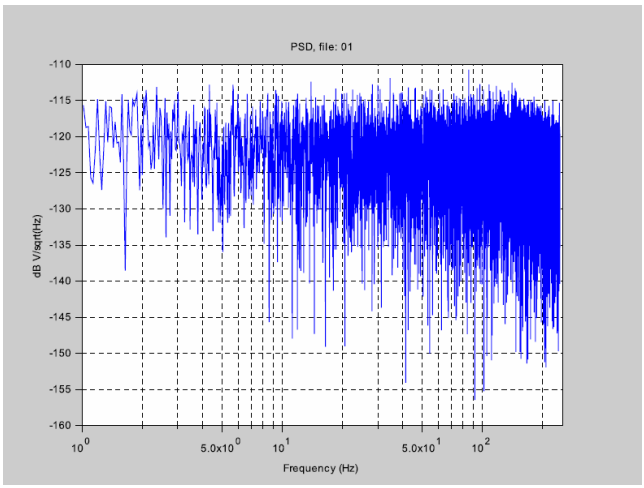

Figure 3: PSD plot at Ta=25deg.C for f_{MCLK}=1MHz, fs=488Sps and Vin=+0.583VDC.

The RMS noise *Vn* in function with the input voltage *Vin* and sampling rate f_s is shown in Figure 4 and Figure 5 respectively.

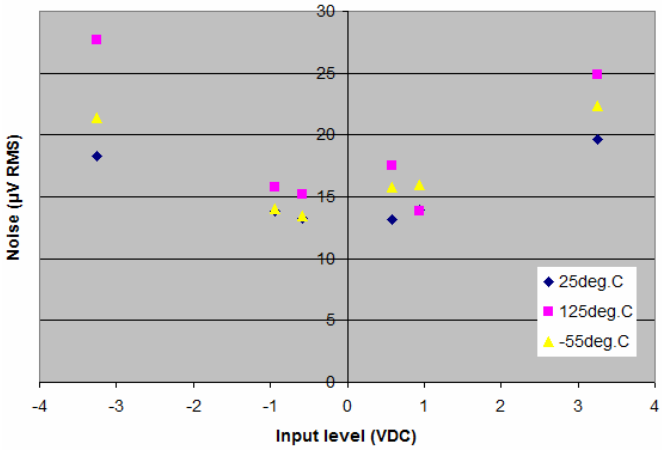

Figure 4: RMS noise vs. input level across temperature (vsupply=nominal, OSR=2048, f_{MCLK}=1MHz, fs=488Sps)

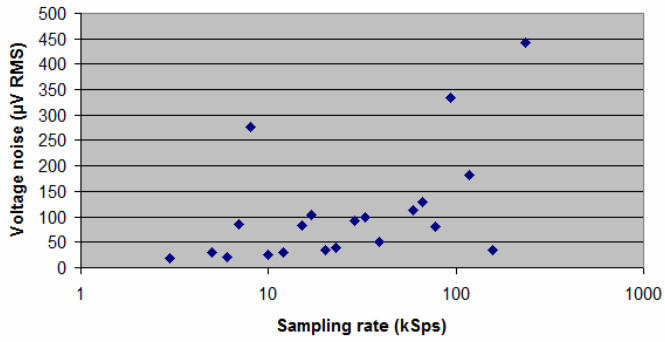

Figure 5: RMS noise vs. sampling rate (Ta=25deg.C)

The analogue bandwidth is almost a linear function of the sampling rate as depicted in Figure 6.

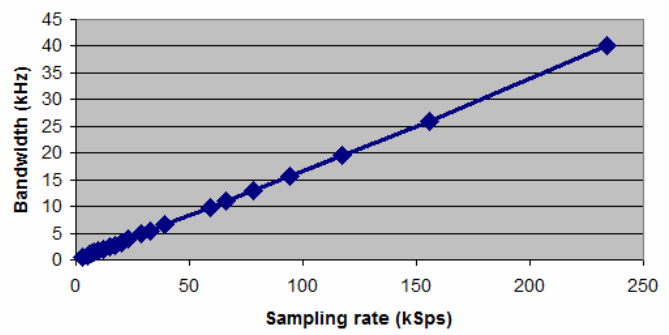

Figure 6: Analogue bandwidth vs. sampling rate (Ta=25deg.C)

The Effective Number Of Bits (ENOB) in function with the sampling rate is shown in Figure 7. The maximum ENOB figure of 18 bit is obtained up to *fs*=3kSps when OSR is maximum (2048x) and can be maintained above 17 bit to 12kSps.

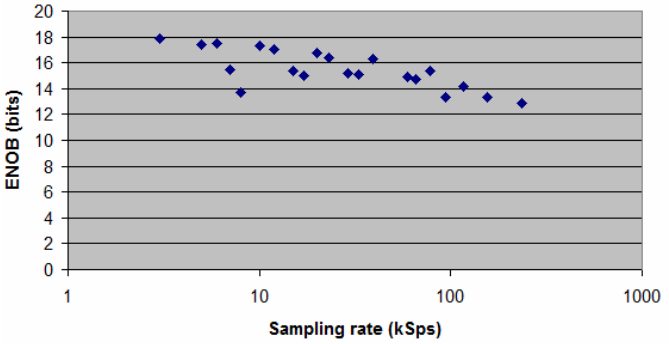

Figure 7: ENOB vs. sampling rate (Ta=25deg.C)

The Signal-to-Noise Ratio (SNR) in function with the sampling rate is shown in Figure 8.

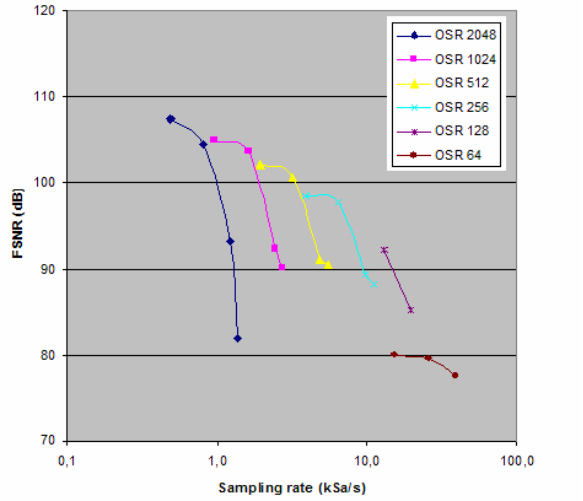

Figure 8: SNR vs. sampling rate for various OSR

A reconstructed sampled sine wave signal is illustrated in Figure 9.

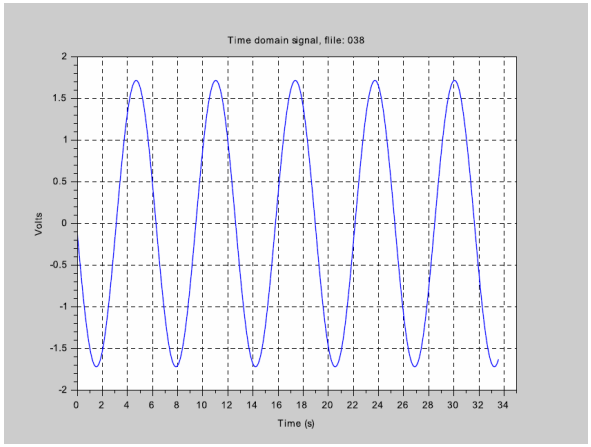

Figure 9: Time series of sampled sine wave 0.16Hz at 3.2Vpp (f_{MCLK}=1MHz, OSR=2048, fs=488Sps)

III. TOTAL DOSE TEST

The Total Ionization Dose (TID) test campaign was held at the Co60 facility of ESA-ESTEC according to the ESCC basic specification [3]. The target dose of 300krad (Si) was achieved in five exposures at a fixed dose rate of 59.7 rad/min (Si). All the samples remained fully functional up to the dose of 300krad. The only deterioration of the performance was the leakage current of the digital core and the I/O pads which increased by 13-20 times after the 133krad step, but fully recovered at the end of the campaign (Figure 10). No transient events have been detected during the exposure.

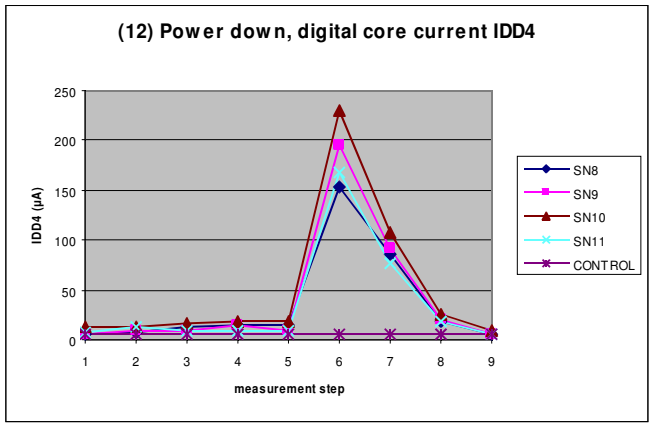

Figure 10: Leakage current variation vs. TID steps

IV. HEAVY ION TEST

The HI test campaign to evaluate the sensitivity of the device to Single-Event Latch-up (SEL) and Single-Event Effects (SEE) was held at HIF facility of UCL Louvain-la-Neuve in Belgium according to the ECSS basic specification [4]. All the samples remained fully functional throughout the test campaign. No SEL, SEU, or SEFI was detected in any of the tested samples and for LET up to 88.4 MeV/mg/cm^2 apart from some SET in the analogue and the I/O buffer current consumption, deemed as insignificant.

V. SUMMARY OF PERFORMANCE

The key measured performances are summarized in Table 1.

Table 1: Performance summary

Specifications	Value
Supply voltage	3.3V and 1.8V (±10%)
Input voltage range	±3.3Vpp
Signal-to-Noise Ratio	108 dB typ
Noise at fs<1kSps	<30µVrms typ
ENOB	18 bit
Sampling rate	Up to 240 kSps
Analogue bandwidth	DC to 40kHz
Monotonicity	Full code range
Power dissipation	70 mW max
LET for SEL/SEU immunity	immune up to 88 MeV/mg/cm^2
TID tolerance	immune up to 300krad
Operating temperature range	-55°C ≤ T ≤ 125°C

III. CONCLUSION

A high resolution ADC suitable for low frequency instrumentation applications has been specified, designed and validated in the 0.15µm CMOS-SOI technology. The obtained dynamic performance of 108dB SNR is a bit lower than the simulated value (110dB) announced in [1], but it well exceeds the desired specifications set at the beginning (>102dB). The performance limitation with respect to the theoretical predictions of the model comes from the analogue part, and more specifically from the sigma-delta modulator. The radiation endurance of the device is deemed very satisfactory and beyond any expectations.

VI. REFERENCES

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Session D

Custom cell-, circuit-, and system design of ICs for space applications

Radiation Hard X-Band Phase Locked Loop and Transceiver in 0.25µm SiGe Technology

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Abstract

This paper presents the experimental results of radiation hard phase-locked loop (PLL) and transceiver (TRX) chips in X-band frequency. The chips are designed and fabricated in IHP's radiation hard SiGe BiCMOS SGB25V technology having peak cutoff frequency (f_T) of 80 GHz. Total Ionizing Dose (TID) and Single Event Effect (SEE) tests have been performed for the chips. The circuit level performance degradation associated with these tests is found to be negligible.

I. Introduction

X-band frequencies (8 - 12 GHz) are used for space and satellite communication both in civil and military applications. Traditionally, discrete microwave integrated circuits implemented in III−V technologies have been combined and used for these applications due to their performance advantages over Si technologies [1]-[3]. Unfortunately, such transceiver modules are typically power hungry, large, heavy and hence costly [4], [5]. SiGe HBT technology, being inherently tolerant to TID, good integration capabilities, medium cost and superior performance over Si technology has big advantage for space and satellite communication application. Other potential application areas are space sector, miniaturized radars mounted on drones, autonomous industrial vehicles or in toys, used for navigation and obstacles avoidance, which would benefit from more compact size, lower energy consumption and ultimately much lower cost at higher production volumes. As mostly demanded, a phased locked loop (PLL) chip and a transceiver (TRX) chip are designed and implemented in SiGe BiCMOS technology. The ICs are tested under normal operation condition as well as under irradiation. The chip details are presented in the following sections.

II. X-Band Circuit Design

The SiGe BiCMOS technology used for the design is the IHP SiGe SGB25V technology with 80GHz peak cut-off frequency (f_T) and 95GHz peak maximum oscillation frequency (f_{max}). This work is a part of a Eurostars funded project of development of a radiation hard mixed-signal library for commercialization of space qualified ICs, "LIBRA". As part of analogue library, a low noise amplifier (LNA), a voltage controlled oscillator (VCO), a phase locked loop (PLL), receiver (RX) and a transceiver (TRX) cell, all in the X-band have been developed. This paper reports the design and measurement results of PLL and TRX circuits. The SiGe HBT is used in the circuit without any intentional hardening considering its robustness. NMOS layout is drawn with special layout technique to ensure radiation tolerance.

A. Phase Locked Loop (PLL)

Figure 1 shows the block diagram of the designed PLL. It consists of VCO, frequency divider, phase frequency detector and charge pump. The VCO is of differential cross-coupled type using bipolar transistors. The divider has a divide ratio of 128. The PLL circuit utilizes dual loop topology with coarse and fine tuning inputs at oscillator. The divider also utilizes bipolar transistor. The phase frequency detector (PFD) and charge pumps are designed with CMOS transistors. For radiation hardness, the layout of nmos gate is drawn with closed gate inside active region. Chip area is 1.22 mm x 0.81 mm. Figure 2 shows the realized PLL chip photo with pad names.

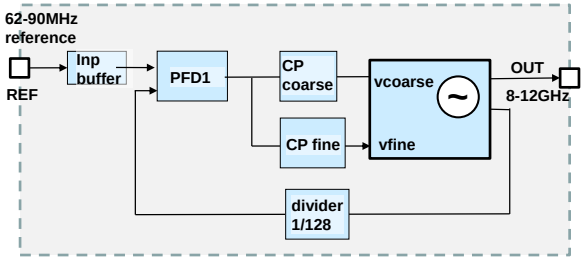

Figure 1: Simplified PLL block diagram

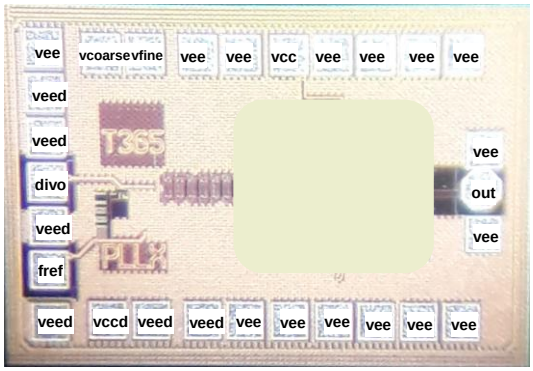

Figure 2: PLL chip photo

B. *Transceiver (TRX)*

Figure 3 shows the transceiver block diagram. It contains voltage controlled oscillator (VCO), power splitter, power amplifier (PA), poly-phase filter (PPF), low-noise amplifier (LAN), quadrature mixer. Built-in selftest (BIST) structure is included to test the circuit functionality without antenna and high frequency equipment. Chip area is 1.84 mm x 1.1 mm. Figure 4**Fehler! Verweisquelle konnte nicht gefunden werden.** shows the realized TRX chip photo with pad names.

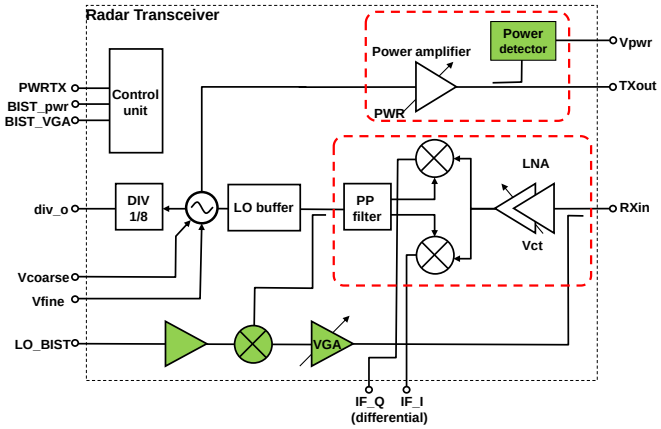

Figure 3: Simplified Transceiver block diagram

Figure 4: Transceiver chip photo

III. Electrical Test

A. *Phase Locked Loop (PLL)*

The realized PLL chip is wire-bonded on PCB and other components are soldered. Figure 5 shows the PLL test board. Measurement is performed with Rohde & Schwarz signal source analyser.The chip is tested as a free running VCO by changing the tuning voltage and observing the output frequency and power. The supply voltage was also changed by ± 100 mV from the nominal supply of 2.5 V. Figure 6 and Figure 7 show the measured output frequency and power of the VCO. Output frequency varies approximately from 8 GHz to 12 GHz for a tuning voltage of 0 - 3.3 V. The output power is relatively low at the lower frequency ranges (8-9.5GHz) but is stable at the upper frequency range. The divider output frequency and power are also measured and shown in Figure 8 and Figure 9. The divider output frequency varies approximately from 62.5 MHz to 90 MHz (divide ratio of 128). Divider output power is almost constant (-9.5 dBm) for the full frequency range.

Figure 5: PLL (VCO) test board with chip mounted

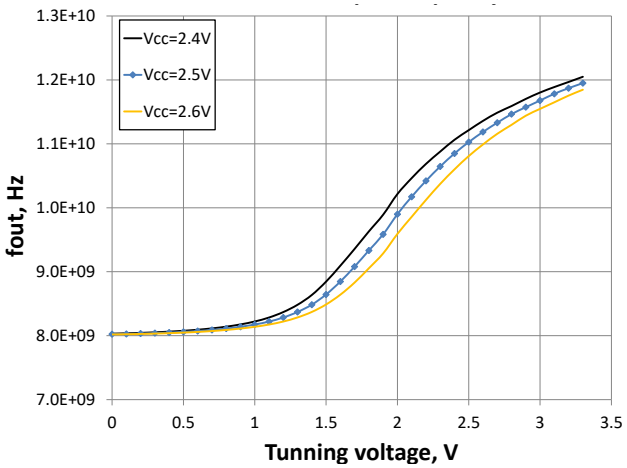

Figure 6: PLL (VCO) output frequency vs tuning voltage

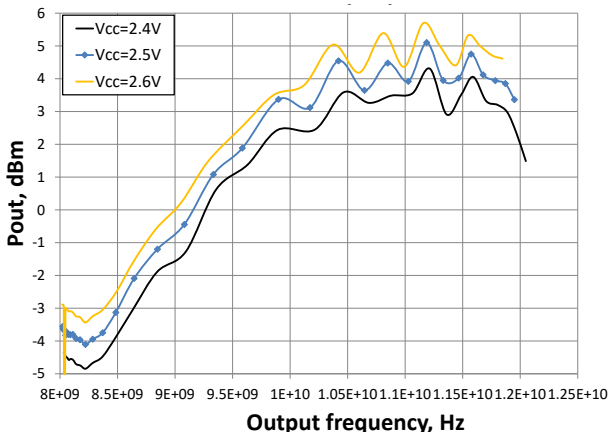

Figure 7: PLL (VCO) output power vs frequency…

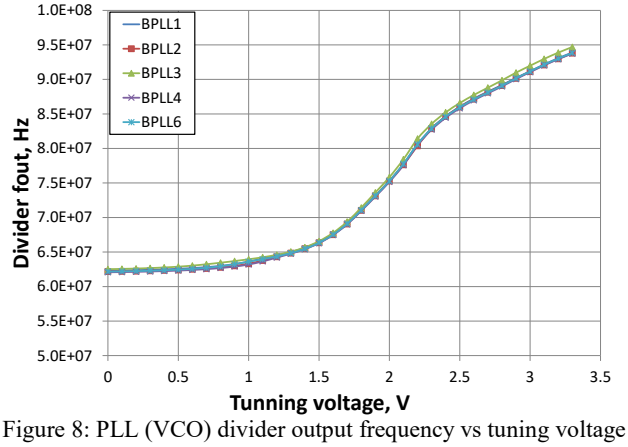

Figure 8: PLL (VCO) divider output frequency vs tuning voltage

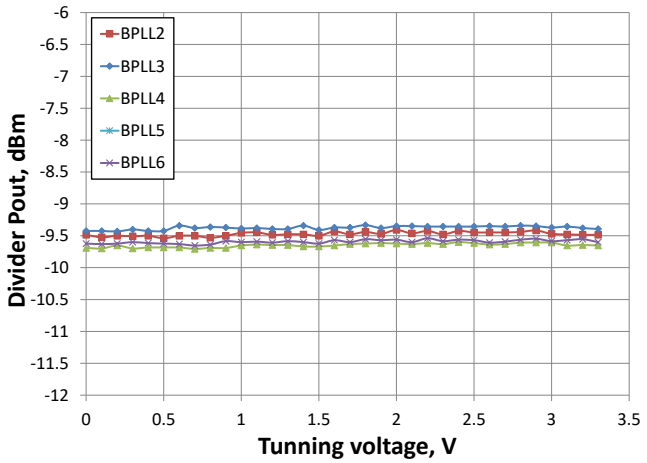

Figure 9: PLL (VCO) divider output power vs tuning voltage

The PLL functionality of the chip is not fully satisfactory. It uses on-chip loop filter and reference input block capacitor. These were not properly scaled. The locking of the PLL is measured from 8.2 GHz to 10.5 GHz for reference frequency of 256 MHz to 330 MHz which is 4th harmonics of divider output. The modification for improvement is implemented in a later design step and now under fabrication.

Table 1: PLL measurement results

	Output frequency (GHz) for PLL Boards				
Ref. Freq. (MHz)	B1	B2	B5	B6	Div. ratio
256	8.19	8.19	8.19	8.19	31.99
300	9.59	9.59	9.59	9.59	31.97
330	10.56	10.56	10.56	10.56	31.97

Measured phase noise at 9.875 GHz and 10 MHz offset is - 105 dBc.

B. Transceiver (TRX)

Like the PLL chip, the realized TRX chip is also wire-bonded on PCB and other components are soldered. Figure 10 shows the TRX test board with chip on board. Measurement is performed with Rohde & Schwarz signal source analyser, signal generator, oscilloscope. Firstly, the chip is tested as VCO by changing the tuning voltage and observing the output frequency and power. The supply voltage was also changed by ± 300 mV from nominal supply of 3.3 V. Figure 11 and Figure 12 show the measured output frequency and power of the TRX VCO. Output frequency varies approximately from 10.6 GHz to 12.6 GHz for a tuning voltage of 0 - 3.6 V. The TX output power is 9 dBm and stable with some exception for measurement error. The divider output frequency and power are also measured.

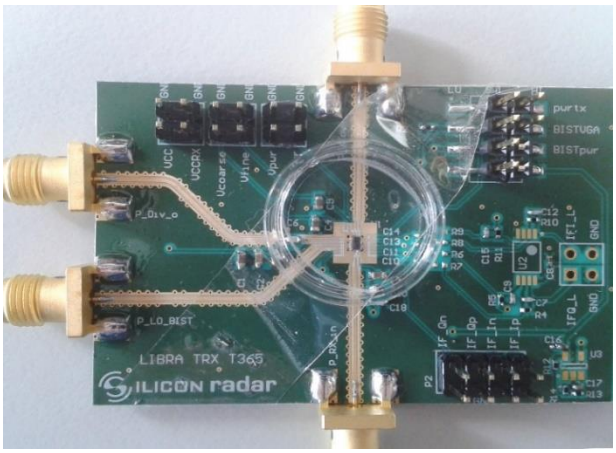

Figure 10: TRX test board with chip mounted

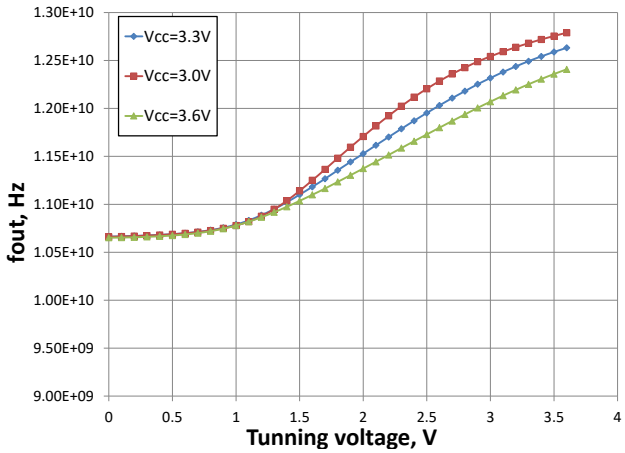

Figure 11: TX (VCO) output frequency vs tuning voltage

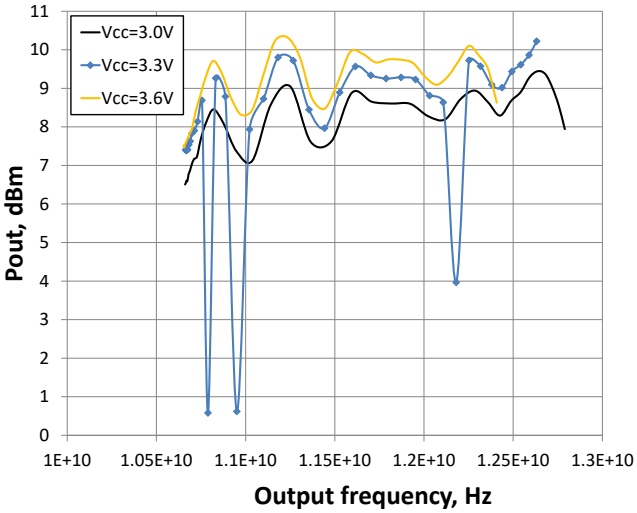

Figure 12: TX (VCO) output power vs frequency

The receiver (RX) is characterized by feeding RF signal at RX input having an offset to LO (TX) frequency. The IF outputs are measured with an oscilloscope. Figure 13 shows a sample of measured IF signal with a RX frequency of 10.713 GHz, RX input power of - 20 dBm and IF frequency of 10 MHz. The receiver (IF) gain is calculated over the RX input power. Figure 14 and Figure 15 show the measured gain for different frequency and different input power respectively.

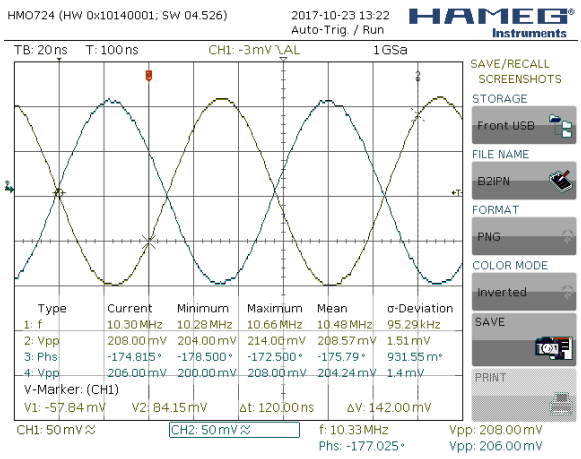

Figure 13: Measured IFIp and IFIn

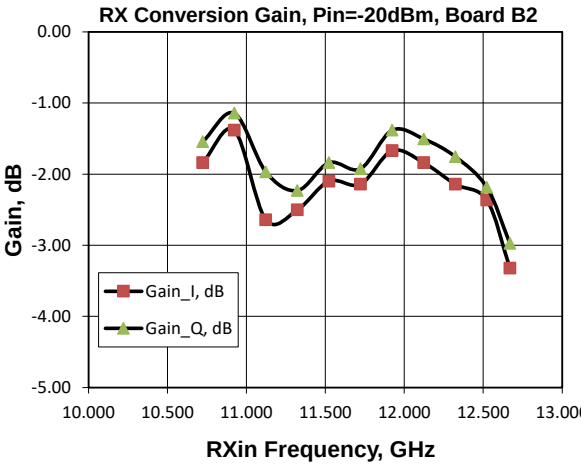

Figure 14: RX gain (single ended) vs frequency

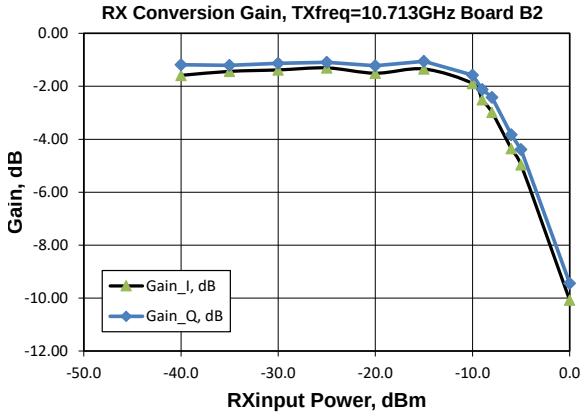

Figure 15: RX gain (single ended) vs RX input power

IV. Test Under Irradiation

After electrical characterization under normal operation condition, the chips are tested under radiation. TID test under gamma ray and SEE test under heavy ion irradiation have been performed.

A. Total Ionizing Dose (TID) Test

The realized chips are tested under TID by the Cobalt-60 gamma radiation source at Helmholtz-Zentrum Berlin, Germany. Tests were performed according to TID test method specification ESCC22900 from European Space Agency (ESA). Five of each type of chips are irradiated and measured at certain interval along with a reference chip which did not go under radiation. Five of each type of boards (total 10) are mounted on a mother board which facilitates biasing all or individual at a time and makes the measurement easy. The mother board is set vertically with respect to radiation as shown in Figure 16. DC supply cables (10 m long) are brought outside the radiation room where dc sources are placed.

Figure 16: TID radiation set up of PLL and TRX boards at HZB

Electrical measurements have been performed after accumulated dose of 25 krad, 75 krad, 150 krad, 230 krad and 300 krad, taking the boards outside the radiation room. Finally, measurement have been performed after annealing of 24 hours at 25°C and annealing of 168 hours at 100°C at IHP facility. Figure 17 to Figure 20 show the measured dc current and output frequency for both types of chips. Figure 19 shows the IF output voltage for the TRX boards. No noticeable deviation in electrical performance (current, oscillation frequency, receiver gain) have been observed in the test results.

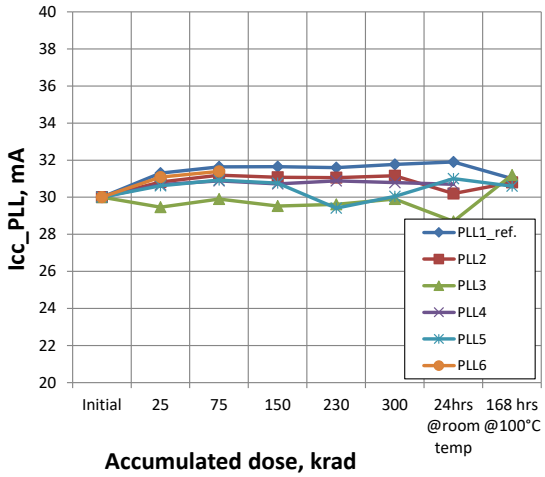

Figure 17: PLL (VCO) dc current at different accumulated dose

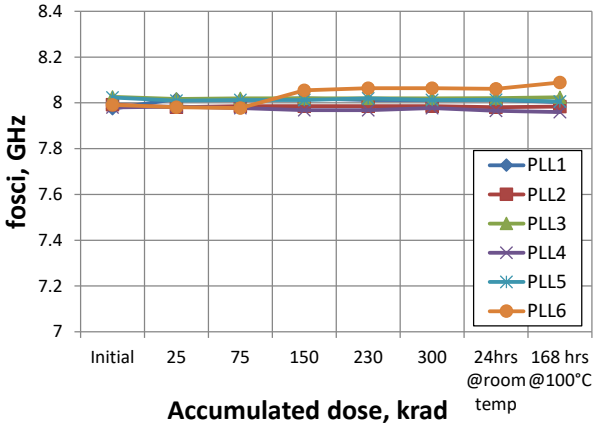

Figure 18: PLL (VCO) output frequency (Vt = 0V) at different accumulated dose

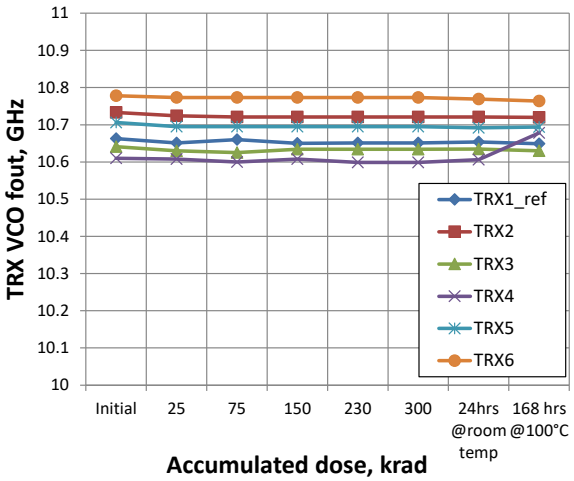

Figure 19: TRX (VCO) output frequency at different accumulated dose

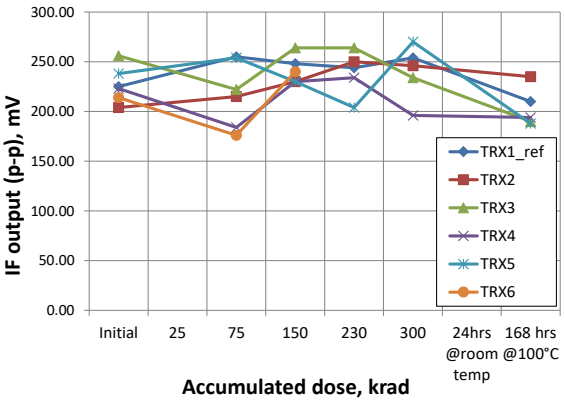

Figure 20: TRX (RX) IF output voltage at different accumulated dose

B. Single Event Effect (SEE) Test

The SEE test has been performed at CYCLONE110 facility in the Cyclone Resource Centre Louvain-la-Neuve, Belgium. For SEE test, a special PCB (daughter board) has been designed with the ability to connect with another FPGA driven motherboard for operation control and single event latch-up (SEL) detection developed by Arquimea. The daughter PCB accommodates both PLL and TRX chips but each of the chips can be powered and controlled separately. The daughter board along with the mother board is fixed inside the chamber, as shown in Figure 21. The chips can be heated up using heating element from back side and the temperature can be monitored using a Peltier module. The motherboard is connected to a laptop using communication box for controlling the test.

SEL monitoring: Each supply current on the boards is monitored and can be switched off (latch up protection), when reaching a predefined limit depending on the typical operating mode current. The SEL test is performed at higher temperature (100 - 110°C). Each latch up event is recorded in FPGA for later evaluation.

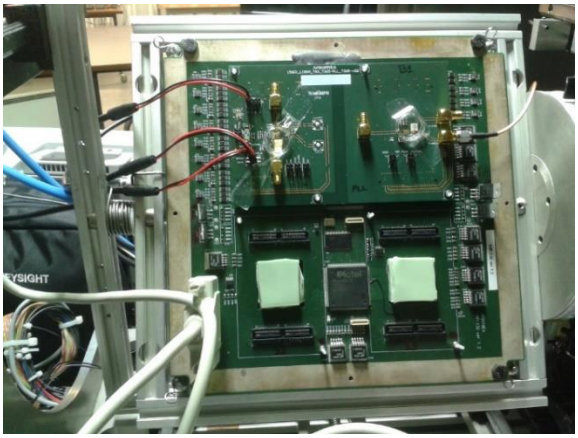

Figure 21: SEE measurement setup (inside chamber)

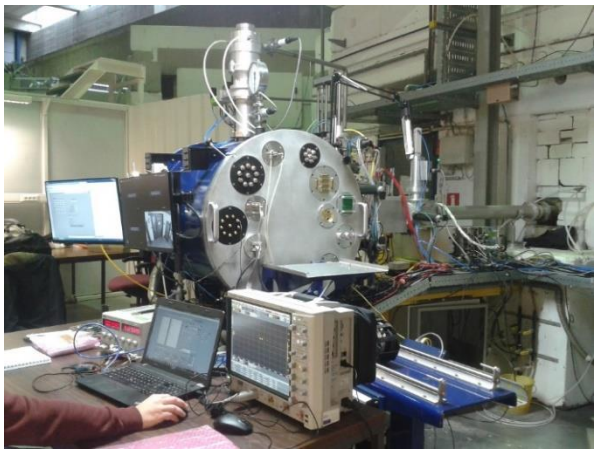

Figure 22: SEE measurement environment

Single event transient (SET) monitoring: SET data are collected with a digital oscilloscope connected to the DUT. The trigger levels are set so that the signal is always bracketed by the two levels, and the oscilloscope triggers only when a glitch drives the output outside the predefined level and a screenshot is saved. SET test is performed at minimum operating condition and at 25ºC temperature.

The SEE test has been performed on the effects of Xe ion irradiation with LET of 63 MeV·cm^2/mg. The experimental results indicate that the PLL (VCO) and TRX chips have not exhibited single event latch-up (SEL) and single event function transient (SET) sensitivity.

Two Upset (Transient) events are detected: one of DUT1_PLL and one for DUT2_PLL under the mentioned radiation and operation condition.

The number of single event transients detected in the test is also very low and those are at the very beginning of test start (within 1.50 minutes).

The PLL operation could not be tested due to limitation of providing reference input frequency and it is rather tested as VCO. This problem can be focused in future. Additionally, implementing a triggering related to frequency shift can be implemented to observe frequency variation.

V. Conclusion

X-band PLL and TRX are designed and fabricated in SiGe technology and tested under irradiation. Measurements show minimal degradation of performance of the chips, verifying the chips' robustness against radiation and hence are suitable for space applications.

VI. Acknowledgement

The chips are designed under the analogue cell development project which is a part of development of a rad-hard mixed-signal library for commercialization of space qualified ICs, "LIBRA" funded by Eurostars and ended in April 2018.

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A 10/100 Ethernet Transceiver for Space Applications

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Abstract

As space systems evolve to become more complex, they need larger computing and communication capabilities. For example, larger data rates must be supported and more flexible technologies that enable several applications to share the network resources while providing predictable and reliable performance are needed. One of the approaches to address those issues is the adoption of Ethernet in space. This has the benefit of reusing existing and field proven technology that also provides evolution to larger data rates. Ethernet is currently used in some space systems and it is being designed into many others like the next generation of Arianne launchers or NASA Orion capsule. Integrated circuits that are used in space systems need to be designed to withstand the effects of radiation that causes errors and failures. These devices known as rad-hard need to be designed and manufactured using specific techniques and processes. Therefore, for Ethernet to be adopted in space, the respective rad-hard Integrated Circuits (ICs) need to be available. The European industry is working on several such ICs including an Ethernet switch and a transceiver. European industry has enhanced and extended the standard with Time Triggered Ethernet (TTE) to provide predictable and reliable performance. In this paper, SEPHY a 10/100 Mb/s rad-hard Ethernet transceiver designed for space applications is presented.

I. SPECIFICATIONS

The SEPHY transceiver is designed to support 10 and 100 Mb/s over twisted pair cabling as specified in the IEEE 802.3i and IEEE 802.3u standards commonly known as 10BASE-T and 100BASE-TX. The device does not implement the automatic configuration features defined in Ethernet like auto-negotiation or the automatic cable crossover [1]. These features are not required since space systems are designed with a fixed configuration and a deterministic behaviour is desired. This is just the opposite of home or offices on which ease of use and the ability to add and remove devices is key. Other functional difference with commercial transceivers is that the device implements special registers to count the number of radiation errors detected in the registers and cold spare capabilities for cold redundancy. Two interfaces for communication with the Media Access Controller (MAC) are supported, the Media Independent Interface (MII) defined in the IEEE 802.3 standard and the Reduced Media Independent Interface (RMII).

In terms of radiation tolerance SEPHY is designed to withstand up to 300 krad to TID and a SEU Bit Error Ratio better than 10^{-12} at LET>70 MeV/mg/cm². This enables the use of SEPHY chip in most space missions and particularly in launchers and earth orbiting satellites [2]. A key requirement is that the device has no ITAR restriction and to achieve this Microchip 150nm SOI technology targeted to space applications is used.

II. ARCHITECTURE

The block diagram of the device is shown in Figure 1 where digital blocks are coloured in blue and analog blocks in orange. It can be seen that SEPHY chip consists of five main blocks: A MAC interface block, a 10BASE-T digital block, a 100BASE-TX digital block, an Analog Front End (AFE) and a Common Blocks.

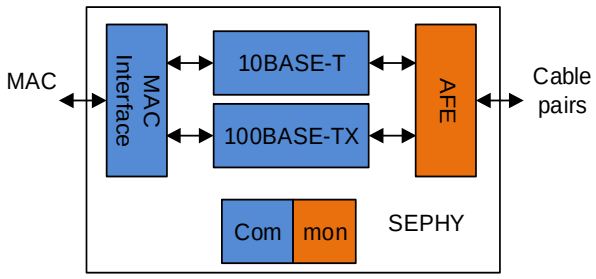

Figure 1: SEPHY block diagram

The MAC interface implements both MII and RMII at 10 and 100 Mb/s. The 10BASE-T and 100BASE-TX blocks implement the transmitters and receivers for both standards [3]. The analog front end is in charge of converting the analog signals received from the cable to digital on reception and the other way around for transmission. Finally, the common block contains both analog and digital functionality that is used in complete device providing clock, reset and the configuration/status registers.

The 10BASE-T part of SEPHY contains a Manchester encoder and a shaping filter on transmission and a Manchester decoder on reception. The device operates at 100MHz in this mode so that 10 samples are available per symbol, which facilitates the receiver implementation. In 100BASE-TX mode, the device operates a 125MHz so that only one sample is taken per symbol. The 100BASE-TX transmit path includes

a 4 to 5 bits mapping followed by a scrambler and an MLT3 encoder. The receiver for 100BASE-TX is by far the most complex block of the device and includes a programmable gain amplifier, an adaptive feedforward equalizer, clock recovery and baseline wander functions, an MLT3 decoder and a descrambler. The block diagram of the receiver is illustrated in Figure 2.

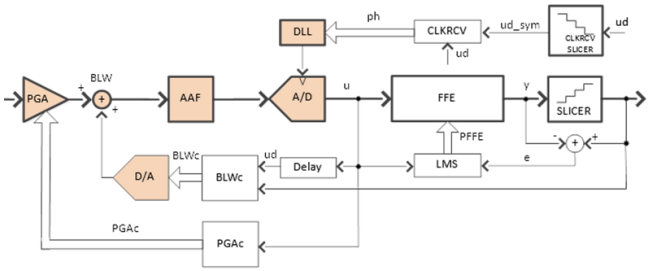

Figure 2: Block diagram of the 100BASE-TX receiver

The Analog Front End (AFE) contains a Digital to Analog Converter (DAC) and a shaping filter on transmission. On reception, it has a Programmable Gain Amplifier (PGA) to compensate cable attenuation followed by an Anti-Aliasing Filter (AAF) and an Analog to Digital Converter (ADC). A Delay Locked Loop is also used to adjust the clock of the ADC to that of the remote transmitter and a small DAC is used to compensate the Base Line Wander (BLW). These last two blocks are only needed in 100BASE-TX mode.

The common block generates the clock and reset signals for the rest of the blocks. To that end, it has a Phase Locked Loop (PLL) that can generate a 100MHz or a 125MHz clock depending on the mode selected (10BASE-T or 100BASE-TX). The common block also contains the Management Data Input Output (MDIO) interface defined in the standard to configure the transceiver and check its status.

III. TRANSCEIVER IMPLEMENTATION

The architecture described in the previous section has been implemented in Microchip´s 150 nm SOI technology targeting a 64 pin CQFP encapsulation. The device has a total area of 18.5 mm^2 and an estimated power consumption of 270 mW in 10BASE-T mode, 22% of which comes from digital section and of 635mW in 100BASE-TX mode with 70% of it coming from digital section. The digital part occupies most of the area with a total of around 80kgates. In more detail, over 75% of the area is digital and the rest is analog. On the digital part, the largest block is the adaptive equalizer that accounts for more than two thirds of the digital area. On the analog side, the largest block is the PLL. This device has been verified on simulation over PVT corners with cables lengths up to 100m and beyond as required by the standard.

IV. CONCLUSIONS

This paper has presented the first prototype of SEPHY, the first European space grade 10/100 Ethernet transceiver. The device has been manufactured with Microchip 150nm SOI Rad Hard technology (ATMX150RHA) and is designed to withstand radiation for TID levels higher than 300 krads and SEE for LET>70 MeV/mg/cm² [3] while achieving a BER better than 10^{-12}, so that it can be used in most space applications.

The die size is 4.3x4.3 mm^2. Estimated power is 270mW for 10BASE-T mode and 635mW for 100BASE-TX mode. Electrical and radiation tests on silicon are expected for September 2018. System tests will be performed in October 2018. Future work will focus on reducing the area and power of the device for the final version. This can be done by carefully dimensioning the adaptive equalizer that accounts for a significant part of area and power [4].

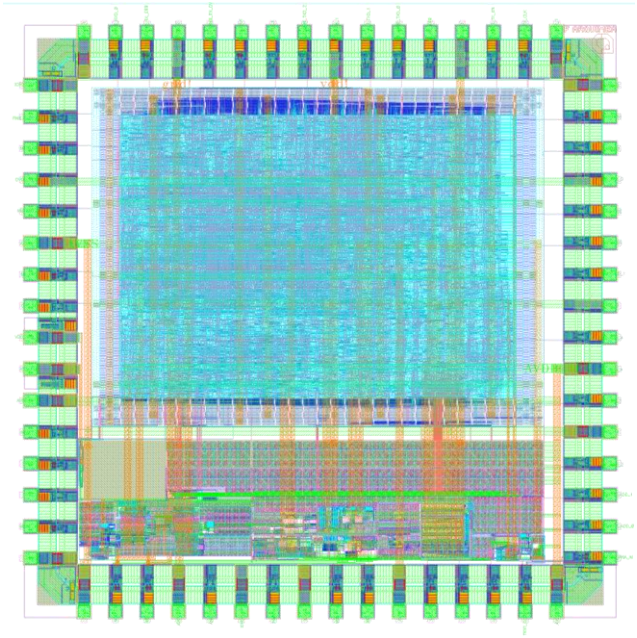

Figure 3: SEPHY die

V. ACKNOWLEDGEMENTS

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Rad-Hard Telemetry and Telecommand IC Suitable for RIU, RTU and ICU Satellite Subsystems

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Abstract

This work presents a radiation hardened integrated circuit (RHIC) that replaces with a single chip solution many of the electrical and electronic components used on satellite subsystems such as remote interface, remote terminal and instrument control units (RIU/RTU/ICU). The presented RHIC is designed to acquire the telemetries (TM) and to generate the telecommands (TC) from and for other subsystems of the satellite platform. Replacing the classical discrete implementation by this TM/TC RHIC entails volume, weight and price reduction of the RIUs/RTUs and ICUs subsystems and hence the overall satellite platform. To minimize risks and time development, several analogue IPs from the Cosmic Vision projects are reused for this development. Communications with TM/TC RHIC are by means of a redundant SPI bus. Telemetries are acquired with at least 11 effective bits' resolution from 54/27 [0; 10] V single ended / [-10; 10] V differential channels, limited in band up to 50 kHz. Telecommands allow bi-level and pulse functionalities with frequencies from 100Hz to 10MHz. TM/TC RHIC is implemented using version 5.6 of DARE180U libraries provided by IMEC and based on UMC L180 technology.

I. INTRODUCTION

A satellite spacecraft is formed by its platform (main infrastructure) and the optional payload (instruments and experiments). Its block diagram [1] is depicted in Figure 1, where AOCS stands for Altitude and Orbital Control System, CDMU for Command and Data Management Unit, OBC for On-Board Computer, PCDU/PCU for Power Control (and Distribution) Unit, P/F for Peripheral, P/L for Payload, SMU for System Management Unit, TTC for Telemetry Traffic Control and X/Ka TX for X or K_a band Transceiver.

In a satellite platform, the RIU/RTU (see Figure 2) supports the OBC/CDMU/SMU controlling other platform subsystems, such as the propulsion, the thermal control, the AOCS, etc. RIU/RTU drives the full set of actuators (valves, pyros, heaters, magnetic torquer and a wide range of platform specific devices) and collects and processes platform TM that the OBC/CDMU/SMU dispatches to ground. These functionalities require many IO interfaces implemented with a lot of electronic components. Typically, a RIU can include up to 4+4 IO interface boards, each including around 2500 electric and electronic components (see Figure 3).

In a satellite instrument, the ICU is the element that processes the incoming data and controls the other downstream elements. The interface module is one of the main functions of the ICU which acquires and monitors logic statuses and analogue TMs generating subsequent commands afterwards. Depending on the instrument needs, an ICU could require up to 2+2 IO interface boards like RIU/RTU's.

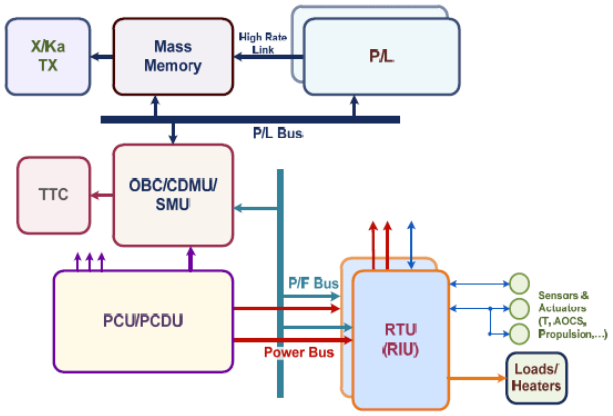
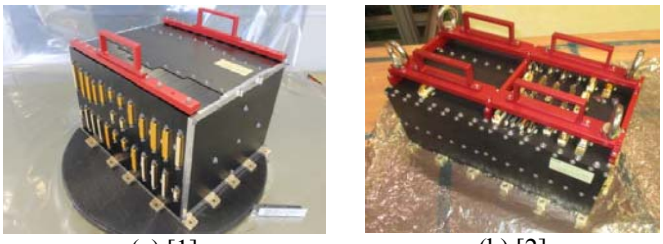


Figure 1: Block diagram of a satellite spacecraft

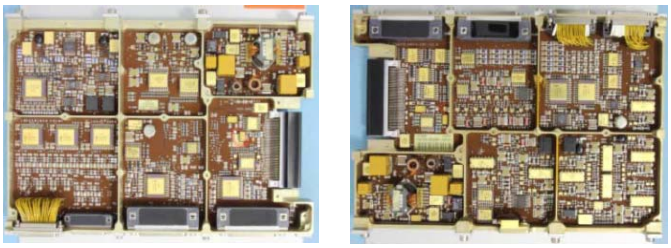
TM/TC RHIC is designed to integrate in a single component many of the electronic components used in the IO interface boards. Replacing the old implementation by the TM/TC RHIC will entail volume, weight and price reduction of RIUs/RTUs and ICUs without any functionality loss; for price, the target reduction for each of the three products is between 10 and 15%.



(a) [1] (b) [2]

Figure 2: AS1000 RIU (a) and Modular-RTU (b) photographs

The following content of the article has been organized so that: section II presents the functionality of the TM/TC RHIC and its entailed challenges; section III analyses TM/TC RHIC architecture and identifies reused IPs within; section IV locates the current development status of TM/TC RHIC within the project milestones; conclusions are compiled in section V; finally, references are collected in section VI.



(a) [1] (b) [1]

Figure 3: Photographs of RTU modules: analogue housekeeping (a) and digital IO (b)

II. DESIGN CONSIDERATIONS

A. Functionality

1) Communication interface

Due to its reliability and simplicity, a redundant SPI is the selected interface for all the communications of TM/TC RHIC. It allows multiple devices to share the same SPI bus. TM/TC RHIC configuration and information extraction (internal status and telemetries measurements) is performed by means of this communication interface. Its frequency can be in the [10; 20] MHz range.

2) Telecommands

TM/TC RHIC allows generating up to four separate telecommands at once, each being configurable independently as bi-level or as pulse. Four IO ports (one per telecommand) are reserved for this functionality, shared with the digital scan chain.

Bi-level option can be set independently but it also considers telemetries supervision comparing their converted values with registered threshold values.

Pulse option allows configuring phase, period and duty cycle, which is suitable for pulse width modulation.

3) Telemetries

TM/TC RHIC can acquire up to 27/54 differential/single-ended analogue telemetries (limited in band up to 50 kHz) that are converted to the digital domain. Telemetries acquisition sequence are configured on-chip through the SPI. Acquired telemetries are stored in a double depth table that collects first and current acquisition; this table is consulted through the SPI. Fifty-four IO ports are reserved as inputs of the telemetry channels.

Telemetry channels are grouped by pairs to handle one differential or two single-ended signals. Single-ended channels can be biased by means of an on-chip programmable current source.

Telemetries shall be acquired with a maximum absolute error of 1% for the whole [-55; 125] ºC operational temperature range. This 1% accuracy shall be independent of the resultant manufacturing process.

All the acquisitions could be configured for thermistor acquisition allowing a more flexible solution for different applications.

4) Testability

Including testability in a new development is highly recommended to optimize the development time of a successful design. Observability of key internal nets and registers is a must to confirm the expected design behaviour or for debugging. For this purpose, TM/TC RHIC includes an analogue test bus (ATB) and a digital scan chain (DSC).

ATB brings access to differential signal path nets, voltage references, bias voltages and regulated supplies. Its simplified block diagram is depicted in Figure 4. ATB can work in single-ended or differential mode, depending on the nature of the internal net required to be monitored. In single-ended mode, ATB allows monitoring two different single-ended nets at once (useful to identify cross-talk or net dependency). ATB has two access options by sharing four IO ports with telemetry channels. This implementation allows testing all the telemetry channels without sacrificing any during ATB usage. ATB allows disabling and bypassing the analogue voltage buffer at its output, which gives direct access to the selected internal net(s). ATB is configured through SPI.

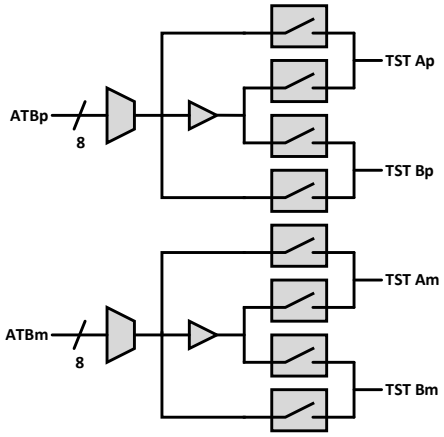


Figure 4: Block diagram of the analogue test bus

DSC brings access to the internal registers of the digital core through the four IO ports reserved for telecommands. To save IO ports, no JTAG interface was included.

B. Challenges

1) Signal ranges above maximum ratings of IO cells library

Signal ranges at system level exceed the absolute maximum rating of the DARE180U IO cells used [3]: [-0.3; 3.63] V. Single-ended signals can be up to the [0; 10] V range. Differential signals up to the [-10; 10] V range with a common-mode in the [-1; 1] V range. Differential measurements are optimized by means of an internal a common-mode control loop (see Figure 5).

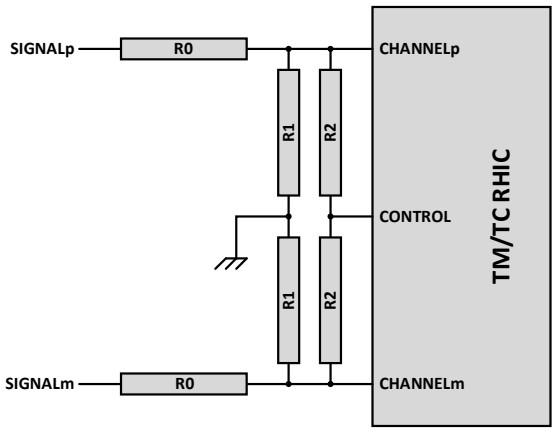


Figure 5: Differential measurement concept

2) Minimum telemetry latency

The different nature of the possible telemetries (single-ended/differential, biased or not, different voltage ranges, etc.) entails a stabilization period after channel switching. Maximum latency of a trustworthy telemetry acquisition shall be quantified and minimized. The target fastest acquisition rate is one telemetry acquisition each 10 µs.

3) Reduced number of IO ports

To have a more flexible chip with low impact in surface, a compromise of 84 IO ports has been reached considering the amount of telemetry channel inputs, telecommands, communications ports, analogue references and power supplies. Since TM/TC RHIC is an AMS design, power supplies shall be distributed among the analogue and the digital domains; this gives 2 pairs of IO ports for the analog supply, 2 pairs for the digital supply and one pair for the core supply. This latter pair is used to provide additional decoupling, since an LDO regulator is integrated on-chip to supply power to the digital core. The reduced number of IOs entailed port sharing as was previously mentioned explaining the Testability functionality.

III. ARCHITECTURE ANALYSIS

A. Block Diagram

The block diagram of TM/TC RHIC is presented in Figure 9. Each block is briefly explained below:

- B1 – LDO ANA block generates the 1.8V analogue core supply from the 3.3V external supply.
- B3 – LDO DIG block generates the 1.8V digital core supply from the 3.3V external supply.
- B4 – SENSOR BIASING block provides the bias capability of the telemetry channels.
- B6.1 – MUX block selects the telemetry channels to be acquired.
- B6.2 – SIGNAL CONDITIONNING block fits the signal coming from the telemetry channels for the ΔΣ modulator input.
- B6.3 – LSSB MODULATOR block (ΔΣ modulator) is the first stage of the digital conversion of the acquired telemetry.
- B6.4 – DIGITAL FILTER block filters and decimates the 1-bit output of the ΔΣ modulator to obtain the final resolution.
- B6.5 – OUTPUT DATA BUFFER block records the acquired telemetries
- B7 – STATUS COMPARATOR compares the acquired telemetries with a registered threshold level.
- B8.1 – V REF block generates the internal voltage references for the ΔΣ modulator.
- B8.2 – I REF block generates the internal current references for the rest of the analogue core blocks.
- B9.1 – MAIN REF provides a stable voltage reference for other blocks of the analogue core. This reference can be provided either by the internal bandgap reference or externally.
- B9.2 – INT REF block generates the bias voltage for external attenuators based on resistive networks.
- B10 – V SUPERVISOR block is a window comparator (acquired telemetry versus registered threshold levels) implemented digitally.
- B11 – RESET MANAGEMENT block generates the internal reset signal for TM/TC RHIC.
- B12 – REFERENCE REG block is a register bank. It records the threshold levels.
- B13 – PWM GEN block implement the PWM functionality of telecommands.
- B14 – STA REG block is a register bank. It stores the status of TM/TC RHIC.
- B15 – ADC REG block is a register bank. It stores the configurations for the digital conversions of the telemetries.
- B16 – ADC TIMING CONTROLLER block manages the timing configurations of the digital conversions of the telemetries.
- B17 – MISC REG block is a register bank. It stores additional registers not considered in the other register banks.
- B18 – SPI/SSB block implements the communication interfaces.
- B19 – COMMAND block drives the telecommands using the information stored in other blocks.

B. Reused IPs

The reuse of silicon proven IPs saves development time of new IC designs and mitigates their risks. In the frame of Cosmic Vision projects [4], several IPs based in UMC L180 technology were developed to be reused in subsequent IC designs for space applications. Four of these IPs were initially selected for the TM/TC RHIC project: two type of regulators, a bandgap reference and a ΔΣ modulator. These IPs cover respectively the functionality of B1, B3, B9.1 (partially) and B6.3 blocks. The following sub-subsections present the electric and radiation performances of the reused IPs.

1) Regulator type 1

This IP was designed to supply power to analogue circuitry that require continuous bias. Its electric and radiation performances are compiled in Table 1 and Figure 6.

Table 1: Electric and radiation performances of the regulator type 1

Parameter	Value	Units
Supply voltage	3.3	V
Reference voltage	1.25	V
Regulated output voltage	1.8	V
Maximum output current	60	mA
TID / LDR	505 / 310	krad(Si) / rad(Si)/h
SEL LET_{th}	> 72	MeV·cm²/mg
SET LET_{th} (Weibull fit)	20	MeV·cm²/mg
SET XS (Weibull fit)	6.4E-9	cm²/device

Additional checks were performed to verify that regulator type 1 performance is not affected by the operational frequency of the DC/DC converter that provides the 3.3V supply at system level. It was concluded that regulator type 1 is reusable for TM/TC RHIC.

2) Regulator type 2

This IP was designed to supply power to switched capacitors or digital circuitries. Its electric and radiation performances are compiled in Table 2 and Figure 7.

Table 2: Electric and radiation performances of the regulator type 2

Parameter	Value	Units
Supply voltage	3.3	V
Reference voltage	1.25	V
Regulated output voltage	1.8	V
Maximum output current	30	mA
SEL LET_{th}	> 72	MeV·cm²/mg
SET LET_{th} (Weibull fit)	3	MeV·cm²/mg
SET XS (Weibull fit)	1.2E-6	cm²/device

In the same way as for regulator type 1, additional checks were performed to verify that regulator type 2 performance is not affected by the operational frequency of the system's DC/DC converter. The reuse of regulator type 2 for TM/TC RHIC is under discussion due to its weaker radiation performances compared to regulator type 1's.

3) Bandgap reference

This IP was designed to provide the voltage reference for regulators type 1 and 2. Its electric and radiation performances are compiled in Table 3 and Figure 8.

Table 3: Electric and radiation performances of bandgap reference IP

Parameter	Value	Units
Power supply	1.8	V
Output voltage	1.25	V
TID	505	krad(Si)
SEL LET_{th}	> 72	MeV·cm²/mg
SET LET_{th} (Weibull fit)	27	MeV·cm²/mg
SET XS (Weibull fit)	1.5E-9	cm²/device

Additional checks were performed to verify that the bandgap reference is accurate enough to meet top level requirements. It was concluded that the bandgap reference needs slight enhancements to be reused for TM/TC RHIC.

4) Delta-Sigma modulator

Delta-sigma data converters are prone for space applications [5] [6] [7]. From a space application point of view, their oversampling can be seeing as a multi-vote spread in time that filters SEE at the cost of increasing system noise.

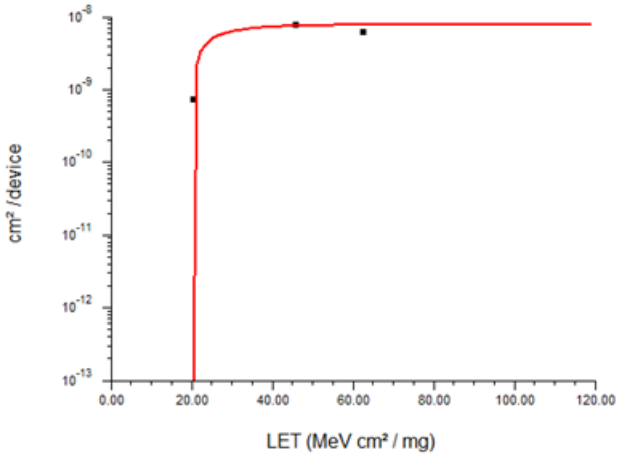


Figure 6: SET Weibull curve of regulator type 1

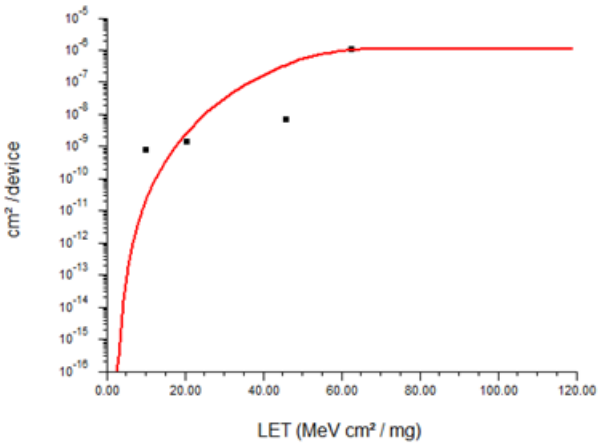


Figure 7: SET Weibull curve of regulator type 2

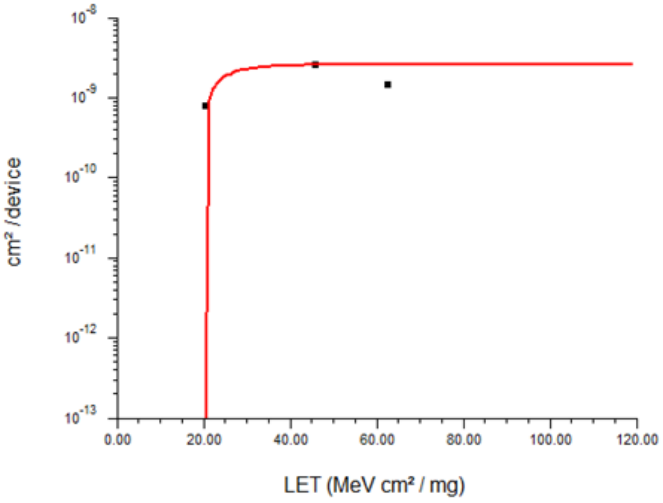


Figure 8: SET Weibull curve of bandgap reference IP

The ΔΣ modulator IP was designed to provide a 16 ENOB 1-bit output data stream inside 50 kHz Nyquist bandwidth with a 13.6 MHz sampling clock. Additional checks were performed to verify that the IP could operate for different sampling frequencies (up to 15 MHz) without degradation below 11 ENOB. It was concluded that the ΔΣ modulator is

reusable for TM/TC RHIC. Its electric and radiation performances are compiled in Table 4 and Figure 7.

Table 4: Electric and radiation performances of ΔΣ modulator IP

Parameter	Value	Units
ENOB	16	effective bits
Nyquist Bandwidth	50	kHz
SEL LET_{th}	> 72	MeV·cm²/mg

5) *Digital IPs*

Almost all the digital core of TM/TC RHIC is composed by digital IPs already implemented in FPGA. The [10; 20] MHz system clock frequency should not entail complications for the implementation of these IPs with DARE180U libraries.

IV. Project Overview

The TM/TC RHIC project aims to provide a TRL 5 design after two manufacturing runs. The project is currently finishing its architectural design phase. Validations results for the prototype are planned for the end of 2019. Qualification of the final chip is planned for the end of the first trimester of 2021.

V. Conclusions

This work presents a telemetry and telecommand rad-hard chip that aims to be a recurrent part inside the Airbus group. Its usage will entail weight, volume and price reduction of RIU/RTU and ICU satellite subsystems. Regarding price, the target reduction for each of the three products is between 10 and 15%. To mitigate risks and reduce time development, the following analogue and AMS IPs based in the same technology (UMC L180) were selected to compose the chip: two type of regulators, a bandgap reference and a ΔΣ modulator. The suitability of each IP was confirmed with additional checks.

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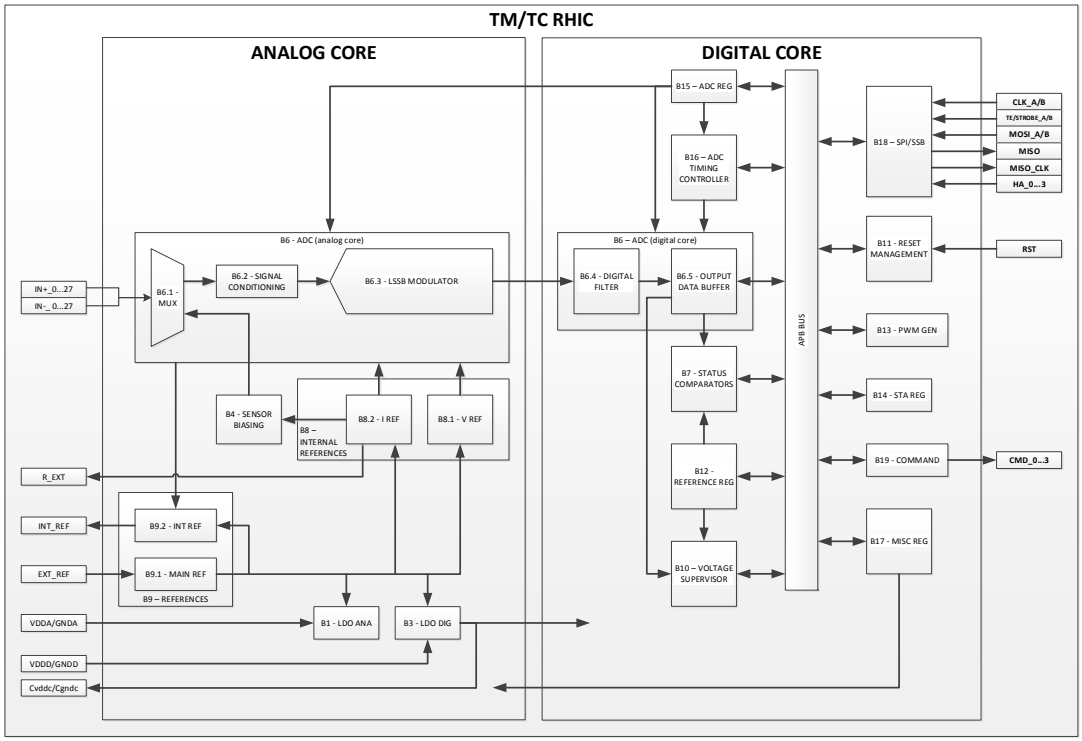

Figure 9: Block diagram of TM/TC RHIC

Atom-Switch FPGA for IoT Sensing System Application

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Abstract

We have developed an atom-switch based field programmable gate array (FPGA) with radiation resistance. The atom switch replaces both configuration RAM and pass transistor, resulting in reducing chip size and enhancing energy efficiency. Atom switch features non-volatility, high on/off conductance ratio, and rewritability. Since the atom switch also has a durability against radiation, the circuit configuration of FPGA is protected.

I. INTRODUCTION

The Internet of Things (IoT) has been envisioned as a fundamental infrastructure that will bring about useful information and knowledge resulting in efficiency and growth in industry and improved comfort and safety in human life. Sensors, networks, and information technology (IT) are designated as key technology elements to make IoT a practical knowledge framework. IoT is to be used for supporting so-called lifeline as energy supply, water works, traffic control, logistics, broadcasting, and telecommunication. Everything is to be connected through Machine to Machine (M2M) network anytime and anywhere to realize the IoT framework [1].

Space systems, such as satellites, can be identified as sensor nodes and relay nodes among IoT applications [2]. It is integrated with ground systems, and wide range of collected information must be transmitted through the limited transmission capacity of existing network. Thus, it is essential to reduce the data size by computationally intensive algorithms including data compression, data prediction, adaptive sampling, and so on. Field programmable gate arrays (FPGAs) with high performance computation are suitable for this purpose. Especially, a single-event-effect (SEE) free FPGA is the most desirable device because the demanding characteristics on satellites is a continuous operation in harsh environment with background radiation in orbit. Low power consumption is another demanding characteristics for realizing less heat dissipation indispensable to space applications operating in exoatmosphere.

In this contribution, an atom-switch based FPGA with radiation resistance is discussed. Atom switch provides rewritable capability for FPGAs without static random access memory (SRAM) or electrically erasable programmable read-only memory (EEPROM) to store circuit configurations. The atom switch functions as routing switch and memory bit in look-up table (LUT). The atom switch has a durability against radiation. This results in mitigating SEE in circuit configuration of FPGA. Memory patrol and memory scrubbing functions are not required for the atom-switch FPGA, and that eliminates external peripheral devices used with conventional rewritable FPGAs. We demonstrate the improved performance of atom switch FPGA, compared to the conventional SRAM based FPGA fabricated in same technology node of 40 nm.

II. COMPLEMENTARY ATOM SWITCH

Atom switch is a resistance-change switch with high on/off conductance ratio [3, 4]. The switch is composed of the polymer solid electrolyte (PSE) sandwiched between Ru and Cu electrodes (Fig. 1(a)) [5]. When a positive voltage is applied to the Cu electrode, Cu is ionized and precipitated at the Ru electrode, and then a Cu metal bridge is formed between the Cu and Ru electrodes. The conductance of the switch changes to high (or on state). When a positive voltage is applied to the Ru electrode, the metal bridge is broken and dissolved into the solid electrolyte and the switch turns off. The programming cycles is up to 1,000. The on or off conductance is maintained even when the voltage bias is not applied. Atom switch is implemented between metals 4 and 5 by using the conventional backend-of-line (BEOL) process (Fig, 1(b)).

Only two photo masks are needed to fabricate the atom switch in BEOL. One of the masks is for opening the cover of Metal 4 and the other for etching the switch stack. The Cu line edge is used for the electrode of the atom switch. Thus, the Cu metal bridge in the PSE is induced at the edge of the Cu electrode, resulting in the improved on-state reliability. The

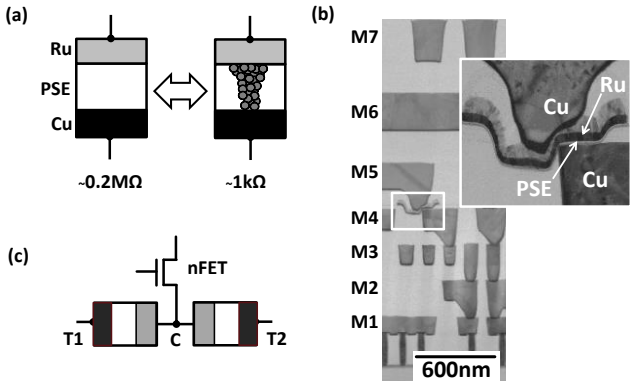


Figure 1: Atom switch. (a) Operation principle of atom switch. (b) Transmission electron microscopy of atom switch embedded into Cu interconnects of 40-nm node CMOS. (c) Complementary atom switch (CAS) for programmable switch in FPGA.

Ru alloy is used for the inert electrode of the atom switch, instead of simple Ru. The Ru alloy further improves the on-state reliability, compared to Ru. Highly reliable on-state is obtained by optimizing the electrode material and structure [6].

The off-state reliability is enhanced by connecting two atom switches in an opposite direction (Fig. 1(c)), which is named by complementary atom switch (CAS) [7]. Both elements are programmed to be on or off state by applying a voltage between terminals T1 and C, and T2 and C, sequentially. The current during the programming is regulated by n-type transistor connected to the terminal C, so as to control the on conductance. During the logic operation of FPGA, logic signal passes through between T1 and T2. For an off state, both elements are programmed to be off. For off-state reliability, the time-to-on should be more than 10 years, while the switch is under stress of the operating voltage (V_{DD}). However, there is a trade-off between high off-state reliability and low programming voltage (V_P). Atom switch with a thick solid electrolyte has a high off-state reliability but a high V_P. Use of high-voltage-tolerant transistor results in a large circuit size. The two-terminal atom switch with a higher V_P needs a 3.3-V-tolerant transistor for programming [8]. When the CAS is applied to the programmable switch, both high off-state reliability and low V_P are realized. A 1.8-V-tolerant transistor or even logic transistor with small foot print are used.

III. Circuit Architecture and Performance Evaluation

This section describes the circuit architecture and the performance evaluation of atom-switch based FPGA [9, 10]. Atom-switch based FPGA is composed of array of configurable logic block (CLB), Input-output cell, and programming drivers for atom switch. The CLB array includes the routing tracks with 4 segment length in all 4 directions (vertical or horizontal direction) (Fig. 2(a)). The logic signal from any CLB can reach CLBs within 4 units away in either direction without passing CAS. Each track has 4 lanes (Fig. 2(b)) and totally 16 lanes are available for one direction. Since the tracks are unidirectional, the tracks for positive and negative directions are provided. This contributes to the routability and the reduction in the signal delay. The segment wires are buffered by AND gate at the section between the second and third CLBs. The AND gate also terminates unused wires to reduce the parasitic wire capacitance. The segment length and the lane number are chosen to have the capability of routing all of the MCNC20 benchmark circuits [11].

Figure 3 shows a schematic diagram of CLB. The CLB has 64 inputs and 16 outputs from/to the neighbouring CLBs. The main parts of CLB are a basic logic element (BLE), buffers and a crossbar. The BLE is composed of a pair of 4-input LUT and D-type flip-flop (DFF). The DFF has control inputs for asynchronous set and reset (RB/SB). We found that the cluster size of 4 is optimum in terms of the logic density and the signal delay. The crossbar circuit plays as multiplexers for signals. The CAS is placed at each cross point of the crossbar circuit. The crossbar has the half-depopulated CASs for routing the input (IN) and the fully

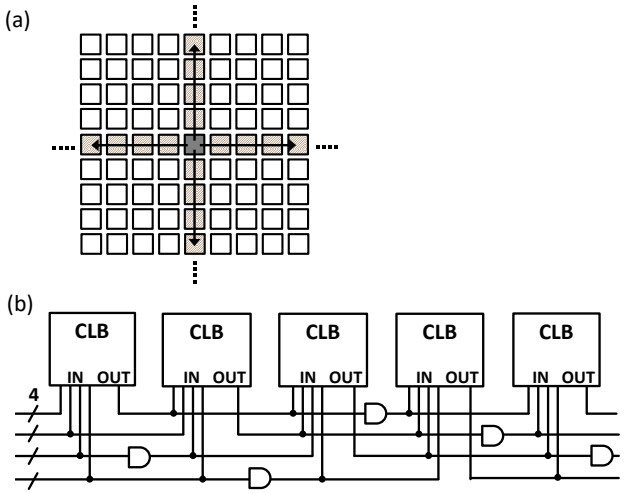


Figure 2: Routing architecture of atom-switch based FPGA. (a) Array of configurable logic blocks (CLBs) and routing path from CLB. (b) 16 routing tracks at right direction. Each track spreads 4 segments.

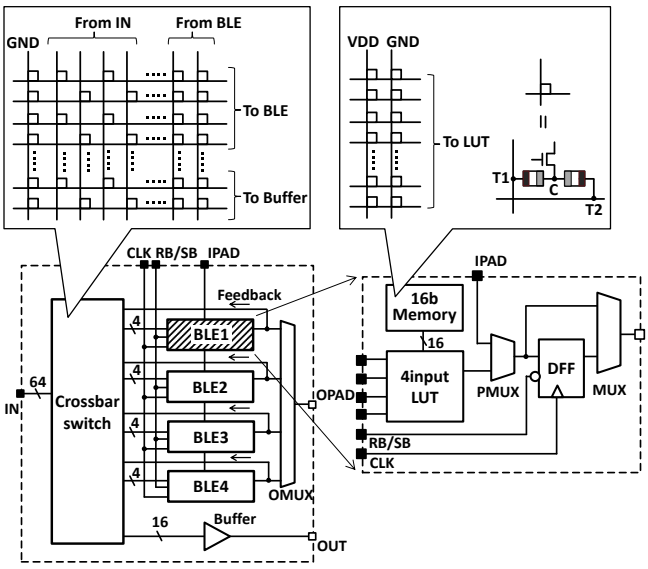
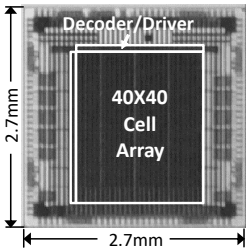


Figure 3: Configuration logic block (CLB) architecture. CLB composed of crossbar switch and four basic logic elements (BLEs) has 64 input (IN) and 16 output (OUT) for signal routing, Each BLE has 4 input look up table (LUT) and D-flip flop (DFF).

populated CAS for feedback lines from BLE. We evaluate the depopulation rate and it is found that MCNC20 benchmark circuit is successfully mapped on CLB arrays with depopulation rate of more than 50%. Programming circuitry of the crossbar is studied elsewhere [9]. The crossbar has 69 inputs, comprising of 64 routing tracks, 4 feedback lines, and the one fixed-low line preventing floating node. The number of outputs are 32, comprising of 16 LUT input and 16 outputs of CLB via buffers. Note that the small input capacitance of CAS (~0.14fF) enables us to design such a large scale crossbar circuits. Additionally, the single stage routing is beneficial to reduce the signal delay.

CAS is also utilized in memory bit of LUT (Fig. 3). The LUT memory outputs either V_{DD} or GND by programming either of two CASs (Fig. 3). Hence, the circuit configuration



Technology node	40 nm 1P7M
Chip size	2.7 ×2.7 mm^2
LUT count	6.4k
Atom switch count	4.38 Mbit
PLL	1
GPIO	128

Figure 4: Die photo of atom-switch FPGA with 40x40 CLB and its specifications.

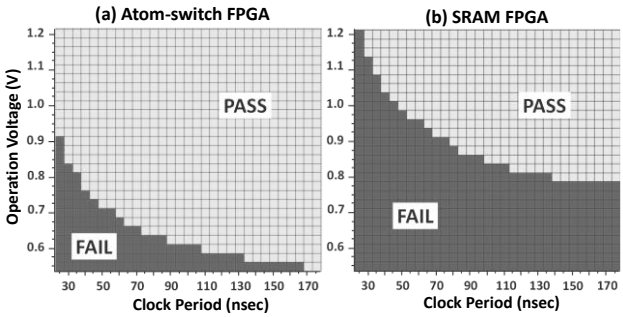


Figure 5: Operation regions of (a) atom-switch FPGA and (b) SRAM FPGA. 16b-alithmatic logic unit and signal generator are mapped on both FPGAs.

maintains even when the power is turned off, and the external non-volatile memory is not required.

Figure 4 (c) shows die photograph of the test chip fabricated by using 1-poly-7-metal 40-nm CMOS process. The size of test chip is 2.7 mm x 2.7 mm and the 40 x 40 CLB arrays are integrated. The 4.38-Mb atom switches are integrated between metals 4 and 5 of Cu interconnect.

We compared the performance of the atom-switch FPGA with the commercial SRAM-based FPGA, fabricated by 40-nm CMOS process [12]. The logic density of the atom switch FPGA is 2 times larger than that of the reference chip. The benchmark circuit of 16-bit Arithmetic Logic Unit (ALU) with a 1k-gate scale was mapped on both FPGAs. The test circuit includes an instruction decoder and input signal generator. 332 LUTs and 73 FFs are used. A count-up signal generated by a mapped 16-bit counter is the input as the operand of ALU. All 28 instructions are cyclically asserted using a one-hot signal generator. The configuration data from arbitrary RTL description were generated by in-house cluster packing and placement/routing tool chain [9]. First, gate level netlist was obtained by logic synthesis. Then, logics were converted into 4 input LUT, and placement and routing were employed to get configuration data. The configuration was done by setting the designated atom switches to the on-state in each cell. The verification pattern was generated from the Verilog test bench, and both devices were evaluated using a logic tester.

Figure 5 shows 2-dimensional shmoo plots in terms of clock period and operation voltage, V_{DD}. The ALU mapped on the atom switch FPGA operated at 3.8 times faster clock frequency when V_{DD} = 0.8 V, compared to that on the state-of-the-art low power FPGA. The novel FPGA also operated down to V_{DD} as low as 0.55 V and the commercial FPGA as low as 0.

The power consumption was compared at the minimum V_{DD} for 15-MHz operation. The atom-switch FPGA operated at 0.73 V and 15 MHz with the active power of 386 µW. Contrarily, the minimum V_{DD} of the reference chip for 15-MHz operation was 0.94 V, and the active power 630 µW. The dynamic power of the programmable logic cell arrays (= 13 µW/MHz) was also lower than that of the reference (= 39.5 µW/MHz). These improvements are mainly originated from the small capacitance in the programmable switch and reduced wire length.

IV. Radiation Resistance

Radiation resistance of atom switch was evaluated by using a heavy ion cocktail beam. For this evaluation, array of 128k-bit atom switches was used. The array of atom switches was exposed by Xe and Kr ions. Linear energy transfers (LETs) of Xe and Kr were estimated to be 68.9 and 40.3 MeV/(mg/cm^2) at the chip surface, respectively. During the irradiation, we observed no SEE, showing that SEE cross section is at least 100 times lower than that of NAND flash.

In FY2018, the atom-switch FPGA will be evaluated in orbit via the innovative satellite technology demonstration program [13]. The program is conducted by Japan Aerospace Exploration Agency (JAXA). During a whole year, the full-HD image will be compressed in the atom switch FPGA and transmitted to ground stations.

Table 1: Radiation Specifications

Items	Details
Radiation source	Cf-252 fission fragments
Test bit	128k
Fluences [p/cm^2]	1.25×10^{7}
Active area [cm^2]	1.5×10^{-11}

V. Summary

A low-power non-volatile FPGA is demonstrated for energy-constrained applications in space system. FPGA composed of a 4.38-Mbit atom switch for the routing switch and configuration memory shows a 2x logic density, 3.8x operation speed, and 3x power efficient FPGA, compared to the conventional SRAM based FPGA with same technology node of 40 nm. The developed atom switch FPGA is a strong candidate for energy efficient computing in space system.

VI. Acknowledge

A part of this work was supported by NEDO. A part of the device processing was performed by AIST, Japan. The authors acknowledge Dr. K. Takeuchi of JAXA for evaluating the resistance against radiation.

VII. References

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Radiation Hardened Pulse Width Modulator in CMOS-SOI

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Abstract

The aim of this project is to provide Pulse Width Modulator controller (PWM) solution that will largely simplify Electronic Power Conditioners (EPC) design due to variety of converter topologies that can be realized within one chip and decrease its cost due to integration of more converter elements in one chip. Field of application of this PWM controller can be far greater than EPCs only, ranging from platform to payload units. It can be used in various topologies (Buck, Boost, Buck-Boost, Push-Pull, Flyback and Forward converters) and their synchronous variations. Commonly used regulation control loop is available (voltage mode and current mode).The Pulse Width Modulator ASIC operates with clock signal (externally or internally generated) ranging from 100 kHz to 1 MHz

The pulse width modulator is implemented in a rad-tolerant 150nm CMOS-SOI process. The ASIC has been radiation-hardened by design techniques (including Triple-Modular-Redundancy, SET filtering, periodic reset with no operation interruption).

I. Introduction

This paper presents a PWM ASIC for use in aerospace environment. Its characteristics make this PWM easily adapted to various DC/DC topologies. This ASIC operates with a single power supply voltage, ranging from 8V to 16V. The power supply of the output stage (VDD and GND) is totally independent from the rest of the ASIC's power supply to avoid any large core supply variations. It has the flexibility to generate its own clock signal or operate with an external clock signal with frequencies from 100 KHz up to 1 MHz. The PWM ASIC can drive other PWM ASICs in phase or shifted and/or with scaled down frequency. The pulses of the two PWM command outputs can have adjustable characteristics. The Leading edge blanking, the minimum duty cycle, the maximum duty cycle and the slope of the ramp signal can be externally adjusted. Also the output logic allows various configurations (opposite, alternated, complementary or one channel only). For the start up sequence an external capacitor can be added to achieve soft-start and avoid high inrush currents.

II. PWM Architecture

The PWM consists of 4 main high level blocks. The clock generation block where the clock generation and manipulation take place (phase shifting, prescaling and frequency division). The Power Supply Interface consists of the regulator and the Under Voltage Lock Out (UVLO) circuits which inhibit the ASIC when the power supply voltage is lower than the set threshold (9V). The output buffer block includes the buffers needed to drive large capacitive loads (power transistors). The rest circuits consists the PWM module containing one independent voltage reference, voltage sensing, regulation and comparison in an analogue voltage control loop, PWM signal generation by comparison with a trimmable compensation ramp, leading edge blanking and minimum duty cycle operation, over current protection and outputs logic allowing various configurations (opposite, alternate, one channel only and complementary outputs).

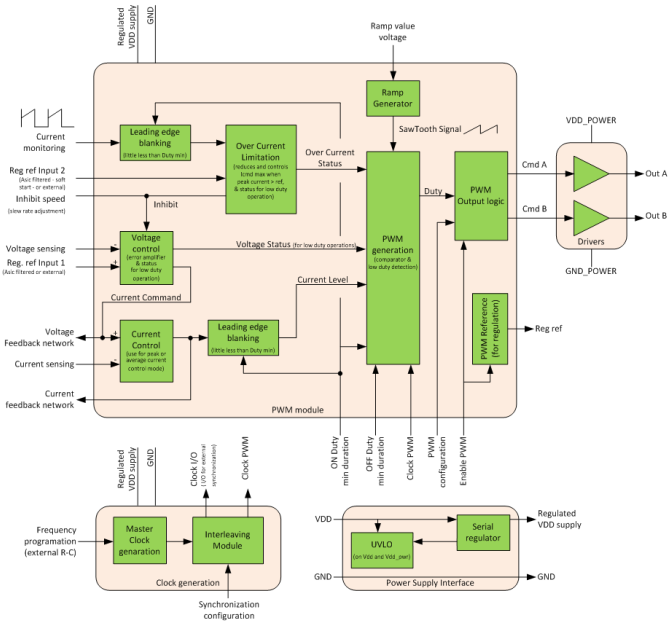

Figure 1: MISAC PWM controller high level block diagram.

A. Clock generation module

The clock generation module provides to the PWM module an adjustable fundamental clock from 100 kHz to 1MHz. Depending on the role of the chip (independent, master or slave) it can feed the ASIC with an external clock (slave) or it can provide, from its internal oscillator, any clock frequency ranging from 100 kHz to 1MHz. This clock can be feed to other ASIC via an external pin (master).

The clock generation module can phase shift the clock, internally or externally provided, by 90°, 180° or 270°. Can

also perform frequency division by two, by four or by eight times. The last stage of this module is controlled by the PWM module and it divides the frequency up to 32 times when an overcurrent event is detected.

The oscillator's frequency, the phase shifting and the frequency division are controlled by external passive components.

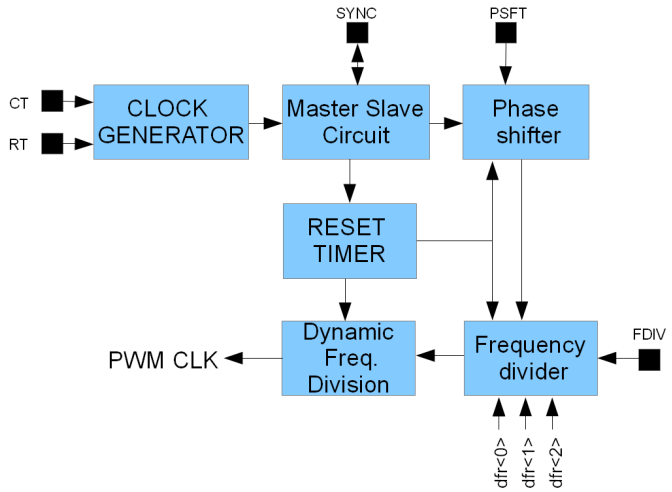

Figure 2: Clock generation module

B. *Power supply module*

This module contains a regulator a Bandgap and the UVLO circuits. The reference voltage generated by the Bandgap can be distributed to the PCB via an external pin and can source up to 10 mA current. The regulator supplies the ASIC with 3.3 V, expect the power module, using an external decoupling capacitor. The UVLO circuits inhibit the ASIC in any case where the power supply falls below 9V or the internal regulated supply falls below 2.65V. The ASIC operation is resumed when the power supply and the regulated supply go above the mentioned threshold values with adequate hysteresis (500mV and 350mV respectively).

C. *Output buffer module*

This block contains the output buffers which are responsible for driving large capacitive loads (power transistors). The buffers are able to source/sink peak currents up to 2 A. These buffers are composed with high voltage transistors (16V) and have a level shifter circuit from 3.3V, for the input signal from the PWM module, to power supply's voltage (up to 16V). Their supply is separate and independent from the rest ASIC's supply.

D. *PWM module*

The principle operation of the PWM module is depicted in Figure 3. The monitored voltage is feed through the compensation network (voltage or current controlled) and then the Leading Edge Blanking (LEB) signal is added to the incoming pulse to blank any switching noise. Then a comparison takes place with an internal generated sawtooth signal and the outcome is the preliminary duty cycle. The Low duty logic compares the preliminary duty cycle with the minimum ON duty cycle and if the preceding is smaller in duration than the latter then a Low duty flag is issued and the minimum ON duty cycle is applied. If the voltage status is triggered by an overvoltage event the Zero duty flag is issued and no pulses are generated until the output voltage is reduced to the nominal value. The overcurrent status is triggered when the voltage across the sensing resistor is exceeds 1V [3]. The Low Duty Logic starts to send the appropriate signals (dfr<0:2>) to the clock generation module in order to sequentially reduce the PWM clock frequency by 2 and up to 32 times. When the overcurrent status is deactivated the frequency of the PWM clock is sequentially restored.

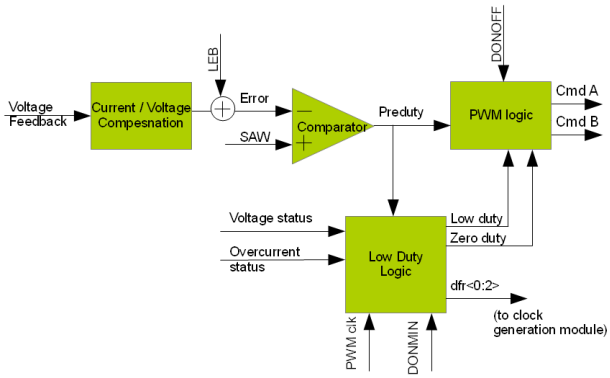

Figure 3: PWM basic block diagram

The PWM logic block is responsible for generating the proper pulse-width modulated waveform to be sent to the output buffer module. It has four configuration modes (opposite, alternate, one channel only and complementary outputs) depending the external circuitry attached to the PWM. The two output channels are not both active at the same time by applying adequate dead time between the two command signals. The maximum ON duty cycle is limited by an external signal (DONMIN).

The minimum ON duty cycle, the overvoltage threshold, the maximum ON time and the sawtooth ramp's slope can be configured by external passive components.

III. LAYOUT

The top half part of the chip (high voltage side) is populated only with circuits, pads and power supplies associated with the two separate output buffers. On the bottom half all the 3.3V circuits are situated

The chip dimensions are 3857μm by 5092μm.

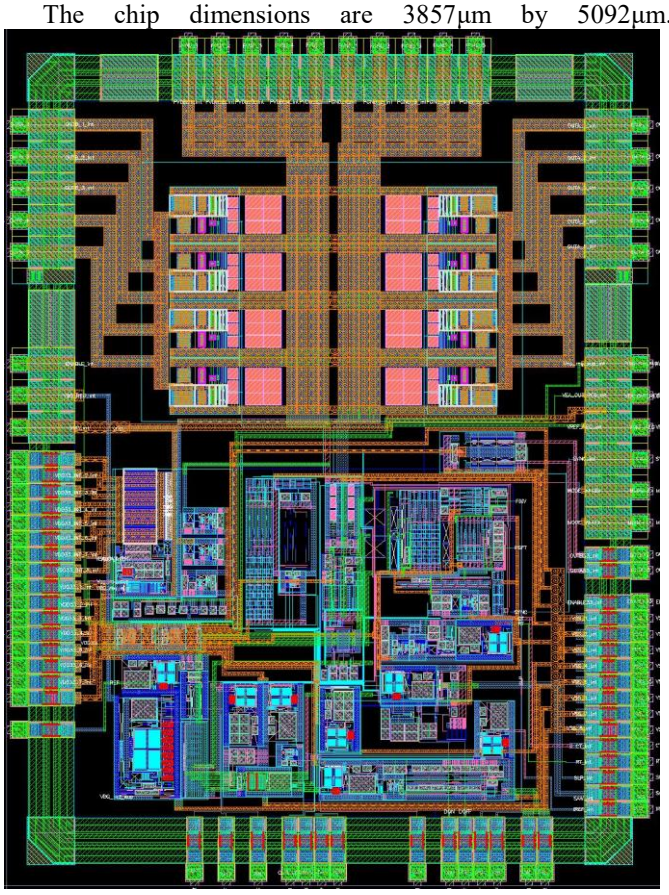

Figure 4: Layout view of the complete design

IV. Radiation Hardening

The ADC is implemented on a 150nm, single-poly, 5-metal, 0.15μm SOI CMOS radiation tolerant process of Microchip (ATMX150RHA). For every digital block Triple Modular Redundancy (TMR) is used to provide protection against Single Event Upsets (SEU). The analogue part is hardened using relaxed layout rules, guard rings and use of enclosed layout NMOS transistors. On every critical node, capacitors have been placed to filter any SET event. On all DFFs a periodic reset is applied to return all the SEU affected registers to normal operation without interrupting the PWM's operation.

V. Performance characteristics

This PWM can operate with switching frequencies from 100 kHz to 1MHz. The output buffers can source or sink peak currents of 2 A. The power dissipation is 10W when operating at 1MHz with maximum load. The design is targeting to achieve a dose tolerance up to 100 Krad and be latch-up insensitive for LET up to 60 MeV.

The project is at the manufacturing phase with the first samples expecting to arrive during summer 2018.

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A Radhard LVDS Chip: Transistor Level Design Aspects

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Abstract

This paper presents several design aspects as implemented in a radhard space-grade LVDS dual transceiver chip. The issues are discussed down to transistor level. Both the LVDS transmitter (driver) and the LVDS receiver are covered. As the chip is intended for space applications, several extra features are required on top of a direct implementation of the LVDS standard. A standard 180 nm mixed mode CMOS technology is used. Supply voltage is 3.3 V. The chip is designed within imec's DARE180U design ecosystem, benefitting from all available tools and know how.

I. Introduction

LVDS (Low Voltage Differential Signalling) digital links are used for die to die to system to system communication, due to its high immunity to common mode disturbances, high speed and low power consumption. LVDS electrical behavior is standardised in [1]. For application in space, robustness is to be maximised, and hence some extra requirements are necessary: receiver to have an extended common mode input range (ECM), and to be fail safe, a high level of ESD protection, cold spare compatibility, 5 V tolerance of LVTTL inputs, radiation tolerance (both TID, SET and SEL), just to list the most important ones. Off-the-shelf components are available, from several manufacturers. These include several space-grade versions. However, several years ago none of these were European made (actually most were US, and hence were subject to ITAR regulation, amongst others). For this reason, ESA (the European Space Agency) initiated the development of several space-grade LVDS components (being to some extend compatible with existing material), [2]; we will discuss a dual transceiver (dual LVDS to LVTTL, dual LVTTL to LVDS; see Figure 1) in this paper, but the issues apply to other components as well. An extra requirement: the design should not infringe on existing patents. Note that an important application of the dual transceiver is to apply to one SpaceWire port, [3].

The key features of this design are listed in Table 1.

Our aim was to use a standard available CMOS technology (for reasons of design and process cost, process quality, availability and life time of the process). A 180 nm technology as available through Europractice [4] was chosen. More specifically, UMC's L180 MM/RF 1.8V/3.3V, Single Poly Six Metal (1P6M), PSub/Triple-Well CMOS technology is used. This process is also used by imec for the DARE (Design Against Radiation Effects) design ecosystem and the corresponding DARE180U library, from which we hence benefited a lot. Note that the chip only uses the technology's 3.3 V IO (or "high voltage") transistors (no 1.8 V transistor is used).

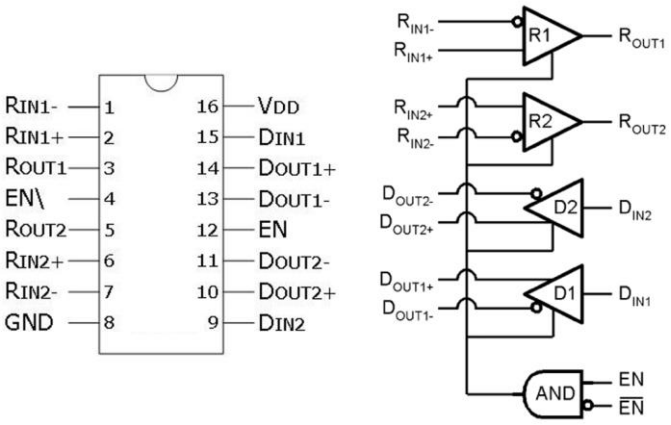

Figure 1: LVDS dual transceiver chip

II. LVDS Standard Requirements

This chapter discusses issues directly following from the LVDS standard.

A. Transmitter Common Mode Regulation

The transmitter output is a differential signal, and the cell also has to set the common mode voltage of the signal, using a common mode regulation (or feedback) circuit. For this the common mode of the two outputs is somehow required. In the DARE180U standard cell (amongst others) this is done by putting a 1 kΩ (on-chip) resistor between the two outputs; the midpoint then is the common mode voltage, and this node is regulated to be equal to the anticipated common mode voltage (in this case 1.25 V, [1]).

The drawback is the 1 kΩ (on-chip) resistor, which is in parallel with the LVDS's (off-chip) 100 Ω termination resistor; both resistors are of different nature, and hence an uncontrollable error results on the differential LVDS voltage (as the transmitter output is current driven). This degrades the realisable accuracy of the LVDS signal. Also, in cold spare two of these resistors are in parallel, further degrading and complicating things. Even worse, suppose several transmitters are put in parallel (obviously with only one being active), things can degrade even more. For all of these reasons, an alternative sensing of the common mode is implemented: two difference amplifiers are used, each having two current outputs; each of the two pins is compared with the common mode reference voltage. The four output currents are added two by two, and these sums then are added (closing the feedback loop) to the LVDS main output currents, one to the sinking current (bottom side of the transmitter's output H-bridge), one to the sourcing current (upper side). This mechanism then regulates the common mode voltage.

Table 1: Key features

TIA/EIA-644-A compliant LVDS inputs & outputs
Radiation hardness
TID: 300 krad (Si)
SET: 30 MeV.cm^2/mg
SEL: 118 MeV.cm^2/mg
Temperature (junction) range: -55 to 145 °C
Supply range: 3.0 V to 3.6 V
Cold spare functionality (LVDS & LVTTL)
Tri-state output control (LVDS & LVTTL)
Power down mode
LVTTLout: 3.3 V / SR control / output impedance optimized
LVTTL in: 3.3 V / 5 V tolerant
ESD
LVDS: 8 kV
LVTTL: 3 kV
Bit rate: 400 Mbps
LVDS receiver:
extended common mode input range: -4 V to +5 V
active failsafe operation
hysteresis; time-filtering going in & out failsafe
ESCC 9000 qualification (anticipated)
Die size (active circuit, dual transcvr): 1350 µm x 3176 µm

Note: the nominal difference between an output pin and the common mode reference voltage is 350 mV / 2 (350 mV being the nominal differential output voltage), this is 175 mV. Worst case this voltage can be somewhat higher still. The input range IR of the difference amplifiers then needs to be designed to be wider than this voltage (in order to still have regulation). Though this IR is rather high, it turned out to no problem.

III. LVDS EXTRA REQUIREMENTS & ISSUES

As said, on top of issues required by the LVDS standard [1], several extra features are implemented. They are discussed in this chapter.

A. Receiver ECM (Extended Common Mode)

To accommodate common mode voltage differences between transmitter and receiver, the receiver has an Extended Common Mode (ECM) input range. This extension is relative to the common mode already imposed by the LVDS standard [1]: ignoring the LVDS differential signal amplitude, the CM is extended from (0 V to 2.4 V) to (-4 V to 5 V).

As the device's power supply is 0 V to 3.3 V, the ECM range cannot directly be handled by the CMOS circuits. The solution then is to first compress (or attenuate) the differential input signal by a resistive voltage divider (partly towards GND, partly towards VDD). The compression factor is about 5; the extended input common mode range (-4 V to 5 V) gets mapped to (1.2 V to 3 V), and this voltage range then can be handled by the receiver's CMOS pre-amplifier. Note though that the area and power consumption (for the speed required) of that amplifier are compromised. Note also that the compressing circuit needs to pass both low bit rate (down to DC) and high bit rate LVDS signals, including their signal edges. For this reason, a capacitive dividing network is added to the resistive network, making it essentially all-pass. The LVDS receiver's input circuitry is show in Figure 2; the voltage attenuation factors are indicated. Note that also the differential amplitude is compressed by that same factor 5.

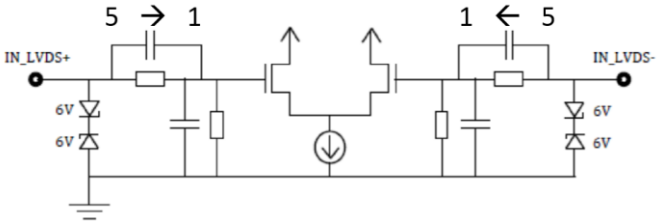

Figure 2: LVDS receiver input circuit: all-pass passive attenuation networks & ESD clamps

B. ECM & Receiver Sensitivity to LVTTL_out

As is clear from the previous chapter, the differential signal is compressed down to about 20 mV in the Rx signal chain (at minimum differential LVDS input amplitude, which is 100 mV, [1]). As a result, at these nodes the susceptibility to supply and other disturbances is high. Actually, this even holds for the LVDS (differential) inputs (pins) themselves. Finally, the input attenuation network is rather high impedant, again increasing signal susceptibility.

In the dual transceiver mode of the chip (the chip can actually also be configured as an LVDS 2x2 cross point; by an optional bond), an incoming LVDS signal is converted into an LVTTL (this is CMOS-like) output signal. And, that output is physically located next to the corresponding LVDS inout (and this is done for reasons of compatibility with existing devices).

The result of all this is a sensitive input, which is located next to the corresponding high amplitude output, and this is an

ideal recipe for an oscillator. And this is what occurred in the first spin of this device (be it that this "self"-oscillation was marginal). Several precautions then were incorporated in a re-spin, essentially solving the issue.

Hysteresis was added to the receiver. Receiver ground connections were made more robust (to reduce voltage drops). Two failsafe minimum duration requirements were implemented, reducing the sensitivity to (short) disturbances. These delays are seen in Figure 3: the two circuits enclosed by dashed rectangles and the corresponding textual details (rest of Figure 3 is discussed in the Receiver Failsafe chapter). Dedicated supply tracks were introduced for the LVTTL output cells, reducing potential crosstalk between these cells and the LVDS receivers. Slew rate control was added to the LVTTL output cell, as well as an optimized output impedance (limiting transients, while still maintaining good eye opening). The ESD protection at the receiver inputs was optimized to reduce the parasitic capacitance between these inputs and GND, reducing the impact of potential GND spurious on the inputs (actually, two clamp solutions existed; the one with the lowest capacitance, a factor three, then was favoured).

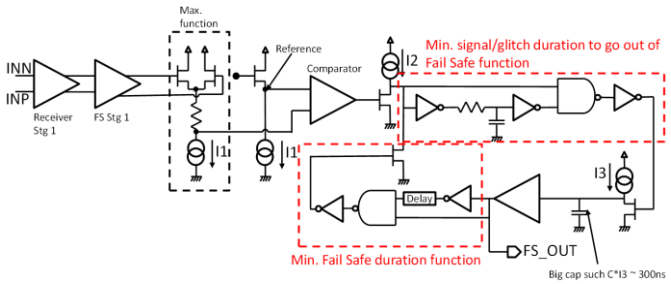

Figure 3: Receiver failsafe, and its minimum duration requirements

C. ECM & ESD

Due to the Rx ECM input requirement, the standard DARE180U ESD protection cannot be used. Indeed, that clamp, which is actually based on a ggNMOS (grounded gate NMOS), cannot tolerate pin voltages more than one Vbe below GND. Also the 5 V pin voltage is an issue, for gate oxide reliability issues (TDDB, time dependent dielectric breakdown).

The 5 V issue is solved though in the DARE library, by stacking two devices (the lower in ggNMOS configuration, the upper cascode-like on top), essentially distributing the pin voltage over both devices; this concept is borrowed. In the library solution, the supply voltage (3.3 V) is used to bias the gate of the upper ("cascode") transistor. However, because of the cold spare requirement, this solution cannot be implemented here (CS → VDD is zero while the pin might be at 5 V). As a solution, a resistive voltage divider is put between pin and GND, and the divider midpoint is used to bias the gate of the upper transistor; essentially, the bias voltage is extracted from the pin voltage (and hence only exists when needed, anyway); in order to guarantee a sufficiently low pin input current, the divider is implemented being high resistive.

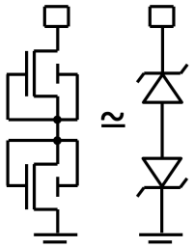

Figure 4: ECM input ESD clamp: stack (anti-series) of two ggNMOS

The negative voltage (down to -4 V) is handled by putting a second ggNMOS transistor in anti-series with the above described stack; see both Figure 2 and Figure 4 (5 V stack is not shown). Note that, similar to a single ggNMOS, the clamp is bi-directional, i.e. handles ESD pulses of both polarities. For each polarity, a ggNMOS, in series with a diode (of the other NMOS), clamps the pulse. This solution and the negative pin voltage requires the use of the technology's triple well (used for the bulk of the two devices) option.

Because of patent infringement reasons, some other issues apply, which cannot yet be disclosed (patent application still to be issued).

Details about the radiation tolerance of this solution are available in [5].

D. Receiver Failsafe

The receiver is to be failsafe, and this function is to be implemented on chip, and using active circuitry (as opposed to passive resistor based solutions). Failsafe refers to the requirement that the receiver has to perform in a well-defined way under several erroneous pin conditions. These conditions: inputs open, inputs floating (i.e. the driving transmitter is turned off), inputs shorted. Each of these states is detected, and the receiver output is set to logic high (as required). The fail detection monitors the LVDS input. Basically a fail is reported when the differential signal at the receiver input is lower than some fraction of the minimal LVDS input signal (which is 100mV, according to the LVDS standard). Note that without this function, the receiver output might show random toggling between zero and one (while there is no indication that this is no valid data).

A possible failsafe implementation can be seen in patent [6], the idea is based on a window comparator. An application note [7] goes in more detail. Because of the patent, this idea cannot be used here (as said).

As an alternative, ESA proposed to first rectify the differential input signal, and then to apply a level detection, as shown in Figure 3. This idea is implemented in the chip, and is patented by ESA [8]. Some more transistor-level details are presented in the conference's presentation.

The circuit enters the failsafe state only after a minimum (failsafe pin condition) duration of 600 ns (nominal; failsafe activation delay). This delay: Figure 3: current source I3 charges the connected capacitor until a certain voltage level is reached. The de-activation delay is 50 ns max (no explicit delay circuit). The failsafe differential input level is set to 50 mV nominal.

Figure 3 shows two more delays, which were already discussed (chapter about Receiver Sensitivity).

E. Cold Spare

Clearly the device has to be cold spare compatible, allowing the application (PCB) to contain two of the devices connected fully in parallel except for their supplies, one device being active ("supplied") while the second is a ("cold") spare; this is a typical space-grade construct / requirement. To allow for this, the typical drain-bulk (parasitic) diode of output PMOS transistors cannot be allowed (as the cold device would be powered from that IO pin). At the time of the design the applicable patent [9] still was active, and hence we came up with a variation of that idea. This was applied in the LVTTL output cell, and in the 5 V tolerant input (see the specific chapter). As in the patent, the idea is again based on a PMOS switch transistor that connects the bulk of the actual PMOS to VDD only when VDD is up. The diode path IO pin - VDD consists of two PMOS drain-bulk diodes in anti-series, and hence the path is always blocked (see [9] for details).

Another issue is the usage of ggPMOS transistors (clamp towards VDD) for ESD protection (in parallel with ggNMOS towards GND), as used in the DARE library. It turned out that sufficient protection can still be guaranteed in the LVDS chips when the ggPMOS is simply removed.

A third issue is the H-bridge output of the transmitter. Typically the two upper switches are implemented as PMOS transistors, but this is not compatible with the cold spare requirement. It turned out though that replacing these with NMOS devices was no issue: the output voltages are far enough below VDD to allow for this solution (though almost no margin is left); no triple well (eliminating the bulk effect), nor low-VT devices were necessary.

F. Failsafe & Cold Spare, & the DARE180U Library LVDS Cells

It is important to note that in the near future, for the DARE180U standard cell library, a second version of the LVDS cells will become available, incorporating:

- cold spare compatibility
- receiver failsafe (as defined in this paper).

(The current DARE180U LVDS standard cells do not include these functions.)

Note though that there are no plans to incorporate an extended common mode input range (ECM) in (the/a new version of) the LVDS receiver standard cell.

G. LVTTL Input: 5 V Tolerant & Cold Spare

This LVTTL input is required to be 5 V tolerant. In combination with the cold spare requirement, this imposes several design concerns.

For ESD, we use a stack of two clamps (5 V) as described already for the LVDS receiver. And again the bias voltage of the gate of the upper device is an issue when VDD is not present (cold spare); again the voltage is extracted from the pin voltage (necessarily resulting in a DC pin current, which hence needed be designed to be sufficiently low). This time several MOS diodes are stacked to do the voltage extraction from the pin voltage. This is done because an extra requirement complicates things: as this is a CMOS-like input, the gates of the transistors of the first inverter are to be driven by the pin. Again a series transistor is needed to distribute the pin voltage (5 V) over more than one device. And again a voltage is to be extracted from the pin, to bias that series transistor.

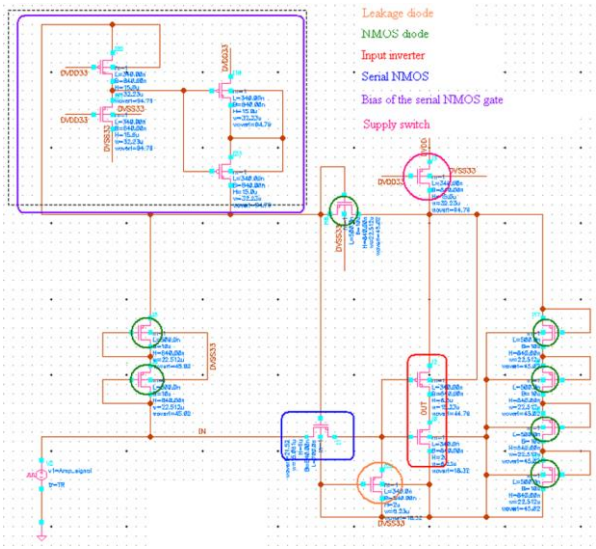

Figure 5: 5 V tolerant and cold spare compliant digital input

Having a drain of a PMOS transistor tied to the pin could not be avoided, when realising the just described bias circuit. Then, for cold spare reasons, again extra circuitry is needed, to avoid the bulk of that PMOS to be directly tied to the VDD node. The technique described in the Cold Spare chapter then is also applied here.

The circuit is shown in Figure 5. (The ESD clamp is not shown; not all details are discussed in the text.)

H. Radiation Hardness

The design is done within imec's DARE ecosystem, including the DARE180U (name refers to the specific CMOS technology used) library of standard cells and IP. Available know how is incorporated into the design of the LVDS chip. See [10] for a description of how radiation know-how is incorporated in the DARE180U transistor level design environment, by an enhancement of the foundry's PDK.

1) TID

TID, Total Ionising Dose, is the effect that under radiation, over time physical / electrical characteristics do move, resulting in the creation of potential leakage paths (this is: when subject to certain bias conditions).

Use of ELT (Enclosed Layout Transistors) avoids source drain leakage along the STI (Shallow Trench Isolation, the technology's thick oxide device isolation) edge between source and drain. Straight transistors are only used when source and drain are at same potential, the only use-case being an MOS capacitor. MOS capacitors are used for SET hardening and for supply decoupling.

Leakage between N-type regions (Nwell, N+ NMOS S/D implants) is avoided by the use of P+ guards (tied to the bias

voltage of the P- substrate in which they reside, GND). Clearly this is only required when the N-type regions are at different potential.

2) SET: the Event

Single Event Transients are due to charge deposited on a node, due a particle strike. The charge accumulation is a sub-nanosecond event. Along the particle's trajectory through the silicon, electron-hole pairs are being generated; normally these carriers recombine, but the electric field in the depletion region of a reverse biased PN junction separates the positive and the negative carriers, resulting in a net charge that accumulates on both of the nodes. It follows that every source/drain of every MOS transistor is subject to this potential charge deposition.

It also follows that the deposited charge is proportional (first order) to the junction's reverse bias voltage. For modelling & simulation we assume (worst case) that this voltage is equal to VDD, corresponding to a charge collection depth of 2 µm.

Further, the number of generated electron-hole pairs is proportional to the LET (Linear Energy Transfer) of the particle. The LET spec to be achieved is 60 MeV.cm^2/mg. Indeed, the particle flux for higher LET particles is low enough (flux decreases strongly for rising LET) for the chip to be able to realise the required SER (Soft Error Rate). (General statement.)

For simulation: using the above, and the fact that for silicon an LET of 100 MeV.cm^2/mg corresponds to 1 pC/µm: our maximum injected charge is 1.2 pC.

3) SET: how to Mitigate the Impact

By design, the impact of Single Event Transients is handled and mitigated in several different ways.

Capacitive hardening: a capacitor is put between the node concerned and a supply rail. Obviously this proportionally reduces the voltage impact of the deposited charge (ignoring the node's intrinsic cap). Capacitors are also used in a different way: capacitive-driven negative feedback is used to actively reduce the impact of a hit. Depending on the circuit, one can just use the existing circuit and add a capacitor between two nodes. Or, some SET-hardening clamps are designed that can be put on a node-to-be-SET-hardened. All these different concepts are used mainly in DC biasing circuits within the analog cells. Examples are shown in Figure 6. Capacitor type: MIM or MOS. For MOS cap: take the chapter about Hot PMOS into account. MOM capacitance: not used for SET hardening, as this type of cap would require too much area.

Drive strength hardening is applied in the digital cells (the die only contains combinatorial cells); an increased drive strength results both in an increased output node capacitance (the SET pulse amplitude is reduced proportionally), and a faster evacuation of the deposited charge (the charge might even be evacuated while it accumulates).

In static / low speed digital signals (e.g. the power down signal), low pass RC filters are used to remove the (anyhow short) SET pulses; the time constant needed is in the order of several nanoseconds.

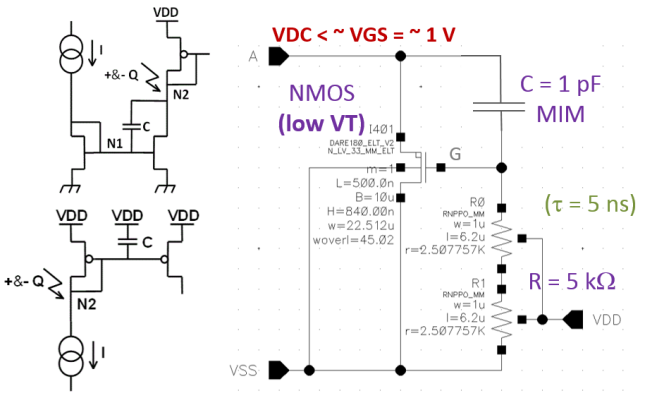

Figure 6: Several SET hardening techniques

Note: clearly the likelihood that a junction is being hit by a particle is proportional to the area of that junction; the sensitivity (in this respect) of the junction is quantified by its cross section; it is the equivalent area that, when hit, results in an SET event. On the other hand, the chip is to realise a certain maximum SER, Soft Error Rate (or, more in general, a BER, Bit Error Rate; communication systems are never required to be perfect in this respect). Combining all this with the expected particle flux (which is a function of e.g. the satellite's orbit): a certain cross section can be tolerated to be un-hardened (or being hardened only until a certain LET < 60 MeV.cm^2/mg. As certain nodes (e.g. analog nodes in the signal path) are difficult to harden (due to the high signal speed), one can justify not to harden them (which we actually did).

4) SEL and SEU

SEL, Single Event Latch-up, is to some extend intrinsically handled by the P+ guarding imposed by TID hardening.

SEU, Single Event Upset, does not apply as the design does not contain any memory element.

IV. Other Design Aspects

A. SET Sensitivity and "Hot PMOS" Devices

In the course of the project a too high SET (Single Event Transient) sensitivity was observed during heavy ion testing (relative to results from simulation). A laser test then was performed, trying to find the rout cause of this behavior: a laser beam is stepped over the die, and at every stop a pulse is fired (mimicking an SET event), and the die response is monitored. The laser has a spot size of about 2 µm, which is sufficiently small to identify the structures causing the issue. It was found, see Figure 7, that PMOS devices having their bulk node not tied to VDD are responsible. This type of devices was used for two different purposes. First, to have an MOS capacitor with the desired CV behavior (as needed by the specific circuit), capacitors meanly intended to reduce SET susceptibility (note that the opposite effect was realised!). The second use case: avoid the bulk effect, allowing more voltage headroom, alleviating the design of certain circuits. We are referring to these PMOS devices as "hot PMOS" (referring to their bulk being tied to a node that is not really low impedant).

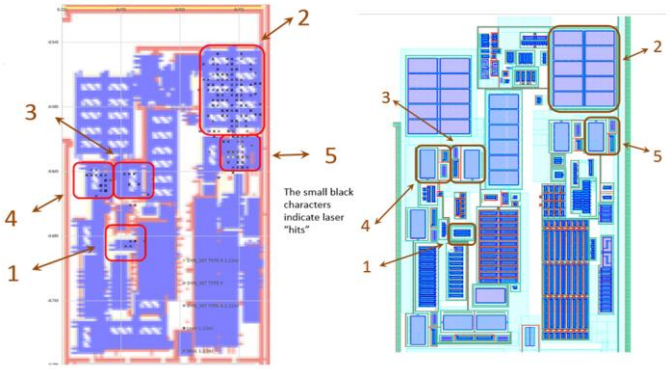

Figure 7: Input from laser testing, and identification on actual layout

A design tuning then was done, removing these devices: 1. replacing the capacitors by MIM caps, and 2. adapting the circuits to allow the PMOS transistors to have bulk effect. Heavy ion testing on the new devices then confirmed the anticipated improvement.

At the moment it is not clear why hot PMOS transistors show this behavior. The bipolar amplification effect is not sufficient (as shown by electrical simulations); TCAD modelling & simulation is currently being employed. On the other hand, we now have as a general rule to not allow the usage of this type of devices.

Note: the design also uses some triple well NMOS transistors, which have their bulk node different from GND (i.e. this is why they are used in this design). Hence they might be expected to suffer from a similar effect. So far we have no evidence though that this is the case.

B. Damped Package-Die Resonance

Significant on-chip supply decoupling is provided, consisting of MOS, MOM and MIM capacitors; all three can be physically stacked. However, the package supply inductance, combined with this on-chip capacitance (between GND and VDD) realises an LC resonant circuit, Fres = 1/2πsqrt(LC). If this network is excited at its resonance frequency Fres, a significant AC signal could get superimposed onto the chip's supply, compromising the chips behavior. We avoid this to happen by damping this network: the on-chip decoupling capacitance is split into two (parallel) groups: one group is a pure cap, but the other is a cap with an explicit resistor in series. The resistor is sized so as to dampen the LC. The final intention / purpose is to reduce the quality factor Q of the network, to the extent that when the supply gets excited by the edge of a repetitive signal (having a frequency equal to the resonance frequency of the network), that that excitation is to have disappeared when the next edge occurs. This then avoids the supply disturbance to build up (to a more significant / harmful amplitude).

Note: both the resistor and the caps are distributed all over the die, using a (small) unit cell that then is instantiated on many places. This ensures that also the damping part of the network is present everywhere.

The total amount of on-die decoupling capacitance is about 4.5 nF, half of it being high speed (f-3dB > GHz), half being low-frequent (used for damping). The impact of this improvement (reduction) on Q is seen is Figure 8 (showing the supply AC impedance of the die as a function of frequency). In total four different dice were made, hence the four different curves (for all: without and with damping; note that we also doubled the amount of capacitance when implementing the damping (the two modifications are un-related)).

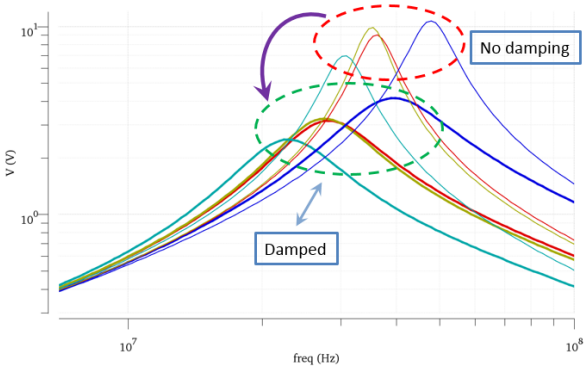

Figure 8: Package-die resonance: impact of damping decoupling

C. Power Down Mode

Though it is stated in the introduction that low power consumption is one of the benefits of LVDS, consumption is still somewhat significant. The transmitter output current is 3.5 mA, as set by the standard [1]. The receiver consumes several mA, to be able to amplify the differential high speed into a digital signal; the ECM requirement, resulting in an initial factor five amplitude reduction (hence down to about 20 mV differential, worst case), has a significant responsibility in this respect.

For this reason, a power down mode is implemented. The device automatically powers down when all outputs are disabled (i.e. tristated). Actually, at package level, two versions of the chip exist, one having this feature, and one that does not have it (selection is done by an optional internal bond). Indeed, one drawback of the power down mode: when powering up again, it takes some time before all internal circuitry is up-and-running again (main delay is due to the bandgap), and, worse, during this start-up time the LVDS outputs risk to output corrupted data (in the electrical domain). For this reason, the outputs are released only when the circuit is fully up. This (on-chip generated) delay is between 150 µs and 500 µs. Note that going into power down is fast, and anyhow the outputs are immediately put in tristate.

Note: another drawback of the power down mode: chips that are intended to be replaced by this design (see also the Introduction) do not have this power down mode, and hence the powerdownable device is not fully (functionally, or even pin) compatible (but our other version is).

D. ESD: 8 kV

The LVDS pins have an ESD HBM (Human Body Model) 8 kV requirement. As this level is simply proportional to the width of the ggNMOS clamp transistors (see Figure 4), implementation was straightforward. Note though that the required area increases accordingly.

E. Receiver testability

Testing the receivers on a standard analog/mixed ATE (Automatic Test Equipment) turned out to be difficult. Reason is the combination of

- the four different input thresholds (all to be tested): the receiver itself has two levels because of the implemented hysteresis, and the failsafe also has two levels, positive and negative threshold; all four differential
- the failsafe timing specification
- the only output available (for observation) is the output of the receiver itself, which is a combination of the output of the receive function and the output of the failsafe detector;

  no other pins (for test) are available, for compatibility reasons with existing devices;

  see Figure 1
- implementing a test mode using the functional pins is not allowed, because it would need to rely on e.g. voltage levels of (functional) pins; for space application such a strategy is not sufficiently secure (chip should never-ever enter test mode in normal operation). (As said, having an explicit test pin was not possible.)

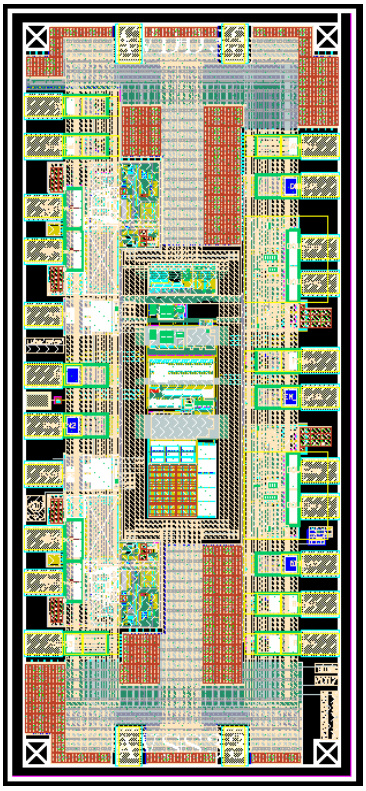

Figure 9: LVDS dual transceiver chip: layout

Hence a test mode was implemented, but that mode is only available at probe level (which is sufficient to guarantee devices to be OK). Extra pads allow to disable failsafe, and to observe the failsafe outputs. (The failsafe disable pad is resistively pulled to enable when not probed, which is very secure). So note that no pins correspond to these pads. All pads then were enlarged, to allow both probing and bonding but at a different coordinate (needed for space reliability reasons). These enlarged pads can be observed in Figure 9.

CONCLUSIONS

A space-grade LVDS transceiver chip is designed, using a standard CMOS technology, and using radiation hardening by design (RHBD) techniques. On top of standard requirements, as e.g. imposed by the LVDS standard, quite some extra features were incorporated. The device passes both electrical verification and radiation testing, both TID and SET. No SEL has been detected. Note that SEU does not apply, as the die does not contain any memory element.

Die layout is shown in Figure 9.

ACKNOWLEDGEMENT

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Robust CMOS time-based sensor interfaces for space applications

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Abstract

This paper presents an overview of the robustness properties of CMOS time-based sensor interfaces using BBPLL-based architectures, which show a good compatibility with harsh space environments. Two study cases are discussed: a BBPLL-based capacitive sensor interface which can achieve 14-bit resolution using the chopping technique to reduce the effect of 1/f noise, and a fully-differential BBPLL-based resistive-bridge sensor interface that has a very high drift resilience by combining different digitally-assisted techniques. The demonstrated robustness proves that this architecture is a valid candidate for space applications.

I. Introduction

Space applications are a growing field, yet the harsh environment of space missions is at the same time a challenging playground for electronic sensor systems. The need for accurate and reliable information about on-board environmental parameters but also about structure sanity, turbine combustion and fuel tank state, among many others, requires sensor systems to be placed *in situ* [1]. Hence, these robust, reliable and accurate sensing systems are required to operate in hostile environments.

Several harsh-environment-compatible features have already been demonstrated using the BBPLL-based CMOS sensor interface architecture for both capacitive [2] and resistive [3] sensors. The main property of the BBPLL-based time-based architecture is its robustness provided by the direct sensor-to-digital conversion, by means of the time-domain representation of the sensor data. Since the sensor analog signal does not need to be amplified before digitization, area- and power-efficient designs are achieved which are compatible with advanced, highly-scaled CMOS technologies. Additionally, its oversampled conversion provides enough redundancy to filter out in the digital domain corrupted data, produced by analog transient effects such as single-event radiation effects. Another feature is the highly-digital implementation, compatible with digitally-assisted techniques such as time-based signal chopping and differential-path tuning, which can improve the resolution and accuracy performance of the system by reducing the effect of DC and low-frequency perturbations. These techniques can be configured to implement simple built-in self-test strategies that can provide information about the state of the circuit and feed this back for compensation. In such way, smart system-level operation can be achieved by driving capabilities at the local level, for example in the case of wireless sensor networks.

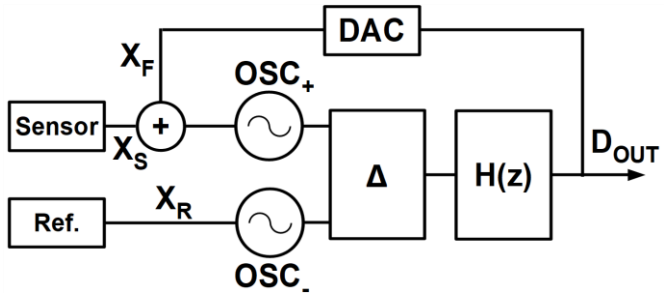

Figure 1: Block diagram of the BBPLL-based sensor interface

This paper presents an overview of the robustness features that make the BBPLL-based CMOS sensor interface suitable for space applications. Two demonstrator cases are discussed as good examples on how CMOS technologies are used as a low-cost platform for space sensors systems. The first demonstrator is a BBPLL-based capacitive sensor interface which can achieve 14-bit resolution [4]. The interface uses time-domain chopping as the main source of compensation for the oscillator mismatch and the low-frequency noise.

The second interface is a fully-differential BBPLL-based resistive-bridge sensor interface. It provides a very high drift resilience by combining different digitally-assisted techniques [5]. A simple online monitoring technique allows to compensate for sources of drift such as temperature, package strain variations and circuit component degradation. Hence, this interface is suited for harsh environments. The target temperatures in this work, even if not yet the maximum required values for space applications, demonstrate the validity of the principles.

This paper is organized as follows. Section II summarizes the BBPLL-based sensor interface operating principle. In Section III, the main requirements for space application sensors are discussed. The design cases are presented in Sections IV and V. Finally, Section VI concludes the paper.

II. BBPLL-based Sensor Interface Operating Principle

The time-based BBPLL architecture, described extensively in [6], is depicted as a block diagram in Fig. 1. The BBPLL-based sensor interface architecture uses oscillators to convert an analog sensor signal X_S into a digital time-domain signal D_{OUT}. The operation of the system is based on the phase locking of the feedback loop. The sensor value is converted to discrete output changes and propagated through the feedback loop as a feedback signal X_F which is added to the input X_S each time the phase detector (Δ in Fig. 1) makes a comparison to track the reference value X_R. Due to

the nonlinear phase detection block, the classical Laplace frequency-domain analysis cannot be used to obtain the system transfer function. Thus, the output reading needs to be obtained by averaging a time-domain train of pulses. To understand the system conversion operation, the time diagram illustrating a simple example is shown in Fig. 2.

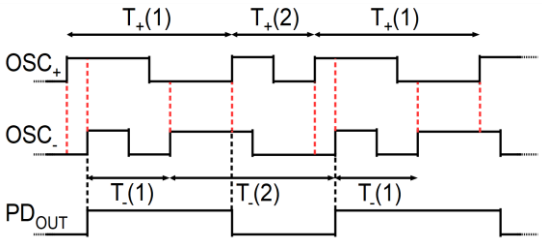

Figure 2: Limit cycle time diagram of the BBPLL-based interface.

Phase locking produces orbits or limit cycles in the phase plane of the system [7]. In this illustrative example, the minimum number of limit cycle values is chosen for simplicity, i.e. two values, identified as value 1 and value 2. The locking condition implies that the total orbit period of both input nodes is equal:

$$T_+(1) + T_+(2) = T_-(1) + T_-(2) \qquad (1)$$

The linear oscillator period characteristic T_+ and T_- as a function of the control variable X (defined by the type of sensor) is written as:

$$T_\pm = T_{0\pm} + T_{1\pm} \cdot X \qquad (2)$$

where $T_{0\pm}$ is the free-running period of $OSC_\pm$ and $T_{1\pm}$ is the gain of $OSC_\pm$.

Assuming matched and period-linear oscillators ($T_{0+} = T_{0-}$ and $T_{1+} = T_{1-}$), the average input variable values of the two oscillators for any number of limit cycle values are forced to be equal:

$$avg(X_S + X_F) = avg(X_R) \qquad (3)$$

The sensor generates a signal $X_S = X_{S0} + \Delta X_S$ with a base value X_{S0} and a sensor variation ΔX_S. If the reference input variable X_{R0} is equal to X_{S0}, then:

$$avg(\Delta X_S) = -avg(X_F) \qquad (4)$$

where X_F is an analog representation of D_{OUT} through the DAC, and is expressed as:

$$X_F = LSB \cdot D_{OUT} \qquad (5)$$

LSB is the least-significant value of the DAC. Therefore, the average sensor variation is related to the digital output of the interface as follows:

$$avg(\Delta X_S) = -LSB \cdot avg(D_{OUT}) \qquad (6)$$

In general, the system needs to be initially calibrated since the LSB value is not accurately known due to process variations, and X_{R0} and X_{S0} can be different due to mismatch effects. Nevertheless, it must be noted that the system transfer function does not depend on the absolute values of the oscillator period, and thus the sensor interface is inherently resilient to the variation of the period value.

III. Space Sensor Interface Requirements

The highly-digital sensor interface implementation of Fig. 1 ensures a compact and low-power operation. These are important features required by space devices such as probes, launch vehicles and satellites, since only limited size and weight is available, constraining the dimensions of the power supply elements such as batteries and solar panels [8]. Moreover, self-heating due to poor heat dissipation in vacuum can corrupt the measurement or destroy the circuit [9], which is a reason to minimize the power consumption of the sensor system.

Additional considerations are related to harsh environment requirements, which are highly dependent on the type of mission (date, duration and orbit) [10]. In the hostile context of space applications, the sensor systems need to operate under extreme temperatures, thermal cycling, pressure and radiation conditions. From the point of view of the sensor interface, silicon circuits are subject to drift in their physical properties due to environmental parameters such as temperature and pressure. The latter can also vary with humidity after initial calibration, for example due to changes in package stress [11]. The sensor interface characteristic drift generates an error in the measurements and requires complex compensation procedures (e.g. measuring the source of drift and compensating it using a lookup table) or recalibration [11]. The latter is most often not possible in space applications. Thus, extended operating condition ranges need to be considered during design depending on the type of mission. For example, the International Space Station rule of thumb for temperature extremes in the LEO orbit is in the range between -200°C and 200°C, with 16 thermal cycles per day [12].

The effect of radiation on silicon electronic technologies is divided into two categories: total irradiation dose (TID) and single-event effects (SEE). For digital circuits, different strategies such as added redundancy, layout techniques and architectural adaptations have shown good results. However, analog circuits are more sensitive to errors produced by radiation due to their continuous-time operation. From the modelling point of view, the net effect of TID is equivalent to adding an extra process corner point to integrated circuit variation simulations [13], due to the acceleration of device aging. Thus, this net permanent change in the physical properties of the circuit can in principle be cancelled out by the BBPLL-based interface's differential structure. On the other hand, the effect of SEEs is a transient charge injection on the circuit's nodes [14]. Since the BBPLL-based sensor interface is an oversampled system with a well-defined limit cycle for low-bandwidth input signals, the corrupted data due to sudden interruptions in the locked operation can be filtered out in the digital domain.

Table 1: Space sensor interface requirements and associated concepts/techniques used in the BBPLL-based architecture

Requirement	**Concept/technique**
Size and weight	CMOS compact and low-power implementation
Power consumption	Highly-digital low-power architecture
Extreme temperatures	Fully-differential design
Temperature cycles	Time-domain chopping and oscillator calibration
Total irradiation dose	Fully-differential design
Single-event effects	Digital filtering of oversampled data
Degradation (e.g. package stress changes)	Time-domain chopping and oscillator calibration

As mentioned before, the sensor interface output depends on the difference between the oscillator periods, and thus the absolute oscillator period is not relevant. Therefore, the locking condition ensures a good rejection of common-mode perturbations produced by uniform temperature and pressure variations. Furthermore, initial and time-varying mismatch in the differential path, caused mainly by the mismatch between the oscillators' transfer function, produce gain and offset errors at the system output. The errors are removed by digitally-assisted techniques such as time-based chopping and oscillator tuning, as described in section V. A summary of the space sensor interface requirements and the respective concepts/techniques used in the BBPLL-based architecture is presented in Table 1.

IV. High-Resolution Capacitive Sensor Interface

Accurate and robust sensor systems are essential for the implementation of autonomous systems, which are also becoming more and more important in the context of space applications. In this section, a capacitive sensor interface demonstrator is presented which uses time-based chopping to increase the conversion resolution at low sampling periods, otherwise degraded by 1/f noise produced by the oscillators [4]. The architecture is shown in Fig. 3.

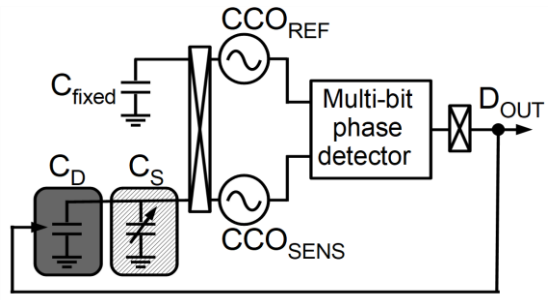

Figure 3: Block diagram of the capacitive sensor interface [4].

A. Time-domain chopping technique

Traditionally, chopping has been used in the voltage domain as an open-loop dynamic offset cancellation technique that reduces the effect of low-frequency amplifier imperfections [15]. The technique uses modulation to shift the signal to higher frequencies where there is no effect of DC offset and 1/f noise, and then demodulates the signal back to the baseband, upconverting the unwanted part of the signal, that is then filtered in a subsequent stage to recover the original signal with reduced low-frequency disturbance.

Since the 1/f perturbation is contained in the phase of the oscillator in the time-based case, it is possible to make an analogy between the effect of 1/f noise in time-based and in amplitude-based systems. An error is introduced when the phase is compared and thus interchanging the electrical position of the oscillators at the input of the phase detector cancels the undesired 1/f noise otherwise present at the output. This is chopping in the time domain.

B. Simulation and measurement results

The system has been simulated at transistor level in Spectre using a standard 0.18 µm CMOS technology PDK to extract the parameters that represent the nonidealities of the different building blocks. These parameters have been used in a Matlab state variable model to simulate the spectrum of the system output with and without chopping, as seen in Fig. 4.

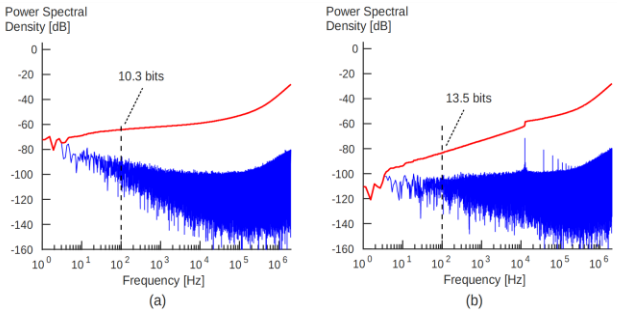

Figure 4: Simulated SNR for the non-chopped and chopped cases for the capacitive sensor interface in Fig 3.

The simulations show that the 1/f noise produced by the oscillators is modulated to the output, limiting the resolution for high oversampling ratios (OSR) (Fig. 4(a)). The time-based chopping technique attenuates the effect of 1/f noise (Fig. 4(b). In the example, 3.2 ENOB is gained at 100Hz bandwidth thanks to the chopping technique.

The capacitive sensor interface has been implemented in a standard 0.18 µm CMOS technology. The output trace has been obtained for a constant input during 1ms sampling time to calculate the PSD for both the chopped and non-chopped cases. This allow to calculate the SNR at different bandwidths, as shown in Fig. 5. The use of chopping restores the 10dB per decade trend expected from theory. This technique is used in the next section to compensate for drift errors in a fully differential resistive sensor interface.

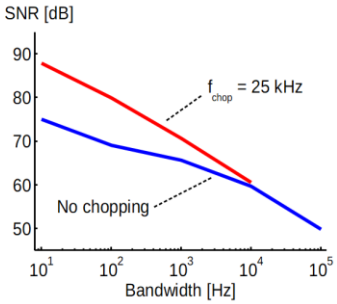

Figure 5: Measured SNR versus bandwidth for the non-chopped and chopped cases for the capacitive sensor interface in Fig 3.

V. Drift-Resilient Resistive Sensor Interface

The high robustness requirements imposed by harsh environments in space missions are a demanding challenge nowadays for the design of electronic systems. While the harsh environment operation and stability of resistive sensors has extensively been studied in the last years [16,17], the drift performance of the sensor interface is now a topic of interest. Sensor interfaces condition and convert the sensor signal to the digital electronic domain, and thus their stability is essential for high-performance sensor systems.

In this section, a second proof of concept is presented to demonstrate the drift-resilient capabilities of time-based sensor interface architectures for differential resistive sensors. The architecture is shown in Fig. 6.

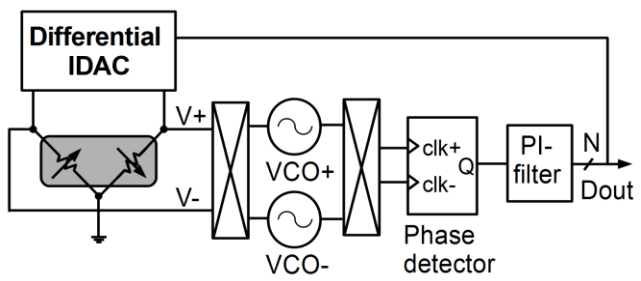

Figure 6: Block diagram of the differential resistive sensor interface.

A. *Drift resilience by design and using digitally-assisted techniques*

The presented architecture uses a current feedback bridge to transform the differential resistive bridge sensor values into voltages V+ and V- that drive the two VCOs. In the locked state, the voltages V+ and V- are forced to the same average value by the fully-differential feedback loop, as concluded in section II. Thus, the input-output characteristic is described by the following simple expression:

$$\frac{\Delta R}{R_0} = \frac{I_{LSB}}{I_0} \cdot D_{OUT} \qquad (7)$$

In case of perfectly matched VCOs, the highly-digital nature of the proposed architecture makes the transfer characteristic dependent on only a ratio of I_{LSB} and I_0. Since highly-accurate and stable current ratios are ensured using current mirrors and common-centroid layout techniques, this architecture is inherently resilient to drift.

However, the mismatch and drift errors in the VCOs produce offset and gain errors in the transfer characteristic. These errors are temperature dependent and cannot be predicted beforehand, requiring time-consuming and expensive calibration procedures.

A method to reduce the above-mentioned errors in a single-temperature calibration is presented in this section. The approach combines two complementary digitally-assisted techniques: VCO time-based chopping and VCO tuning. The first technique dynamically compensates both the gain and offset VCO errors. Additionally, time-based chopping attenuates the effect of low-frequency noise introduced by the VCOs below the chopping frequency f_{chop}, as discussed in the previous section. The second technique reduces the chopping spikes and increases the full-scale range degraded by the mismatch between the VCOs using a VCO tuning algorithm. The method ensures that the initial sensor interface calibration is valid for a wide range of operating scenarios and long lifetime, without the need of additional measurements or offline recalibrations.

B. *Simulation results*

The state-variable model from [6] is used to simulate the resistive sensor interface system that implements the chopping technique. In Fig. 7, the simulated and analytical model error resulting from VCO free-running frequency error (OST0) and gain error (OST1) are plotted [5]. The normal phase (initial position of the VCOs), the inverted phase (inverted position of the VCOs) and the activated chopping cases are depicted. The plots show that the output errors due to mismatch between the VCO characteristic functions are completely removed by chopping.

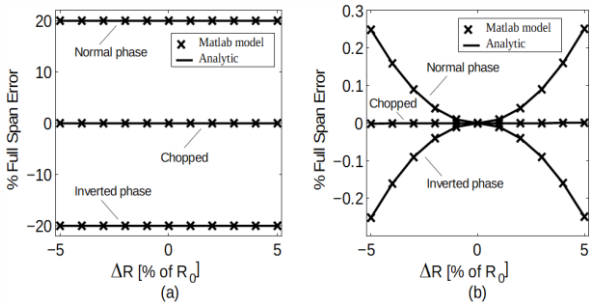

Figure 7: System output error for (a) a free-running period error OST0 = 1% (with OST1 = 0%) and (b) a gain error OST1 = 10% (with OST0 = 0%).

In Fig. 8, the output error is plotted when a combination of VCO free-running frequency and gain errors are present. The chopping technique greatly mitigates the output error, but it cannot remove it completely. The error is lower than 0.05% of the full scale if OST0 and OST1 are less than 3%.

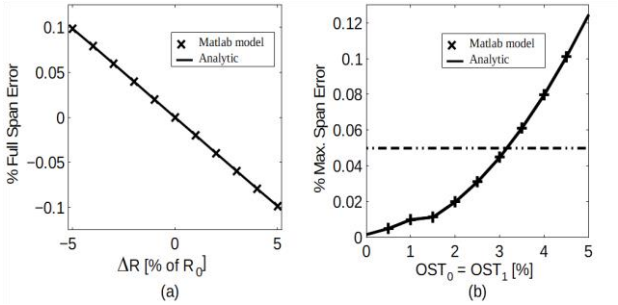

Figure 8: (a) The error produced by OST0 = 1% and OST1 = 10% using the current feedback is not fully removed by chopping. (b) The maximum output error increases with increasing OST0 = OST1.

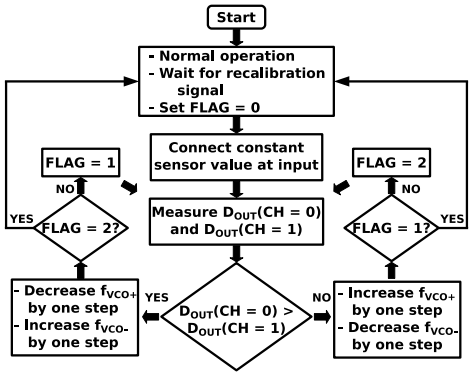

Figure 9: VCO tuning algorithm flowchart.

To achieve a low drift even in cases in which the error in the differential path increases over time, such as temperature-dependent VCO mismatch, circuit degradation or local permanent radiation effects, the VCO tuning technique is used. The main advantage of this technique in the context of BBPLL-based sensor interfaces is the fact that accurate

external references are not needed, since a fixed arbitrary input is enough to determine the error from both chopping phases. In Fig. 9, the tuning algorithm is depicted. A tuning example is shown in Fig. 10, where the tuned condition is achieved after 3 tuning steps.

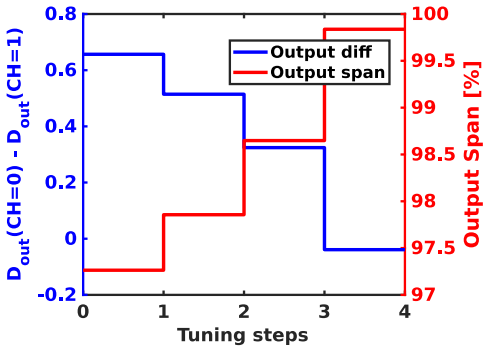

Figure 10: Output span recovery achieved using the VCO tuning algorithm.

The system has been simulated at circuit level using a standard 0.18µm CMOS technology PDK to verify the performance over a temperature range between -40°C and 175°C. In Fig. 11(a), the free-running average frequency of the VCO is plotted, showing a considerable variation over temperature. In Fig. 11(b), the current ratio I_{LSB}/I_0 present in the system transfer function is plotted, demonstrating the small variation achieved. Very stable current ratios are achieved using proper layout techniques. In Fig. 11(c), the simulated system output error variation with respect to the theoretical equation (7) is plotted, demonstrating a very stable operation over a wide range of temperatures despite the common-mode variations.

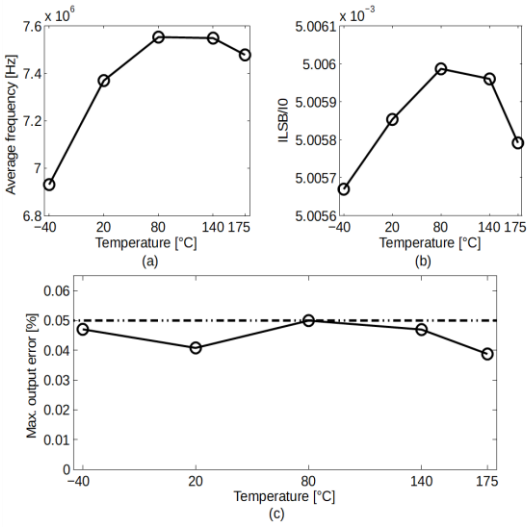

Figure 11: (a) The VCO locked frequency drifts with temperature. (b) The ratio I_{LSB}/I_0 has minimal drift. (c) The maximum absolute output error of the full system is less than 0.05% over the temperature range between -40°C and 175°C.

Another issue is the nonlinearity at the system output produced by the DAC element mismatch. This issue is attenuated using the dynamic element matching (DEM) technique, which modifies the order in which the DAC elements are used at each clock cycle. This averaging combined with the oversampled operation reduces the effect of the DAC element mismatch. The plots in Fig. 12 show the histogram of the nonlinear output error for a Monte-Carlo run using 1000 samples. The maximum nonlinear error is reduced below 0.05% of the full scale.

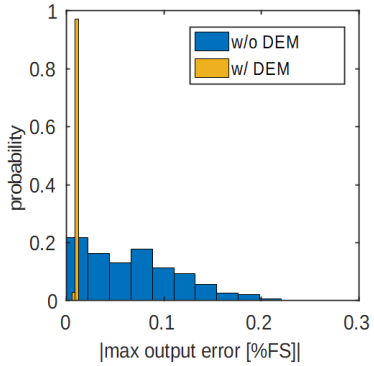

Figure 12: Histogram showing the maximum output error over the entire input range for 1000 Monte-Carlo I-DAC mismatch configurations without and with DEM using a random error of ±1%.

VI. Conclusion

The CMOS time-based sensor interface examples discussed have medium-to-high resolution, consume low power and have a small footprint. It results in low-area and low-weight implementations as needed for space applications. Additionally, high robustness is achieved using the BBPLL-based sensor interface architecture with the presented techniques and without a large overhead in power or area. This work constitutes a step towards robust, accurate, light/compact and smart sensor systems that can collect and process high-fidelity data in todays' space missions.

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Status update on GR716 Rad-Hard Microcontroller For Space Applications

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Abstract

This paper describes the mixed-signal microcontroller GR716 targeting embedded control applications with hard real-time requirements. Prototype devices are currently beeing tape-out in the activity *Microcontroller for embedded space applications,* initiated and funded by the European Space Agency (ESA).

The presentation and paper will describe the architecture, functionality and simulation results of the device. This abstract describes an on-going development where the devices are in the stage to be taped-out.

I. BACKGROUND

Software based data acquisition, dataprocessing and simple control applications are widely used in spacecraft subsystems. They allow implementation of software based control architectures that provide a higher flexibility and autonomous capabilities versus hardware implementations. For this type of applications, where limited processor performance is required, general purpose microprocessors are usually considered incompatible due to high power consumption, high pin count packages, need of external memories and missing peripherals. Low-end microcontrollers are considered more attractive in many applications such as:

- Propulsion system control
- Sensor bus control
- Robotics applications control
- Simple motor control
- Power control
- Particle detector instrumentation
- Radiation environment monitoring
- Thermal control
- Antenna pointing control
- AOCS/GNC (Gyro, IMU, MTM)
- RTU control
- Simple instrument control
- Wireless networking

In these kind of applications the microcontroller device should have a relatively low price, a low power consumption, a limited number of pins and must integrate small amount of RAM and most of the I/O peripherals for control and data acquisition (serial I/Fs, GPIO's, PWM, ADC etc.). The requirements for memory and program length are usually minimal, with no or very simple operating system and low software complexity.

II. MICROCONTROLLER APPLICATIONS

Spacecraft subsystem control and monitoring of parameters such as power supply voltages, currents, pressures and temperatures are ideal applications for the LEON3FT microcontroller. Bridges between different communication standards or interface of an equipment towards a higher level controller or the central On Board Computer (OBC) are also ideal applications for the LEON3FT microcontroller.

The LEON3FT microcontroller can perform

advanced data handling to offload any higher level controller or the central On Board Computer (OBC). By hiding the data handling details the transmitting data volume can be reduced and simplified functionalities and timing requirements are requested to the higher level controller.

The LEON3FT microcontroller integrates several on-chip data bus standards, such as SpaceWire, CAN, MIL-STD-1553, I2C, SPI, UART and can easily provide data packetization for serial communication using standard protocols. The microcontroller can also efficiently replace FPGAs in accomplishing the above functionalities. Generally the FPGA implementation is faster but much more complexity and flexibility can be captured in the software of a microcontroller even with limited processing capability. The correct use of FPGAs in space applications can be complex to achieve and also cost, package size and availability of integrated analog functions can favour the use of a microcontroller with respect to FPGA.

Below are listed a number of possible microcontroller use cases and specific applications.

- Nanosatellite controller
- Instrument Control Unit
- Remote Terminal control
- Mass Memory control
- Propulsion Unit control
- Electric Motor Control

III. MICROCONTROLLER ARCHITECTURE

Figure 1 shows an overview of the mixed architecture of the GR716. The mixed architecture integrates many system functions for easy system integration e.g. power on reset and clock generation.

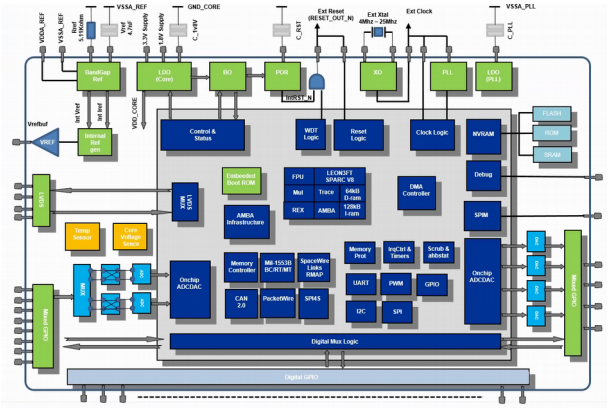

Fig. 1. Analogue Architecture overview

The digital system is shown in figure 2 and the system consists of three AMBA AHB buses, one main system bus, one debug bus and one bus for DMA traffic.

The main bus will include the LEON3FT core connected to a shared on-chip RAM and ROM. The main bus also connects all other peripheral cores in the design as well as the external memory controllers. Several peripherals are connected through two AMBA AHB/APB bridges where the bridges are integrated with the design's DMA controller.

The debug AMBA AHB bus connects a serial UART debug communications link to the debug support unit and also to the rest of the system through an AMBA AHB bridge.

The third bus, a dedicated 32-bit Debug bus, connects a debug support unit (DSU), AHB trace buffers and several debug communication links. The Debug bus allows for non-intrusive debugging through the DSU and direct access to the complete system, as the Debug bus is not placed behind an AHB bridge with access restriction functionality.

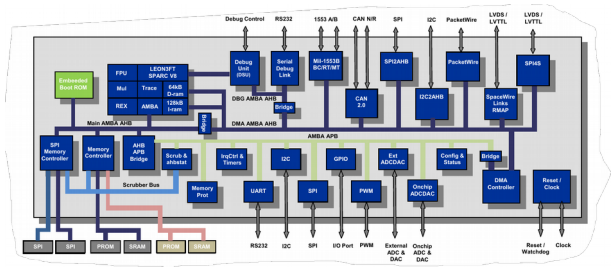

Fig. 2. Digital Architecture overview

The list below summarizes the specification for the complete system:

- System Architecture
  - Fault-tolerant SPARC V8 processor with 32 register windows, 192KiB EDAC protected tightly coupled memory and reduced instruction set
  - Double precision IEEE-754 floating point unit
  - Advanced on-chip debug support unit with trace buffers and statistic unit for software profiling
  - Memory protection units with 8 zones and individual access control
  - Single cycle instructions execution and data fetch from tightly coupled memory
  - Deterministic instruction execution and interrupt latency
  - Fast context switching (PWRPSR, AWP, Register partitioning, irq mapping, SVT, MVT)
  - Atomic operations support
- Memories
  - 192KiB EDAC protected tightly coupled memory with single cycle access from processor and ATOMIC bit operations.
  - Embedded ROM with bootloader for

initializing and remote access
    - Dedicated SPI Memory interface with boot ROM capability
    - I2C memory interface with boot ROM capability
    - 8-bit SRAM/ROM (FTMCTRL) with support up to 16 MB ROM and 256 MB SRAM
    - Support for package option with embedded SRAM/PROM.
    - Scrubber with programmable scrub rate for all embedded memories and external PROM/ SRAM and SPI memories
- System
    - On-chip voltage regulators for single supply support. Capability to sense core voltage for trimming of the embedded voltage regulator for low power applications
    - Power-on-reset, Brownout detection and Dual Watch Dog for safe operation. External reset signal generation for reseting companion chips
    - Crystal oscillator support
    - PLL for System and SpaceWire clock generation
    - Low power mode and individual clock gating of functions and peripherals
    - Temperature and core voltage sensor
    - External precision voltage reference for precision measurement
    - Four programmable DMA controllers with up to 16 individual channel
    - Timer units with seven 32-bit timers including watchdog
    - Atomic access support for all APB registers (AND, OR, XOR, Set&Clear).
    - Peripheral access control
    - Embedded trace and statistics unit for profiling of the system
- Peripherals
    - SpaceWire with support for RMAP and Time Distribution Protocol
    - Redundant MIL-STD-1553B BRM (BC/RT/BM) interface
    - Multiple CAN 2.0B bus controllers
    - Six UART ports, with 16-byte FIFO
    - Two SPI master/slave serial ports
    - SPI4SPACE. Hardware support for SPI protocol 0,1 and 2 in HW for SPI for SPI4SPACE
    - Two I2C master/slave serial port
    - PacketWire interface
    - PWM with up-to 16 channels. PWM clock support upto 200 MHz
    - Up to 64 General input and outputs (GPIO) with external interrupt capability, pulse generation and sampling
    - Four single ended Digital to Analog Converters (DAC), 12-bit at 3MS/s
    - Four differential or eight single ended Analog to Digital Converters (ADC) 11-bit at 200KS/s with programmable pre-amplifier and support for oversampling. Dual sample and hold circuit integrated for simultaneously sampling
    - External ADC and DAC support up to 16-bit at 1MS/s
- I/O
    - Configurable I/O selection matrix with support for mixed signals, internal pull-up/pulldown resistors
    - LVDS transceivers for SpaceWire or SPI4SPACE
    - Dedicated SPI boot ROM support for configuration
- Supply
    - Single 3.3V±0.3V supply or separate Core Voltage 1.8V±0.18V, I/O voltage 3.3V±0.3V

IV. PROCESSOR PERFORMANCE AND DETERMINISM

In order to improve determinism, the LEON3FT microcontroller contains only a local instruction and data static RAM with fixed response times. All EDAC units in the system have the same latency and behaviour in the corrected as in the uncorrected case. This also applies to the CPU, so dynamic SEU handling schemes such as the LEON3FT pipeline restart on error options is not used.

Local instruction RAM tightly coupled to the LEON3FT CPU will be the main memory to execute the software. Due to its direct connection to the CPU, the execution of the software will be deterministic. For applications where full cycle-level determinism is not needed, it will also be possible to execute software from an external SRAM.

The local instruction memory will be implemented using dual-port RAM. The memory's second port will be connected to the main system AHB. This will allow modifying of the local instruction RAM without the intervention of the CPU. The contents of this memory will be protected against SEU errors with EDAC and scrubbing.

If the DMA peripherals and the processor are connected to a shared single-port memory, or to a memory via the same bus, and try to simultaneously access the shared resource then the DMA activity will have an effect on the execution time. On the other hand DMA activity will have no impact on SW execution time by using a dual-port on-chip data RAM and a separate bus for the DMA peripherals. This means that there is a separate access path for the CPU core to local instruction and data RAMs that is unaffected by concurrent DMA activity.

For applications demanding determinism on nested interrupts, a special interrupt handling scheme will be

implemented in software where nested interrupts are allowed to occupy one additional register window. The number of levels of nested interrupts that can be handled without additional timing penalty depends on the complexity of the software implementation.

In the architecture, deterministic interrupt latency will be achieved by:

- Running software (including interrupt handlers) from local RAM and accessing any data needed during the interrupt handling through port separate from AMBA ports.
- Adapting the register window usage (using a flat model) structure to avoid unexpected window over/underflow traps. This is done in the compiler and application code, and most OS code does not need modification.
- The alternate window pointer feature from the SPARC V8E extension to allow window over/underflow handlers to run with traps enabled.
- Register file partitioning to allow partitioning of the register file (the windows) to different "contexts". Contexts can for example be threads to speed up context switching and/or interrupt contexts to dedicate windows to ISRs.

V. LEON/REX AND RUNTIME IMPROVEMENTS

The new LEON/REX alternate window pointer feature (AWP) support and the improved interrupt single vector trap handler (SVT) have been tested and characterized in a series of measurements running on prototype hardware.

By delaying a timer interrupt N clocks into an overflow or underflow trap handling the interrupt latency and interrupt latency jitter as a result of SAVE/RESTORE can be quantified.

Five different software runtime configurations were benchmarked:

- Current BCC SVT
- Improved BCC SVT
- Improved BCC SVT with AWP
- Current BCC MVT
- Current BCC MVT with AWP

In order to understand where the latencies comes from the time from the interrupt is asserted to the time the ISR is reached is split up in three parts presented in the plots below:

- Interrupt assert to acknowledge (assert to first instruction of trap executed)
- Acknowledge to the Interrupt Service Routine (first instruction of trap to first instruction of ISR)
- Total latency (Assert to ISR first instruction)

The worst case interrupt latencies seen when an interrupt is asserted on top of a window underflow/overflow handler are presented in the table below. The highlighted rows are estimates results that can achieved in the LEON/REX environment.

Latency / Config	Assert to Acknowledge		Acknowledge to ISR		Total – Assert to ISR	
	Overflow	Underflow	Overflow	Underflow	Overflow	Underflow
CWP, SVT	134	143	539	281	673	424
CWP, new SVT	70	62	296	166	366	228
AWP, new SVT	**35**	**34**	**202**	**166**	**207**	**200**
CWP, MVT	60	52	262	152	322	204
AWP, MVT	**25**	**24**	**188**	**152**	**193**	**176**

Table 1: Worst case latencies measured

The new LEON/REX architecture also improves the "context" switching by allowing partitioning of the register file (the windows) to different "contexts". By assigning windows to software threads or interrupts the software execution don't have to wait for the LEON3FT processor to store used windows on the stack.

Benchmark on prototype systems shows a large reduction of software execution time of switching "context"

VI. FLAT REGISTER MODEL FOR LOW RESPONSE TIME

Very low interrupt response time can be achieved by utilising LEON3FT microcontrollers large number of register windows. Low interrupt response time can be achieved by using a FLAT register window model. The FLAT register window model eliminates window underflow/overflow-trap and the number of cycles executed with trap disables.

A real-time application compiled with the single register window model (FLAT) using GCC does not issue any SAVE or RESTORE instructions so it executes inside a single window. When a trap is taken (interrupt trap), the current window is decremented with one.

Each unique trap handler is to execute each level of the interrupt nest hierarchy in its own window. Since the FLAT ABI preserves local and input registers as needed, there is no need for the interrupt trap handler to store these. The output registers become the next interrupts input registers and are thus "protected" by the ABI. Only the global registers have to be stored/restored

when jumping between interrupt nest levels. There is room to temporarily store the global registers in the local registers of the trap window.

Examples provided with software environment version 2.0.2 demonstrates that the total latency from interrupt assert to ISR can be as low as less than 28 clock cycles.

Benefits from using FLAT register model:

- Interrupt ack to ISR is 22 cycles (constant)
- Interrupt exit is 15 cycles
- No registers stored to memory in interrupt trap
- No registers loaded from memory in interrupt trap (except to get ISR handler)
- Supports interrupt nesting
- No application specific considerations

Limitations of FLAT register model:

- If SVT is used, then 11 cycles have to be added for the ack to ISR cycles
- Requires one register window per nested interrupt request level

VII. PROGRAMMABLE DMA

Cobham Gaisler has developed a DMA controller able to preform concurrent programmable sequences of data transfers between any on-chip peripherals in the AMBA address space. The DMA controller is able to transfer data both between peripherals, between peripherals and memory and between memory areas. If the accessed memory is internal or external does not matter, as long as the memory is mapped into AMBA address space reachable from the AHB bus where the core is mapped.

The DMA controller has been specifically designed to offload the CPU and provide DMA capabilities to peripherals that do not have an internal DMA engine. The CPU is offloaded by the fact that the peripheral event is directly routed to the DMA controller. By routing events directly to the DMA controller or even directly between peripherals, these interrupts are in effect offloaded from the CPU. These reduce also the number of concurrent interrupts the CPU must handle and that may erode the system determinism.

VIII. PIN-MULTIPLEXING

The device shall be an attractive solution for a wide range of applications. Because of the small package and high number of interfaces, the functionality of the pins must be configurable and the pins must be shared between several peripherals. The number of configurable user pins has been chosen to be 64.

IX. PROFILING AND DEBUGGING

The device provides debug interfaces via the JTAG and UART. The dedicated Debug bus allows non-intrusive debugging since the DSU, trace buffers and performance counters can be accessed without causing traffic on the Processor AHB bus.

The LEON3 statistics unit provides performance counters, with support for filtering, for a large number of events, including:

- Data write buffer hold
- Branch prediction miss
- Total/Integer/Floating-point instruction count
- Total execution count
- AHB bus statistics for Processor AHB bus and Master I/O AHB bus

The interrupt controller in the design supports interrupt time stamping with time stamps interrupt line assertion and processor interrupt acknowledge.

X. PROM-LESS APPLICATIONS

The device provides an easy access for systems that want to avoid having a boot-PROM connected to the device and prefer to upload software remotely. The device can be accessed and remotely configured via SpaceWire, SPI, UART and I2C.

XI. TECHNOLOGY AND PACKAGE

The technology used is UMC 180 nm, using the DARE library from IMEC, and the package is a 132 pin CQFP

XII. SOFTWARE SUPPORT

The architecture is already supported by all operating systems and tool-chains provided by Cobham Gaisler.

XIII. CONCLUSION

The device in development is a SPARC V8 microcontroller that is based on the well known LEON architecture. The device is a prototype for a possible future device targeted at microcontroller applications and will have several new features that are not found in contemporary LEON devices. This includes architectural features to improve determinism, availability of the device in a low pin-count package, and support for the reduced instruction set.

Microchip ATMX150RHA

European Mixed Technology for Advanced Designs

SAMRH71

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I. Introduction

Microchip Technology Inc. is a leading provider of microcontroller and analog semiconductors, providing low-risk product development, lower total system cost and faster time to market for thousands of diverse customer applications worldwide. Microchip offers outstanding technical support along with dependable delivery and quality.

Thanks to Atmel acquisitions, Microchip is now one of the leading company in microcontroller and processor based on ARM core through long partnership established with ARM since 1995. Microchip has introduced ARM 32 bit solutions in most of the applications today: automotive, industrial, consumer and home appliance for example. With its current SAMV71-RT and SAMRH71 developments, Microchip is currently introducing the performance of the proven ARM solutions for space market.

Thanks to the experience of the microcontrollers available for the automotive and Aerospace markets and thanks to its European ITAR-Free mixed ATMX150RHA technology Microchip is capable to offer not only digital devices to the Space market but also complex system on chip integrating analog functions.

In addition to the development of the product itself, Microchip is owner of the complete supply chain that guarantees parts delivery to applications with high quality and reliability constraints.

Taking the benefit from its best in class microcontroller families proposed to consumer and automotive markets, reusing the knowledge and development techniques from the technical teams that made from AVR and currently ARM architectures worldwide successes, this combined with the hardening expertise of the Aerospace and Defense team, Microchip is capable to propose optimized mixed development perfectly suiting the constraints of space applications.

II. Space Technologies Unrivalled Asset

For nearly 30 years, the Microchip Aerospace division has been providing rad-hard digital ASICs for the most critical applications.

In order to meet the needs of next-generation satellites and launchers, we are offering advanced new ASIC technological nodes for both standard product development and ASICs. The two current running nodes are the followings:

- ATMX150RHA is a mixed-signal ASIC with non-volatile memory and high-voltage options, based on SOI 150nm technology
- AT65RHA offers a high level of system integration and increased computing power. The device is designed in 65nm technology, with up to 50 Mgates and more embedded features such as very high-speed serial links

Over the aerospace ages, Microchip has been continuously deploying advanced technologies for the space markets:

- 180nm (internal name AT58K) available at LFoundry (France, Rousset) and UMC (Taiwan), used by Automotive and Microcontrollers
- 150nm embedded EEPROM (internal name AT58K85) available at LFoundry (France, Rousset) and UMC (Taiwan), used by Automotive and Microcontrollers.
- ***150nm (internal name AT77K SOI) developed with Automotive with first qualification since Nov. 2013 at UMC (Taiwan) and under Space assessment by Microchip Aerospace under a running CNES contract.***
- 90nm UMC process used by Microcontrollers with a wide catalog of silicon proven digital and analog lib
- ***65nm ST process used for advanced ASICs***

All these processes have been especially refined for use in space applications. They have all been deployed with respect to the more stringent requirements from space domain:

- -55°C to +125°C for space
- Quality level (automotive is running below 1ppm in stable production), proving a process fab completely under control
- Radiation Management – TID, SEL and SEU

Microchip Corp. still have a full team dedicated to process definition and process installation in foundries. The fact that Microchip Corp. handles negotiation with foundries give more power in the negotiation and enable Microchip Aerospace to use qualified and validated process. The production volume for Aerospace is not sufficient to lead to good fab out quality and to ensure a sufficient lifetime for the process.

III. Mixed Oriented Developments

Design tools being more and more complex and more and more expensive, Microchip has developed for all its technology offering complete framework to be used by developers. While used for all its internal development, Microchip Aerospace is considering how to give access at a reasonable price to its tools in remote access, through a secured line.

The growing complexity of the devices and also the use of analog cells which must be hardened have led Microchip A&D to introduce radiation simulation in its flows. It is still on R&D level but already leads to interesting results in terms of optimization of design rules and research of critical nodes in analog cells considering SEU and SET.

A full set of library is hardened (standard cells, 3.3V IOs, hard memory blocks and specific cells and fully characterized in space military range up to 145°C Tj. This rad-hard performance is assessed and validated using PM, TCV and SEC methodology compliant with MIL and ESCC standards. A final packaging (including in the Design Kit DK) is managed with all library models (netlist generation: .lef, .cir .gds, .lib...).

For all its technologies, dedicated design flows are in place to optimize the development of the products.

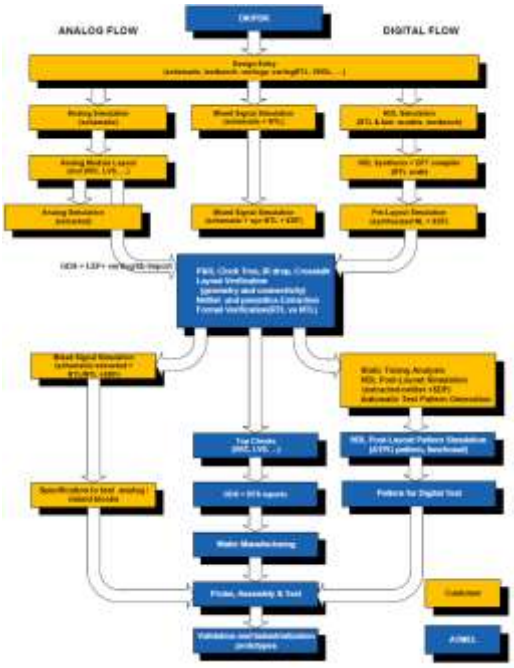

Figure 1. ATMX150RHA development Flow

The design flows presented here are the flows currently used for the ATMX150RHA developments for both the Microchip internal device development and the ASIC designers.

Microchip is continuously committed to maintain and support this design flow for space applications.

IV. SAMRH71 - ATMX150RHA MCU

While some space application can accept the use of COTS and radiation tolerant devices due to limited radiation requirement constraints, there are still applications for which use of devices with high level of robustness against radiation effects is necessary. The ATMX150RHA technology has been especially designed to allow development of those devices requiring the highest level of radiation hardening.

The SAMRH71 presented here after is the first development of a complex standard product deployed over the ATMX150RHA. The goal of this device is to propose a highly integrated processor integrating basic analog functions.

The SAMRH71 is a high-performance microcontroller based on the 32-bit ARM® Cortex®-M7 RISC (5.04 CoreMark/MHz) processor with Floating Point Unit (FPU). The device operates at a maximum speed of 100 MHz and features up to 128 Kbytes of Flash, 16 Kbytes of dual cache memory, more than 1 Mbyte of embedded SRAM (364 Kbytes of TCMRAM and 1 Mbyte of multiport SRAM), and external memory interfaces EEPROM, Flash, SRAM, SDRAM (with embedded Error Correction Code) and QSPI. It is available in a 256-pin package.

The SAMRH71 is ideal for many space applications by integrating deterministic features (timers), analog controls (PWM), data analysis features (Embedded SRAM memory and external memories) and various space reception/ transmission links to vehicle data, such as SpaceWire and 1553.

The device peripheral set includes Ethernet 10/100, two CAN-FD, up to 10 FLEXCOMs (USART/UART/SPI/I2C), as well as high-performance crypto-processors SHA and TRNG.

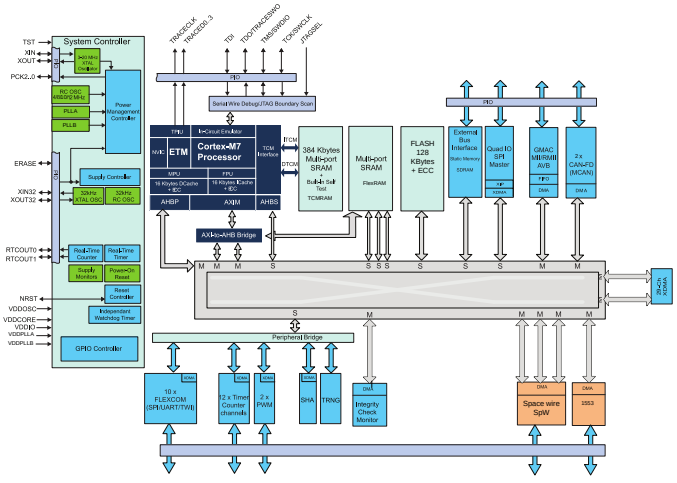

Figure 2. SAMRH71 Architecture overview

The SAMRH71 devices are high-performance Space microcontrollers that target critical missions for on-board computing, sensor management application and connectivity applications. They embed a concurrent AMBA system bus with advanced DMA features to perform several tasks at the same time, without excessive processor workload. The SAMRH71 devices are implemented on the ATMX150RHA process that has been specially designed for space applications by implementing on-chip transient and permanent error detection and correction.

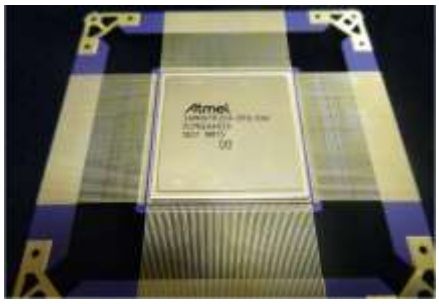

Figure 3. SAMRH71 Processor

Based on the same reference architecture as the COTS and RAD-TOLERANT, the RHBD device optimized both at feature level and at technology level to offer the best in class robustness for deep space missions.

The RHBD devices relying on a design fully dedicated to the space applications, it is possible to embed space specific features and also to improve some interfaces to increase the robustness of standard IPs. The SAMRH71 is for example an opportunity to integrate on-chip the SpaceWire and 1553 interfaces that we can't find in any component originated from COTS.

As an extension to the mechanisms already available in the automotive version of the device, the re-design for a RHBD version allows to optimized the on-chip error management by adding/optimizing the ECC required on all the memory interfaces. In the SAMRH71, the FLASH, the internal RAMs, the TCMs and the external bus interface have all been upgraded to ensure the highest level of safety.

The main constraint for space applications remains the sensitivity to radiation effects. Improvement of the radiation hardness of the device is performed using especially hardened cells. The ATMX150RHA library is used for the development of the SAMRH71.

In order to build-up the system controller of the device, the SAMRH71 relies on a large set of ATMX150RHA analog IPs that allow advanced integration and internal automation.

From the memory point of view, the SAMRH71 contains 128Kbytes of embedded Flash with build in ECC (up to 2 errors correction). This feature is based on 4 instances of the 32K non-volatile memory block available from the ATMX150RHA.

For integration of the system controller, the SAMRH71 has been built around the following analog functions

- Built-In Power-on-Reset (POR) using the ***POR18RHA 1.8V Power On Reset cell***
- Crystal or ceramic resonator oscillators: 3 to 20MHz main oscillator with failure detection - ***OSCXT20MRHA 3-20 MHz Crystal Oscillator***
- High-precision 4/8/10/12 MHz factory-trimmed internal RC oscillator for device startup. In-application trimming access for frequency adjustment - ***OSCRC10MRHA 4/8/10/12 MHz programmable RC Oscillator***
- 32.768 kHz crystal oscillator - ***OSCXT32KRHA 32 kHz Crystal Oscillator***
- 32 kHz (typical) RC oscillator as source of low-power mode - ***OSCRC32KRHA 32 kHz RC Oscillator***
- A 300MHz PLL for system clock – ***PLL400MRHA cell*** configured for an optimal operation at 300MHz
- A 200MHz PLL for peripherals – ***PLL400MRHA cell*** configured for an optimal operation at 200MHz

In addition to its advanced architecture, the SAMRH71 microcontroller takes the benefits of the Microchip ATMX150RHA technology especially developed for manufacturing of space components. Thank to this technology, the SAMRH71 can offer a built-in SEL immunity up to 60MeV and a 100KRad capability.

For the RHBD, the screening and qualification process are fully compliant with the QML/ESCC processes.

As a derivative of the SAMRH71, Microchip is specifying a new device that will offer much more advanced analog function on top of the digital platform.

This new device will consist in the integration of an advanced analog front-end for management of the analog inputs/outputs. The target is to embed the following additional analog features:

- A 8 channels multiplexer – ***MUX8RHA 8 Channels Analog Input Multiplexer***
  The multiplexer is used to provide up to 8 different sources to the ADC input. This allows interconnection of multiple sources to be sampled by the ADC.
- A 12-bit ADC - ***ADC12RHA 12bit Cyclic Pipelined ADC***.
  This ADC has a selectable single-ended or fully differential input and takes benefits from a 2bit programmable gain. It employs a cyclic pipeline algorithm based on a single multi-bit stage architecture to achieve sampling rates up to 1Ms/s while consuming very low power. The power consumption of the analog core may be adjusted externally through a 2bit bias control bus providing possibilities for smart optimization of power and effective resolution relatively to the application speed request.
- A 12-bit DAC – ***DAC12RHA 2MSPS Modular DAC***.
  This DAC is modular and offers up to 4 analog output sample-and-hold circuits selectable via 2bits to address the analog voltage to one desired output channel and a separated 'mode' bus enables to power on/off output channels individually

The user can choose between single ended or fully differential sample and hold circuits for each of the 4 output channels.

V. SOFTWARE, TOOLS AND SERVICES

All those solutions based on same SoC Architecture can benefit from the same free ecosystem in term of software libraries and tools but also in term of services and hardware support. Here are the key benefits and common asset shared by this product family from COTS to RHBD device:

- Hardware environment & Tools for software development and system debug
- Software package to ease design phase with hardware abstraction layer
- Operating system reference porting through partnership business model
- Experience from industrial and automotive reference design through applications note
- Hands on, on the field training with support from our expert FAE. Possible onsite training session

For Software and Hardware tools, those solutions share the same environment set up:

- Same Xplained board for COTS and Rad Tolerant device
- Same Software free development & debug package for all versions : Studio/MPLAB tools suits
- Same ICE tools debugger & programmer for all versions



All solutions benefit from the same software libraries and same applications note database through Studio /MPLAB software suite. The software package contains ready to use example projects for Microchip studio. Projects are available for most of the peripherals of the SAMV71

- Each demo comes with detailed documentation
- samv71_softpack_1.5_for_astudio
- Exist for other software environment (IAR EWARM, KEIL, XULT GNU)

All solutions can use state of the market tool suite for a more complete & qualified tool chain through the following providers:

IAR SYSTEMS KEIL Tools by ARM

Some OS port are also available for those targets, here below some examples:

ERTOS µLinux Micrium seggen HCC expresslogic

Porting for OS more used in the Aerospace applications is also ongoing: RTEMS, VxWorks and Xstratum.

To facilitate hardware design ease the transition between the different versions of SAMV71, same pin out distribution is kept between plastic and ceramic versions for same number of pins. With this approach, COTS plastic version can be used in the early stage of the project before moving for example to ceramic space grade rad tolerant part with a dual footprint PCB design.

VI. CONCLUSION

The ATMX150RHA ITAR-Free Mixed technology offers all the facilities to facilitate the development of performant complex system on chips.

With its standard digital cells library, its advanced IO library and a large set of analog ready-to-use IPs, the ATMX150RHA proposes a cost effective complete offering perfectly suited for performant space dedicated developments.

Prototype of a Multi-Mode C-Band Capable 12-bit 1.5/3/6 GSps Quad ADC in Flip-Chip Non-Hermetic Technology

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Abstract

Teledyne e2v has developed a new 12-bit 1.5/3/6 GSps quad ADC on STMicroelectronics BiCMOS9 technology, and assembled in Flip-Chip non-hermetic technology.

This device is C-band capable embedding a cross point switch for flexibility and chaining capabilities for multi-component synchronization and clocking.

The BiCMOS technology used features 130nm CMOS and SiGeC NPN HBT bipolar technology (Ft/Fmax = 166/175 GHz).

The device is assembled in a non-hermetic flip-chip CBGA package using HiTCE glass ceramic material in order to reach optimized RF performance and higher pin density.

I. Context

Satellite-based applications like telecommunication, earth observation and navigation increasingly demand more flexibility [1] in terms of utilized capacity, performance and mobile usage. At the same time satellite constellations are getting more complex in order to meet these flexibility demands [2]. Emerging satellite systems therefore use intelligent communication payloads based on capable on-board signal processors. These should be able to interface effectively to complex antennas, flexibly generating hundreds of traffic beams or inter-satellite connections and handling multi-GHz processed bandwidth per port.

Payload systems performance is directly linked to the performance of components used at every stage of the signal chain within the satellite payload: starting from the reception antenna followed by low-noise amplifiers to the final transmission antenna, through the analogue-to-digital conversion, digital processing and the digital-to-analogue transfer stages. Two components are of key importance here because they have a direct effect on signal quality at receive (Rx) and transmit (Tx) side and therefore are key enablers of the global system performance: the analogue-to-digital and digital-to-analogue data converters (ADC and DAC). Within this context, Teledyne e2v has developed a new quad 12-bit 6GSps ADC in the frame of a European H2020 program. This ADC is capable to reach a high integration level with more channels on a board, low power consumption, large bandwidth and high dynamic performance.

This paper is composed of six parts. A first section will present the market trends in which the ADC has been developed for. Then an overview of the product is proposed and details of the multiple-component chaining features are presented. The fourth section is dedicated to the packaging technology used for the ADC. Then radiation hardening techniques employed are revealed. In the last section, first measurement results are shown.

II. Market Trends

The space market evolves with a growing variety of reliability requirements and an increasing variety of system architectures as the usage of digital signal processing techniques on microwave signals continuously expands its range of applications in space systems [3].

Consequently, the prototype ADC is built to be delivered in several reliability grades. And from the onset, this new ADC has been defined to be a multi-purpose device designed and architected to digitize broadband microwave signals in a broad variety of system implementations. Its unique Cross Point Switch in the input stage is a fundamental part of its multi-purpose nature.

Additionally, the C-Band capability of the ADC supports the market trend to simplify RF receiver signal chains with direct digitization of signals in P-, L-, S- and C-band, and high IF implementations for system operating in higher bands.

As a result, the engineering efforts needed to adopt a new ADC can then be leveraged on a broad variety of system architectures, including in telecommunications payloads, UWB or multi-band SAR [4], broadband uplink modems, altimeters, high accuracy Lidar systems, GNSS systems and other space payload instruments.

This also contributes to address the growing expectations of short time to market in the space industry.

III. Product Overview

The prototype called EV12AQ600 presented in this paper is a quad channels 12-bit 1.5 Gsps ADC. It is based on STMicroelectronics BiCMOS9 technology featuring 130nm CMOS and SiGeC NPN HBT Bipolar technology (Ft/Fmax = 166/175 GHz) [5]. The built-in Cross-Point-Switch (CPS) allows multi-mode operation with the capability to interleave the four independent cores in order to reach higher sampling rates. In 4-channel operating mode, the four cores can sample, in phase, four independent inputs at 1.5 Gsps. In 2-channel

operating mode, the cores are interleaved by 2 in order to reach 3 Gsps sampling rate on each of two inputs. In 1-channel operating mode, a single input is propagated to each of the four cores which are interleaved by 4 in order to reach a sampling rate of 6 Gsps. Figure 1 shows the CPS configuration: the ADC inputs (from IN0 to IN3) to the ADC cores (from core A to core D). This high flexibility enables digitization of IF and RF signals with up to 3 GHz of instantaneous bandwidth, up to 6 GHz.

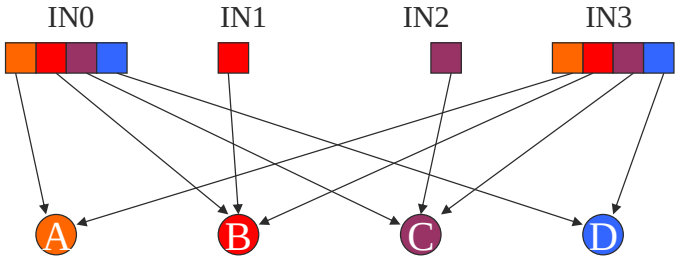

Figure 1: CPS Configuration

Each channel is composed of a single core 4 stages folding interpolation ADC sampling at up to 1.5GSps. Based on an innovative architecture without interleaving, it provides high spectral purity. It offers an analog input bandwidth (-3 dB) of up to 6 GHz with two selectable configurations to optimize SNR performance when working in lower Nyquist zones or linearity performance in higher Nyquist zones. With an extended input bandwidth above 6 GHz the EV12AQ600 allows sampling of signals directly in the C-band (4-8 GHz) without the need to translate the signal to baseband through a down-conversion stage. Figure 2 shows the block diagram of the ADC.

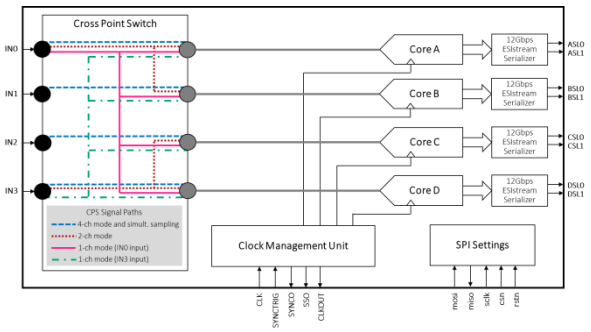

Figure 2: Block diagram

The ADC uses 8 low latency serial lanes at 12 Gbps with ESIstream protocol [6]. Serial lane rate is linked to sampling clock frequency by a ratio of 2, allowing no need of extra PLL, avoiding extra overhead with fractional ratio and being more robust against radiation. The ESIstream protocol is a 14b/16b encoding based on 14 scrambled bits along with 2 overhead bits: clock bit and disparity bit. Applied to the EV12AQ600, the 16 bits frames are as follows (cf. Figure 3):

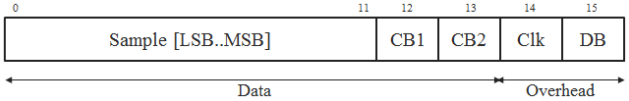

Figure 3: ESIstream frame with EV12AQ600

DB is the disparity bit, CLK the clock bit, CB1 and CB2 are control bits of the ADC and bits 11 to 0 contain the ADC sample. Bits 13 to 0 are scrambled using an LSFR (Linear Feedback Shift Register) that generates the PRBS (Pseudo-Random Binary Sequence).

It also features a novel synchronization method to ease the synchronization of a large number of ADCs. The device is controlled through an SPI interface. All sensitive areas of the device have been triplicated to increase robustness. This includes, but is not limited to, clock circuitry and SPI registers.

IV. Multiple-Component Chaining Features

A method for synchronizing multiple data converters is embedded, already deployed on EV12AD550 [7]. It is based on a daisy chain approach between data converters and one or multiple processing units, i.e. Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC). A synchronization pulse is propagated between data converters. The Figure 4 shows a diagram of the interface between multiple data converters and a processing unit.

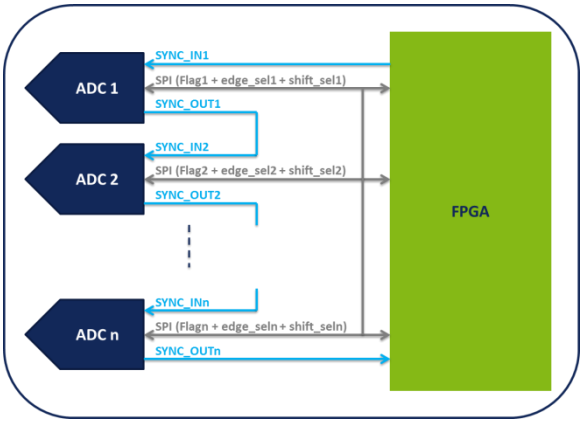

Figure 4: Multiple-device synchronization system overview

Three settings are necessary to manage or configure each ADC:

- Flagx: this signal indicates whether the synchronization pulse is in a meta-stability zone in regards to the clock of the data converter;
- Edge_selx: this signal is configured to choose which edges of the clock of the data converter is used to recover the synchronization pulse;
- Shift_selx: this signal is configured to add a certain number of clock cycle delays to the synchronization of the device after the pulse has been recovered by the data converter

The SYNC_OUT is a copy of the SYNC_IN that is sampled on the reference clock common to all data converters to ensure repeatability of the timings between power-ups and each time the synchronization process is started. Using the three settings, and a training of the system, the different data converters can be synchronized.

Calibration procedure is described in [8].

This synchronization process brings multiple advantages to systems having large count of channels:

- The parameters are accurate between power-ups, synchronization process and printed circuit board based on the same design. This is useful to develop industrial scale system, as the determination of the parameters can be done during prototyping only;
- This method relaxes all layout constraints on the SYNC signal. This means that it can be propagated on one board, or between multiple boards through a backplane which is unavoidable when systems have hundreds of channels to synchronize;
- This method is also compatible with different implementation. The daisy chain shown in Figure 4 is one of them but a tree configuration is possible as well as any hybrid between the two. This brings flexibility to the system;
- Finally, this method does not impact the sampling clock performance. This is essential as some synchronization method adding delays on the sampling clock can degrade its jitter and thus degrade the SNR (Signal to Noise Ratio) performance of the data converters. Communication and wideband radar are two applications which performances are limited by SNR.

In terms of limitations, there are still layout constraints on the reference clock that needs to be time aligned at the input of all the data converters. However, method exists to help either through digital processing or using a slow reference and PLLs to generate the fast clock fed to the high-speed data converters.

Speed wise, this method is limited by the setup and hold time and jitter achievable compared to the reference clock.

The ADC has also an output clock signal provided by the circuit as a clock reference to other ADCs or DACs. This signal is the image of ADC input clock through a buffer, adding some jitter (less than 60 fs rms) to the reference clock. It can be used for ADC chaining (up to 4 components) or clocking a DAC on a same PCB, without significant impact on total converter clock jitter. Clock chaining with multiple ADCs or a DAC is illustrated on Figure **5**.

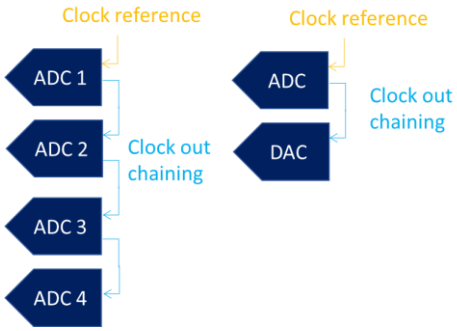

Figure 5: Clock chaining scheme

V. Packaging Technology

For the EV12AQ600 ADC, the choice of FlipChip technology appeared naturally because it is an efficient, effective and reliable device packaging solution.

Indeed, one of the inevitable side-effects of the increased maximum sampling rates and input bandwidth is that the classic configuration of an edge wire-bonded die attached within a package cavity and enclosed by a hermetically sealed lid is no longer feasible, due mainly to the inherent losses and inductances of the bond-wires and their limited distribution to the die.

EV12AQ600 is realised on flip-chip bumped die featuring area-attach. The intermediate multi-layer substrate which accepts the die on one surface and hosts solder balls on the other is fabricated using Low-Temperature Co-fired Ceramic (LTCC) permitting the use of noble metal conductors (Copper instead of Tungsten). Use of conductors made of Copper for example means that the losses at microwave frequencies are minimised and more accurate ultra-broadband impedance matching is possible where required. LTCC also features a high coefficient of thermal expansion which allows the accommodation between the expansion rates of the die and that of the PCB. This condition is a prerequisite for a highly reliable solder joint capable of surviving many hundreds of thermal cycles.

On the bottom side of LTCC substrate, 323 lands allow for solder ball attach. Thus a CBGA323 BGA package is achieved.

A copper heatspreader (Nickel finished) is attached on top with thermal interface material glued to die backside. Walls of the heatspreader are also glued to substrate with venting holes.

Package dimension is 16x16 mm and the ball pitch is 0.80 mm. Pictures of top and bottom views of the packaged device are shown on Figure **6**.

Figure 6: Top and bottom views of packaged device

Package configuration is shown on Figure 7.

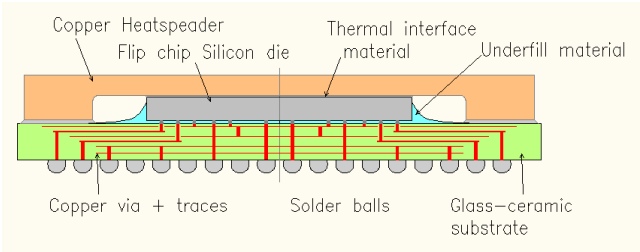

Figure 7: Cross section view of packaged device

Extensive 3D electromagnetic (EM) simulations have been performed using full-wave simulator ANSYS HFSS [9]. These EM simulations enable to predict radio-frequency effects and to assess the target specifications, such as insertion loss from the solder balls to the die bumps, return loss at the

input of the package, crosstalk between inputs, between outputs and between clock input and output. On Figure 8 is shown the 3D view of a part of the package modeled (analog inputs).

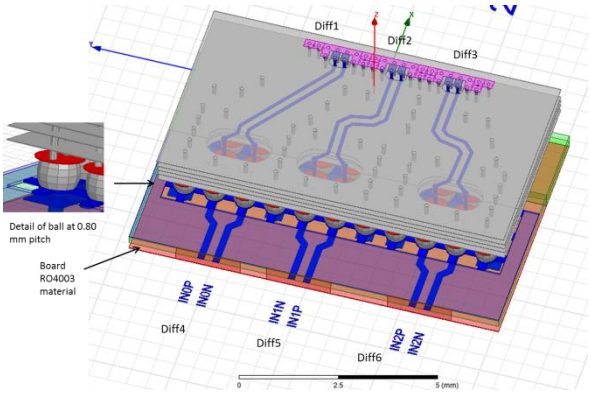

Figure 8: 3D view of a simulated analog inputs

As compared to classic package configuration (ie. wire bonded, hermetic), the EV12AQ600 comes with 2 new features:

- Flip chip
- Non-hermetic

Whereas this type of configuration has been used for many years in other applications, its adoption is quite new for space ones. Apart from technical challenges [10], an important concern was that, a few years ago, Space Standardization did not bring provisions for flip chip devices. Non hermetic flip chip has been introduced in US standards (MIL-STD-883 & MIL-PRF-38535) at the end of 2013 by the addition of the now famous class Y. At the same time, a Working Group (WG) was set up by ESA in order to introduce non hermetic flip chip in ESCC standards (ESCC 9000 & ESCC 2269000). This WG gathered attendees from Agencies, component manufacturers & end users. Those entities were represented by Quality Assurance and / or packaging experts, in order to address both standardization and technical concerns.

Teledyne e2v was granted the leadership of the WG. The group quickly agreed the following guidelines:

- Inclusion of non-hermetic / flip chip in existing ESCC standards (vs inception of fully new standards)
- When possible, consistency with European hybrids & US microcircuits standards, in order to avoid duplication of similar tests
- Addition of requirements for passive add-ons, which are very often associated with flip chip devices

The WG started its work mid 2014 & submitted a proposal to ESCC during fall 2015. Beginning of 2016, this resulted in the publication of ESCC 9000 issue 8 [11] & ESCC 2269000 issue 5 [12].

This achievement has played an important part in the adoption of flip chip for space, through a common reference and language, between agencies, component manufacturers & end users.

VI. Radiation Hardening

ST BiCMOS9 technology does not propose rad hard library. However, first radiation hardened protection assessment has been obtained on EV12AD550 using the same technology and a similar architecture.

Designing a rad hard component requires special cares both in product architecture definition, cells designs, layout implementation in order to either limit the impact of radiation event and/or decrease the event occurrence by increasing the required critical charge threshold to produce an event [13].

A. Layout for radiation considerations

Specific implementation rules have been defined and adapted case to case to limit ionization leakage current propagation into parasitic path.

Some examples of adopted rules:

- NMOS transistor isolation with a P+ guard ring.
- Bulk tie have largely been implanted in order to limit leakage current between transistors.
- Minimization of bulk resistance by placing bulk tie as close as the active device.

For the prevention of latchup, the following rules have been used:

- A deep NWELL NISO is used to isolate the digital blocks and extra substrate ties are added to standard cells to collect radiated charges (cf Figure 9).

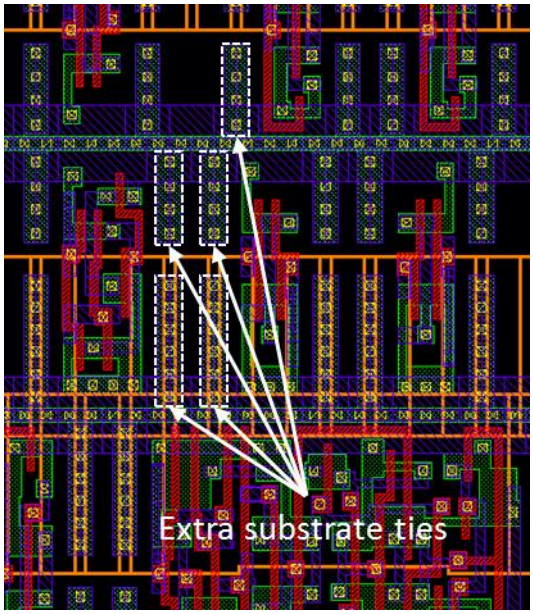

Figure 9: Detail of digital block circuit

- Enlarging minimum space between p and n zones in all analog part and adding deep NISO isolation to reduce radiated charge accumulation, isolating bulk including rail power supplies (cf. Figure 10).

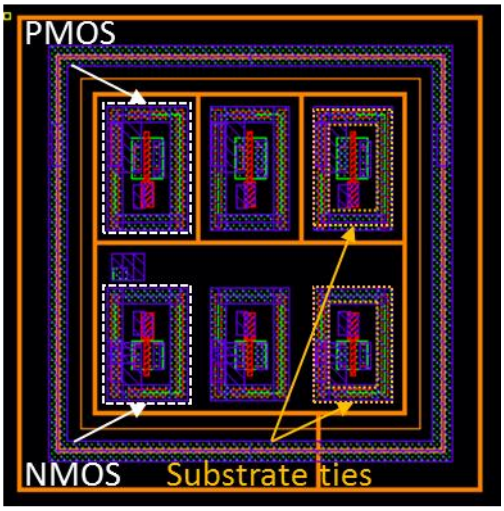

Figure 10: Detail of analog block circuit

- Reduce the serial resistance of the parasite thyristor to prevent from activation.
- Multiply the number of bulks and substrates ties
- Larger of guard ring should not be too much resistive i.e. it is mandatory to not open them.
- Increase minimum distance between guard rings.
- Between NWELL and PWELL it is necessary to put a double guard ring connected to VDD/VSS.

A specific Design Rules Check tool has been developed by Teledyne e2v for superior automation.

B. Design protection approaches

Design protection techniques to prevent occurrence of events include: large drive current of transistors, large transistors, large capacitance.

1) Analog architecture

When possible, analog redundancy has been used. That consists of parallelizing "n" times a circuit and connecting replicated nodes through a resistance to a common node, so that the perturbation effect is divided by "n".

In order to increase node time constant and then increase the parasitic critical charge required to produce a SET, Miller capacitance and/or resistance have been used.

Analog RC filtering is implemented to reduce SET.

2) Digital architecture

The protection of digital blocks is one of the most challenging topics as no rad hard libraries are available. In addition to the layout protection listed above, architecture is optimized by implementing:

- TMV (triple redundancy voting)
- Anti-glitch structure.
- A special mode (SE Protect) has been implemented to strengthen the radiation immunity to Single Event Functional Interrupt (SEFI).

However the drawback of all those protections is that they constrain the performances in terms of power consumption, speed, and size. That is why a specific study has been done on each block in order to protect the most critical nodes.

EV12AQ600 robustness to radiation will be shortly tested with two test campaigns:

- Total Ionizing Dose (TID): due to a BiCMOS process and to test the Enhanced Low Dose Rate Sensitivity (ELDRS), the ADC will be tested at a Low Dose Rate (LDR) of 36 Rad/h, up to 150Krad(Si)
- Single Events (SE): the Texas A&M University (TAMU) facility will be used to evaluate the Single Event Effects (SEE). The Single Event Latch-up (SEL) will be tested up to 80 MeV.cm²/mg without tilt. The Single Event Transient (SET), the Single Event Upset (SEU) and the Single Event Functional Interrupt (SEFI) will be tested up to 92 MeV.cm²/mg (80MeV.cm²/mg with a tilt of 30°).

VII. MEASUREMENT RESULTS

Figure 11 to Figure 13 show typical FFT spectra at frequencies varying from 100 MHz to 2980 MHz. SFDR performance as high as 75 dBFS is obtained at full power in the first Nyquist zone. Lowering input power allow reaching more than 70 dBFS SFDR performance from DC to 6 GHz frequencies.

The EV12AQ600 ADC shows an extremely good spectral purity. As can be seen on Figure 13, the harmonic tail of a 749.9 MHz signal decreases to noise floor very rapidly and no spurs remain in the spectrum.

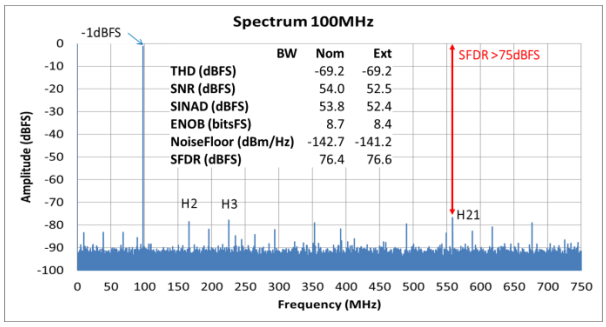

Figure 11: Typical -1dBFS spectrum and FFT computation results @ Fin=100 MHz.

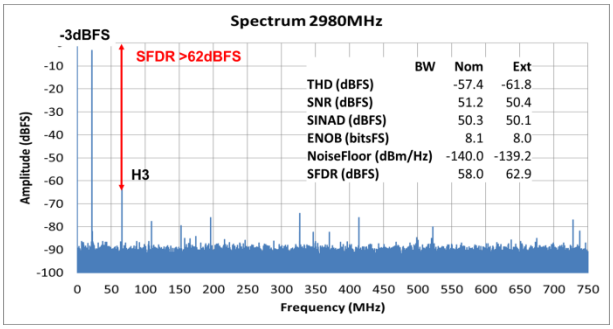

Figure 12: Typical -1dBFS spectrum and FFT computation results @ Fin=2980 MHz.

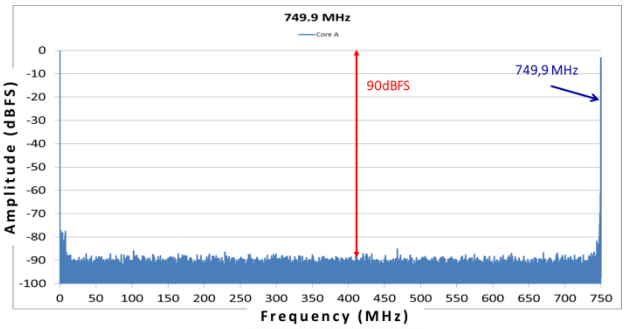

Figure 13: Spectral purity ≥ 90 dB

Figure 14 to Figure 19 show SFDR, SNR & ENOB performance for both -1dBFS and -12dBFS input powers over the full bandwidth (DC to 6 GHz).

The two bandwidth modes available in EV12AQ600 allow adjusting the performance depending of the result sought.

On the one hand, Extended Bandwidth allows for better linearity SFDR for large signals (cf. Figure 14). On the other hand, Nominal Bandwidth, by reducing jitter effect will strongly improve SNR and ENOB for small signal amplitudes (Figure 17 and Figure 19).

The spectrum and performance of a 100 MHz sine wave signal digitized in interleaved mode are shown on Figure 20.

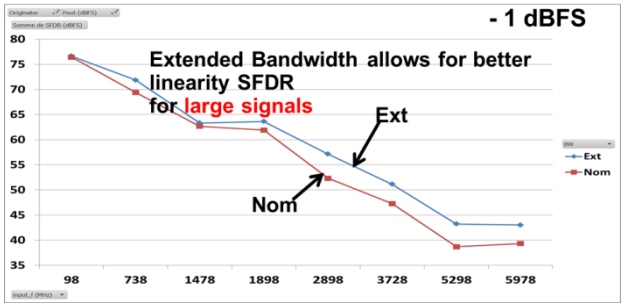

Figure 14: SFDR performance vs frequency @-1dBFS

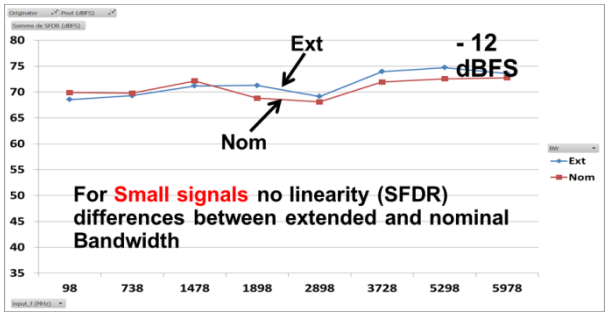

Figure 15: SFDR (dBFS) performance vs frequency @-12dBFS

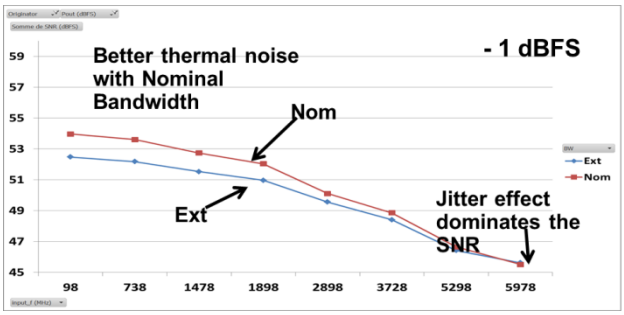

Figure 16: SNR (dBFS) performance vs frequency @-1dBFS

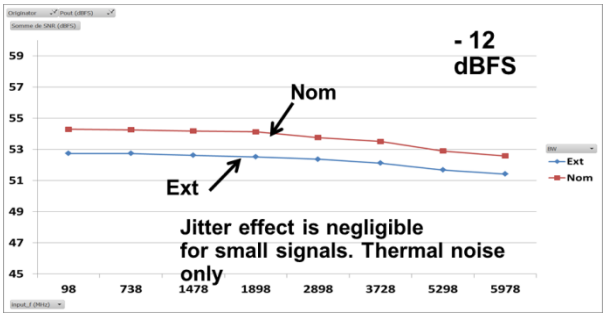

Figure 17: SNR (dBFS) performance vs frequency @-12dBFS

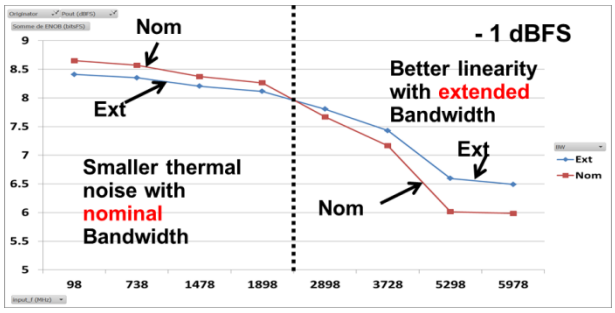

Figure 18: ENOB performance vs frequency @-1dBFS

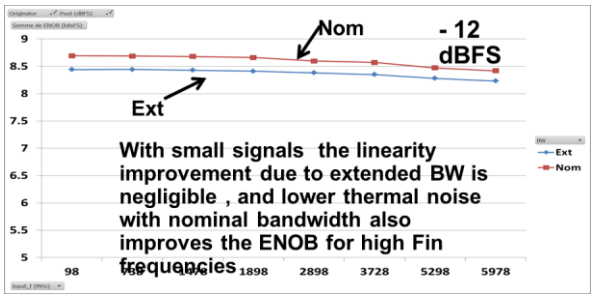

Figure 19: ENOB (Bit_FS) performance vs frequency @-12dBFS

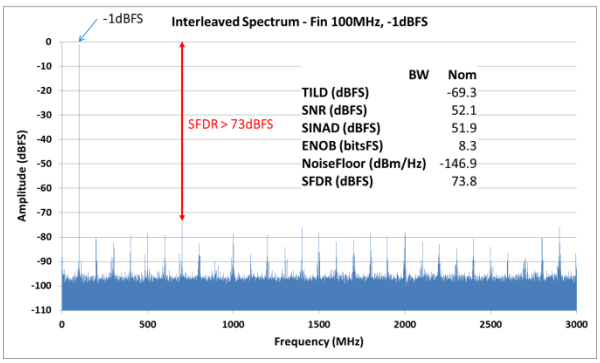

Figure 20: Spectrum and performance in interleaved mode

VIII. Conclusion and Perspectives

A prototype of a quad channels 12-bit 1.5 Gsps ADC has been presented. The ADC is a multi-purpose device designed and architected to digitize broadband microwave signals in a broad variety of system implementations. Its unique Cross Point Switch in the input stage is a fundamental part of its multi-purpose nature to address the growing flexibility demand of next generation satellite systems.

First measurement results have been presented. Further results will come in the near future to cover the entire characterization plan.

In addition, the ADC can be accompanied by a custom interleaving error correction IP provided by Teledyne SP Devices team. It will enhance the performance of the ADC in 1-channel mode (4 cores interleaved) in order to reach unprecedented performance for such a multi-purpose ADC.

IX. Acknowledgments

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This INTERSTELLAR collaborative project led by Teledyne e2v sees a fruitful partnership with Airbus Defense and Space ADS (UK), Fraunhofer IIS (D) and Thales Alenia Space TAS (FR).

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CORRELATORS FOR INTERFEROMETRIC RADIOMETRY IN REMOTE SENSING APPLICATIONS, A SCALING PERSPECTIVE

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INTRODUCTION

Remote sensing in the radio spectrum is becoming increasingly important for both metrology and climatology as well as for interplanetary missions [1]. Correlators are used for performing interferometry for both spectral analysis and for aperture synthesis imaging. CMOS technology scaling has made digital correlators increasingly competitive by both increasing their bandwidth capability and by reducing power dissipation per operation.

Autocorrelation is an efficient way of performing spectrometry. It was invented in 1963 [2] and used for discovering the first interstellar OH molecule [3]. Since then it has been widely adopted and used in, e.g., the Odin satellite launched in 2001 [4]. The autocorrelator for Odin was among the first to be optimized for power efficiency. One of the advantages with autocorrelation spectrometers is their flexibility; the bandwidth and, hence, spectral resolution can be modified by changing the sampling frequency. Taking the Fourier transform of the autocorrelation function, the power spectrum is calculated, using the Wiener-Khinchin theorem [5].

A relatively new application for correlators in remote sensing is aperture synthesis. Here, imaging is performed using an array of many antennas and performing cross-correlation between antenna pairs (baselines), sampling the UV-plane. By using the inverse 2-D Fourier transform, a brightness temperature image is achieved. While aperture synthesis is nothing new[1], the first and so far only aperture synthesis array implemented on a satellite was the Microwave Imaging Radiometer with Aperture Synthesis (MIRAS) launched to low Earth orbit (LEO) with the Soil Moisture and Ocean Salinity (SMOS) satellite as late as 2009 [6]. Several initiatives of placing an aperture synthesis imager in geostationary orbit (GEO) is currently ongoing; in the USA with the Geostationary Synthetic Thinned Aperture Radiometer (GeoSTAR) [7], in Europe with the Geostationary Atmospheric Interferometric Sounder (GAIS) [8], and in China with the Geostationary Interferometric Microwave Sounder (GIMS) [9].

While the time-limited, digital cross-correlation function, as shown in Eq. 1, is performed on two signals, f and g, autocorrelation is the cross-correlation of a signal with itself ($f = g$). The signals are multiplied and averaged over a time, M, for a number of different time delays (lags), n, applied to one of the signals. Here, f^* is the complex conjugate of f.

$$(f \star g)[n] \stackrel{\text{def}}{=} \sum_{m=0}^{M} f^*[m]\ g[m+n] \tag{1}$$

We have previously presented two cross-correlator application-specific integrated circuits (ASICs) [10, 11] developed using full-custom design in a 65-nm CMOS process technology. The first cross-correlator implemented

[1] Aperture synthesis has long been used for achieving high resolution in radio astronomy such as VLA, LOFAR and ALMA.

64 2-level input channels, while the second can be configured as either a 96-channel 2-level correlator or as a 48-channel 3-level correlator. A separate, 8-channel analog-to-digital converter (ADC) has also been custom made for these cross-correlators [12] in a 130-nm BiCMOS process. The motivation behind using a separate ADC was two-fold; it made channel isolation of below 30-40 dB much easier to achieve and it also meant bipolar transistors could be used, while the CMOS-based cross-correlator could be implemented in significantly more advanced (65-nm) technology nodes. The choice of bipolar logic for the ADC improved device matching properties [13] and made it easier to implement a high-precision comparator without using automatic offset cancelation techniques. The ADC together with the 64-channel cross-correlator have been assembled into a complete cross-correlator system [14].

We also implemented an ADC and an autocorrelator ASIC for spectrometry using full-custom design. The autocorrelator ADC was implemented using a 130-nm BiCMOC process technology, which was also used for the cross-correlator ADC, and was designed to support two 3-level channels. To obtain higher bandwidth, the autocorrelator ADC uses a time-division (TDM) scheme: We use four times the number of digital streams (TDM4), each outputting data at a rate of a fourth of the sample rate. The autocorrelator was implemented in a 28-nm fully-depleted silicon-on-insulator (FD-SOI) process technology and supports up to 8638 lags.

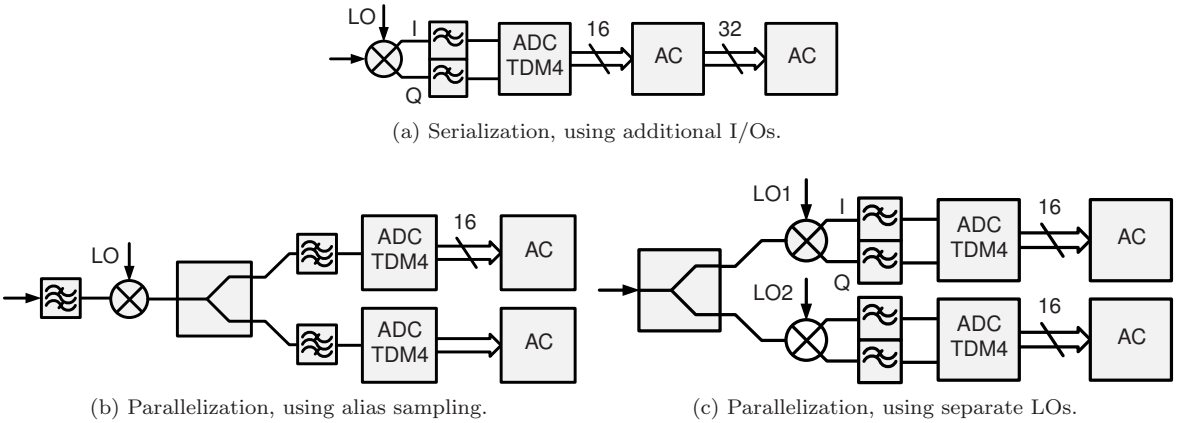
In this paper, we will evaluate different design methodologies of implementing cross-correlator and autocorrelator systems and their impact on system complexity and power dissipation, for design scenarios where we expand the number of baselines or spectral channels of the systems beyond the capabilities of the implemented ASICs. Our main focus is in on-satellite applications where size, weight, and power budgets are very restrictive, however, other applications such as security scanning applications [15], balloon experiments, etc. may have similar restrictions.

EXPANDING CORRELATOR DESIGNS

When construction correlators with high channel-count requirements, one have to consider the tradeoff between chip scaling and system scaling, i.e., the number of ASICs vs the number of channels per ASIC. These tradeoffs affect system complexity and, thus, size, weight, cost, and power dissipation. We will investigate implementation styles and system architectures, for both autocorrelators and cross-correlators, to handle system level-scaling based on a fixed number of channels per chip.

Autocorrelators

For autocorrelator systems, two approaches to increasing the resolution beyond a single ASIC are investigated; serialization and parallelization. We further divide the parallelization methods into two sub-categories, i.e., either using alias sampling or using multiple local oscillators (LO) to divide the band before analog-to-digital (AD) conversion. The three different schemes are shown in Fig. 1.



(a) Serialization, using additional I/Os.

(b) Parallelization, using alias sampling.

(c) Parallelization, using separate LOs.

Figure 1: System architectures for connecting multiple autocorrelators (AC).

The serial scheme has historically been more common due to the very limited number of channels that could be achieved on-chip. It is the simplest solution of the three to achieve greater resolution. In the serial scheme,

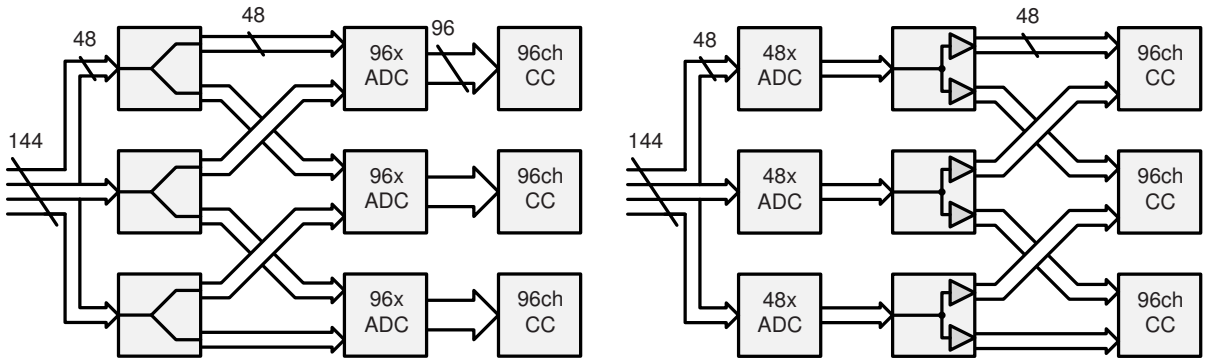
the entire band is sampled by a single ADC, after which the digital autocorrelator ASICs are linked, one after another.

Parallel schemes have usually been motivated by their ability to extend the total bandwidth beyond what ADCs and CMOS logic could handle. In the parallel alias-sampled approach, the band of interest is split, using power splitters, after down-conversion. Filter banks are used for sub-band division. Each sub-band is sampled by an ADC at a rate that is the Nyquist rate for the full band, divided by the number of ADCs used. For the multiple-LO scheme, the signal is split before down-conversion. A different LO frequency for each mixer divides the band into sub-bands along with low-pass filtering before each ADC. The sample rate here is the same as for the alias-sampling version. There is also the possibility to mix the serial scheme with any of the parallel ones. We will, however, not explore any such schemes in this paper.

While the parallel approaches may infer a significant extra cost, in terms of additional ADCs, splitters, filters and mixers, the serial scheme requires additional I/Os for the autocorrelator ASIC. To be able to serially link ASICs, instead of one IQ input pair, an additional delayed input and output for both non-delayed and delayed data are required, which leads to a total of four times as many I/Os as for a non-linkable design.

Cross-Correlators

For cross-correlators, the ASICs have to be connected in parallel, and signals have to be split to multiple cross-correlator ASICs for full baseline coverage. Still, we have the option of where to perform signal splitting; before or after AD-conversion. Two examples are shown in Fig. 4. Power splitters are used for the analog split, while current-mode logic[2] (CML) splitters are used for digital splitting. The difference in number of ADCs required for the shown case is a factor of two.



(a) Split before ADC using power splitters.

(b) Split after ADC using digital splitters.

Figure 2: System architectures for connecting multiple cross-correlators (CC).

SYSTEM SCALING ESTIMATIONS

Autocorrelators

The number of autocorrelator ASICs required naturally scales linearly with the number of spectral channels needed, and for the parallel schemes so does the ADC count.

Apart from complexity in terms of chip count, the different systems have very different advantages and disadvantages. If not only resolution is to be expanded, the case with separate LOs gives an advantage since the analog bandwidth requirement of the ADC is much lower than for the alias-sampled and serial schemes, where ADCs have to cover the entire analog band. In addition, with separate LOs, the sub-bands can be arranged and rearranged freely, ideal in cases where a large band has to be covered, but where continuous coverage is not necessary.

[2]The implemented ADCs use CML buffers for digital outputs.

The serialized scheme does impose a vulnerability if any of the circuits becomes faulty. A faulty ASIC in the chain could break the data flow and make remaining ASICs inoperable. The parallel schemes exhibit a more graceful degradation for broken correlator and ADC ASICs, giving more redundancy. The scheme using separate LOs gives an additional advantage in that any channel can potentially cover for any other broken one by switching the frequency. Even backup channels could be implemented this way.

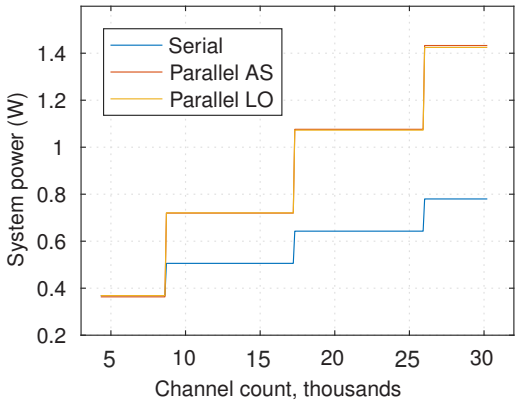


Figure 3: Estimated autocorrelator system power, including signal and clock splitters, ADC and autocorrelators, for three cases: Serial, Parallel with alias sampling (AS), and parallel with separate mixers (LO).

System power estimation, shown in Fig. 3, is based on measured results from the fabricated autocorrelator ADC, and simulated results including wire parasitics for the autocorrelator ASIC. Included are also mixer power, CML interface power and input power requirement, based on filter, splitter, and mixer losses. As shown, the two parallel schemes dissipate nearly the same amount of power and this is because total power dissipation is dominated by ADCs and correlators, which are identical for the two parallel schemes.

Cross-Correlators

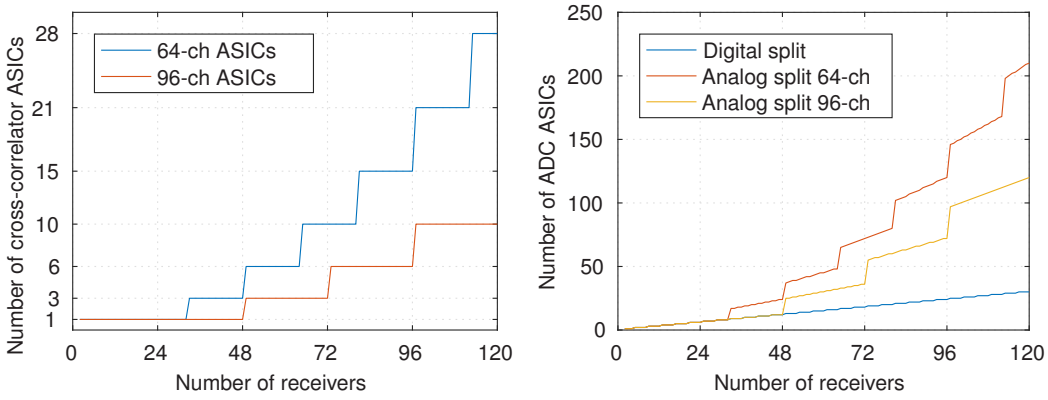
The number of required n-input ASICs grows as $\lceil N/n \cdot 2 \rceil \cdot \lceil N/n \cdot 2 - 1 \rceil / 2$, where N is the number of input channels from the front-ends. The number of cross-correlator ASICs, for two different input count alternatives, 64 and 96 2-level channels as in [10, 11], is shown in Fig. 4a. The numbers increase dramatically with higher input channel count requirements.

The number of ADCs when performing signal split after conversion, as shown in Fig. 4b, is naturally linear with the input count, but grows much quicker when splitting before AD-conversion. We base these estimations on an 8-channel ADC, as in [12]. With very large cross-coupling networks, the peak bandwidth may be reduced due to timing issues, and sub-banding may also be required, further exacerbating system complexity issues. Thus, it is clear that a high single-chip channel count is of the essence for keeping system complexity down, especially considering the cross-coupling that has to be performed for the cross-correlator application.

The power dissipation of cross-correlator systems with split before and after ADC, operating at 1.5 and 3 GHz, is shown in Fig. 5. Calculations include power dissipation for ADCs, cross-correlators, splitter circuitry and for additional input gain required when using power splitters. With the ADCs taking a large part of the complete system power dissipation, the split-after-ADC approach is clearly advantageous.

CONCLUSION

We have explored a few different correlator systems focusing on expanding channel counts beyond single ASICs; three for autocorrelators and two for cross-correlators. For autocorrelators, it is clear that the serial approach dissipates less power with the currently studied components, however, disadvantages such as less reliability, flexibility and significantly increased chip I/O-count means this is not necessarily the best option. For cross-correlators, we find that of the two schemes explored, splitting signals after AD-conversion is significantly more power efficient, at least with our current ADCs. It is also clear that the system complexity in terms of ASIC and I/O count scales dramatically worse for cross-correlators than for autocorrelators. With these results in mind,



(a) Number of 64- or 96-channel cross-correlator ASICs for systems with different number of receivers.

(b) Number of 8-channel ADCs for systems with different number of receivers.

Figure 4: Resource requirements for larger correlator systems.

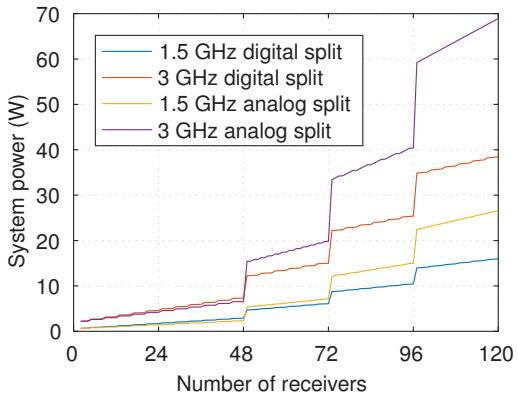


Figure 5: Estimated cross-correlator system power, including signal and clock splitters, ADC and cross-correlators, for four cases.

we find that there is great motivation for implementing large channel counts already at ASIC level to reduce system design complexity, especially for cross-correlators. This is further motivated by the significant reduction in cost of MOS devices, in terms of price per transistor, that has been achieved since the early correlators.

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Session E

Radiation tests of analogue and mixed-signal ICs

Radiation Tolerant Stochastic Fourier-Transformation

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Abstract

When radiation affects electronic equipment, bit errors are caused on the digital level. It is likely to avoid such errors especially on most significant bits (MSB). Stochastic computation (SxC) utilizes bit streams with all bits having the same significance. The information is, e.g., stored in the probability of ones. Single bit flips have less impact compared, e.g., to fix-point representation. Additionally, multiple errors can cancel each other out and reduce the impact of radiation even further.

Using the example of a Fourier-Transformation, the reliability of the calculation for a fixed-point and a stochastic approach are compared.

I. Introduction

The significance of Fourier-Transformation is proved by its numerous applications. Its importance increased through the possibility of implementing it on hardware in the specialized form known as the Fast Fourier-Transform (FFT).

For space applications, radiation is one of the most significant factors to be taken into account, when reliability of electronic equipment is in the focus. Long term usage and large temperature differences are present for electronic devices in satellites as well. On circuit level for terrestrial applications the keyword summing up these effects is PVTA, which is the short form for process variations (P), supply voltage variations (V), temperature (T) and aging (A).

Regardless of the actual effect, bit-flips must be taken into account at the digital or algorithmic level. Within a fixed-point representation, such errors have of course the highest impact on the MSB. On the contrary stochastic computation use bit-streams and store the information in the frequency of logical 1's or the ratio of logical 1's to 0's. This way all bits have the identical significance and the outlined impacts are expected to have less severe effects on the reliable calculation of the exemplarily chosen Fourier transform.

In the following section II both approaches are presented followed by details about the model of the simulation setup. Using that simulation environment the performance of the two setups is analyzed in section III. The spectrums are calculated for different parameter setups to represent different environmental conditions, e.g., caused through a mission duration or profile. In section IV further details about an implementation approach for the SxC setup are given according to the complexity and necessary logical modules. Finally, this work is concluded in section V.

II. Simulation Model

Two setups are compared with each other. On the one hand a double precision scaled fix-point FFT and on the other a stochastic DFT using the two-line bipolar representation. The results of both setups are referred to the MATLAB built-in *fft()* function.

The basics of stochastic computation have been published in [1], among others. Using an unipolar encoding, values in the range of *[0,1]* can be represented. The probability of ones within the overall stream length corresponds to the information. By linking the ratio of 1's and 0's to the overall length a bipolar encoding is set up, extending the representable range to *[-1,1]*. Assuming uncorrelated streams, simple mathematical operations can be performed by logical gates. E.g., a real multiplication is achieved by an AND gate. If the square is needed one stream needs to be delayed to avoid the correlation. For each addition, OR gates are used next to further modules to take care about the overflows, e.g., by scaling. Further details are given in [5]. Nevertheless, the SxC approach offers high system clocks, much parallelism options and, as will be shown in the next section, high reliability without using expensive rad-Hard components.

[2] and [3] showed approaches of a stochastic FFT and DFT introducing an unscaled adder and a stochastic representation using a sign- and magnitude stream. In contrast to those first publications on stochastic DFT/FFT, another encoding form is used here: The two line bipolar representation, which separates between real and imaginary part and for each between the positive and the negative part. The total of 4 streams are portrayed with 1024 bits each. It should be mentioned, that the type of representation as well the usage of a bipolar or unipolar encoding on the one hand defines the range of representable values, and on the other it has a distinct influence on the later on discussed performance. The way how the arithmetic's needs to be implemented, the necessary or used amount of bits and of course the achievable precision of the representation. Implementing an algorithm like the FFT, temporal back-conversions to the decimal domain may be necessary.

The fixed-point (FI) representation is well known and documented. Within this work, the setup works with double precision and thereby utilizes 64 bits per real and imaginary part.

The overall system setup is shown in Figure 2: From an analog time signal, considering out of the superposition of four trigonometric functions, 64 samples are taken and converted to

the digital domain using the shown ADC. The input signal is shown in Figure 1.

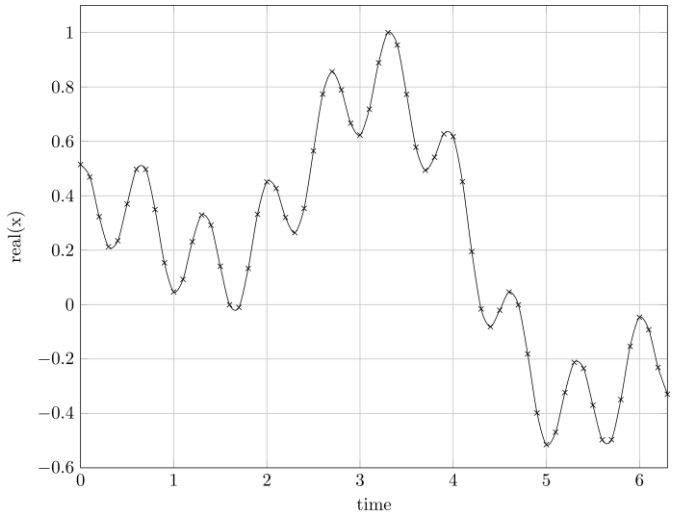

Figure 1: Input Signal

The PVTAR faults are applied to the digital samples of the input signal assumed to be stored within D-FlipFlops (FFs) in the shown N-bit buffer. The twiddle factors are assumed not to be affected.

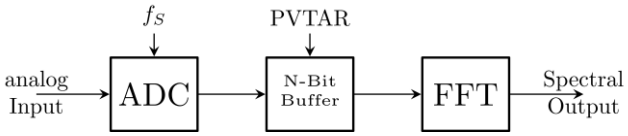

Figure 2: Simulation Setup

The error model, affecting the digital representation, is based on the analog circuit design. In detail, the PVTAR effects are simulated for each transistor in the D-FF circuit separately and summed up to model the FF in total. An error on bit level is injected, if the subsequent logical devices copy a false value compared to the FF input. The error model was published in [4].

III. Performance Analysis

As mentioned in section II the FI approach utilizes 64 bits twice, while the SxC system encodes each sample with four times 1024bits. In the first place, no PVTAR effects shall be present. The FI system is able to show its expected very high accuracy and precision (absolute error in order of 10^{-16}) in Figure 3, while the SxC setup is able to achieve an absolute error (compared to the built-in reference function) in the range of 10^{-3}, which is comparable to the inverse of the length of the bit-stream. Note that for each spectral sample the mean of 100 iterations is calculated. This holds for all following results.

However, both approaches offer very good spectral analysis. The first results match to the expectations, due to the binary representation techniques/encoding of the systems.

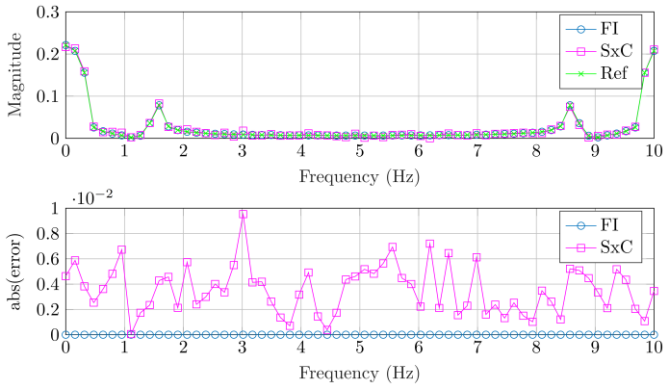

Figure 3: Performance without PVTAR

Next, both systems are analyzed in a more realistic scenario, considering to be used in space. The simulations parameters compromise process variations, a supply voltage of 0.8V, an operational temperature of 60°C, a Linear Energy Transfer (LET) of 500keV/µm and no aging/new devices. The spectrums are calculated according to the input signal given in Figure 1.

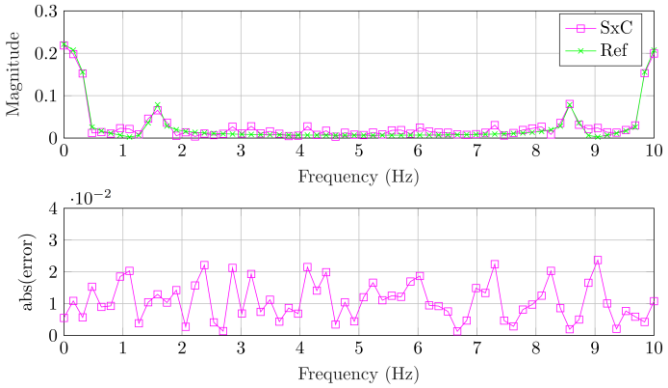

Figure 4: SxC spectrum with reference for P, V=0.8V, T=60°C, R=500keV/µm

In Figure 4, the calculated SxC spectrum is shown next to the reference of the MATLAB built-in function only. As the error for the FI setup increases from the first case (no PVTAR) to the order of ~10^{+300} the visualization is skipped in Figure 4. This means, that the FI approach is unusable within an exemplarily space mission. No reliable FFT can be calculated for the assumed parameter set. Additional radiation hardening techniques or certain devices are obviously necessary for a reliable FI processing. On the other hand, the SxC approach loses, due to the PVTAR impact, roughly one order of the magnitude considering the absolute error. However, a good approximation of the given reference spectrum is still achieved and visualized in Figure 4, even when no certain space qualified devices are assumed. These results motivate to take a closer look on the achievable performances with the SxC encoding type, as well to find a limit for the FI approach.

Figure 5 depicts the FI spectral results for two different cases. The parameters are set as follows: disabled process

variations, a supply voltage of 0.9V, a temperature of 20°C and a LET of 150keV/µm (case 1) or 250keV/µm (case 2).

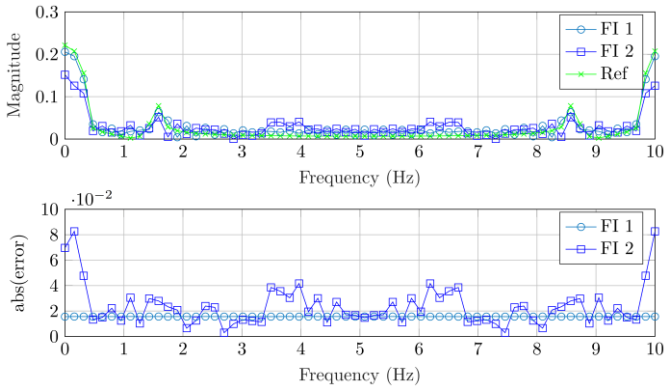

Figure 5: FI spectrums for P=0, V=0.9V, T=20°C, R=150 bzw. 250keV/µm

The moderate temperature and supply voltage enable the evaluation of the sensitivity of the FI approach for mainly radiation impacts. The mean of the absolute error is in the same order for almost both cases, but the precision for the low radiation case suffers from an offset. Therefore, the spectrum is still very accurate to the given reference. Increasing the LET (case 2) is it obvious, that the quality of the calculation decreases. According to the results visualized in Figure 4, it can be concluded that the FI setup has a limited usability with commercial of the shelf (COTS) components.

As the SxC approach already showed significantly more accurate results for higher PVTAR impacts (cmp. Figure 4), these two parameter sets are not to be considered for the SxC implementation. Instead, higher radiation is applied to figure out its upper limit. The simulation parameters are: P=on, V=0.9V, T=120°C, R=750keV/µm. The results are shown in Figure 6.

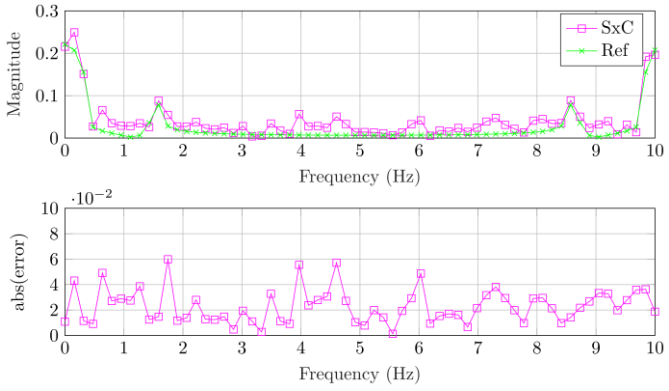

Figure 6: SxC spectrum for P=1, V=0.9V, T=120°C, R=750keV/µm

The mean of the absolute error is in the same order as the first case, discussed and presented next to Figure 4. Out of this, it becomes clear that even a LET of 750keV/µm achieves sufficient results in terms of accuracy and especially precision. However, for occasional uses the upper limit for radiation impact is even further extendable.

IV. SxC Complexity

A. Stochastic arithmetics

In section II, it was pointed out, that the SxC approach offers the usage of logical gates to perform simple arithmetic calculations. In detail, this depends on the representation type, meaning an exemplary multiplication can be performed by a single AND gate in a single line, unipolar representation type, using XNOR's for a bipolar single-line approach and several AND gates for the two line bipolar format.

For SxC-based additions, it needs to be ensured, that no overflow will occur. One possibility to avoid any result out of the limited range, is to introduce an additional scaling. In [2] an alternative approach is presented considering a sign and magnitude stream as well as additional counters.

B. Stochastic DFT

In order to perform the discrete Fourier Transformation (DFT), shown in Equation (1) a bipolar representation offering the in- and outputs with positive and negative signs is usually chosen.

$$X[n] = \sum_{k=0}^{N-1} x[k] \cdot e^{-j\frac{2\pi kn}{N}} \quad (1)$$

Out of equation (1) it becomes clear, that complex values must be handled. Hence, the stochastic representation separates between the real and the imaginary part. For the calculation of the algorithm this needs to be taken into account. The two-line bipolar representation finally uses in total four streams.

The processing of every DFT point, thereby requires 16N multiplications, each one performed by a logic AND gate. As the positive and the negative, as well as the imaginary and the real part, are considered separately the final addition requires a large multiplexer with 16N inputs and four outputs (one for each stream). The control signal of the multiplexer uses arbitrary binary numbers of $\log_2(4N)$ length. The entire scheme of the implemented DFT is given in Figure 7.

Alternatively, the DFT can be set up with scaling free adders (cmp. [2]). This would result in four streams as well (sign + magnitude for real and imaginary part), and a multiplication needs 4N AND's for the magnitude streams and 4N XOR's for the sign streams. Two further additions per multiplication and one N-point sum per real and imaginary part are necessary to complete one complex multiplication in that case. A high sensitivity against overflows is a huge drawback for this way of implementation. The two line bipolar approach, can be expected to give higher accuracy and was therefore the preferred choice.

C. IC-Implementation

A synthesis of the two-line bipolar approach was realized for 65nm CMOS technology using the Cadence Genus Synthesis tool for length from 16 to 256 points. For a 64 point implementation without pipelining, a frequency of 600MHz was achieved using an area of 364µm² and less than 55mW power consumption.

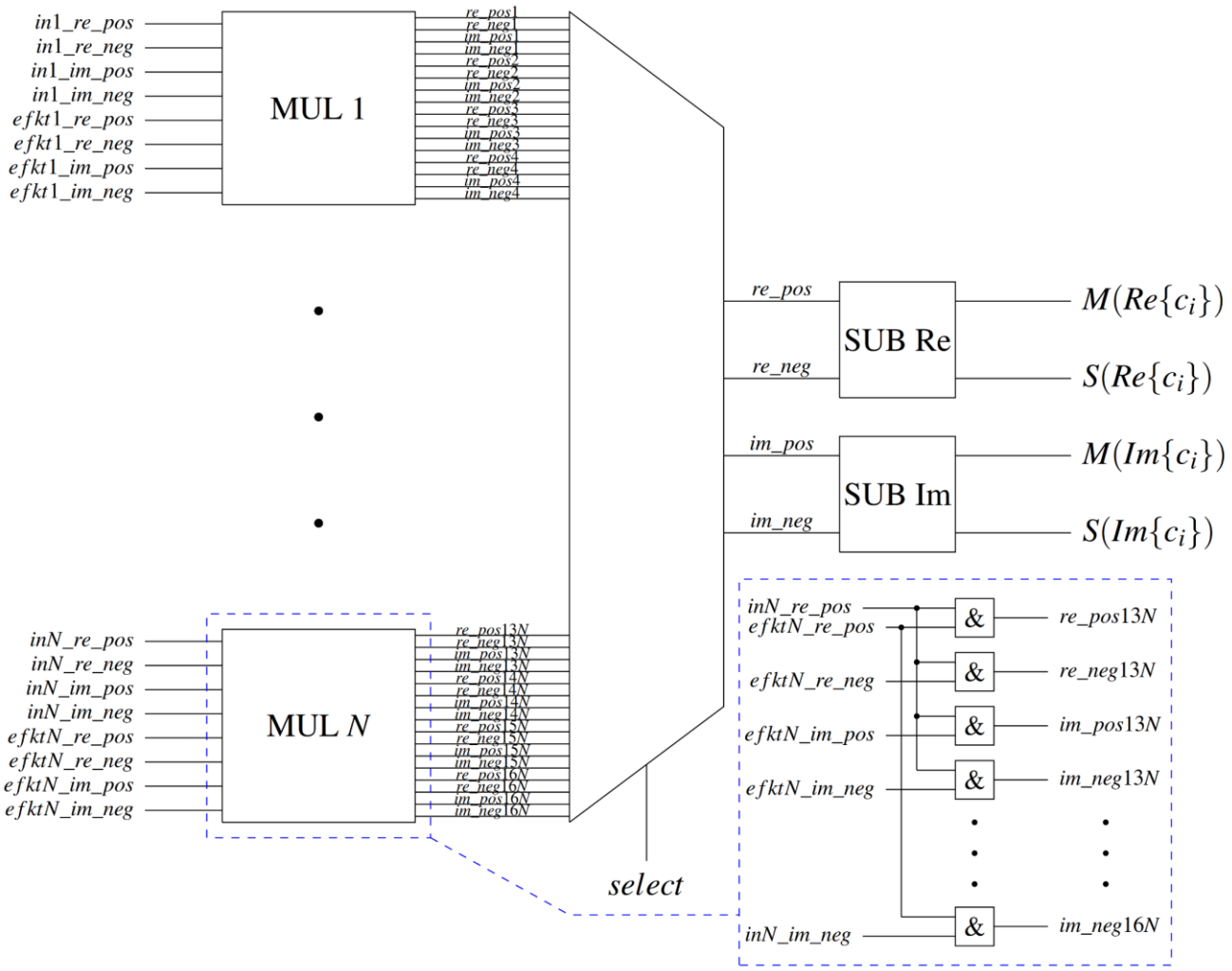

Figure 7: Schematic for two-line bipolar N point DFT, with scaling free adder used for the subtraction.

V. Conclusion

As it was stated in the ECSS-E-ST-10-12 document, "there is no space system in which radiation effects can be neglected." The effect of radiation is one of the PVTAR effects modeled in this work to simulate its impacts on the digital level. Exemplarily, the well known and in numerous (space) applications used Fourier-Transform, it was shown, that the SxC encoding scheme outperforms the common FI approach according to the precision and accuracy in the presence of multiple bit errors.

The benefits of very high system clocks and parallel computing possibilities compensates more than the drawbacks stemming from the increased number of the overall used bits, or the remaining imprecision for ideal conditions.

All in all, it was discussed, that different stochastic encoding types have its own pros and cons, which needs to be taken into account for developing or adapting an algorithm. The two line bipolar setup emerges good for the presented DFT application but does not need to be the best choice in every case.

Furthermore, the precision of the SxC approach benefits from longer bit streams. Studies on this aspect were presented in [5].

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The First SEE Test Campaign in Turkey at the METU Defocusing Beamline Preliminary Setup

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Abstract

The preliminary setup of the METU Defocusing Beamline was commissioned in December 2017. This beamline, which is at the Turkish Atomic Energy Agency (TAEA) Saraykoy Nuclear Research and Training Center (SANAEM), follows the R&D beamline at the proton cyclotron of Proton Accelerator Facility (PAF) which accelerates beams to 15-30 MeV kinetic energy [1]. The preliminary setup, with two quadrupole magnets provides an irradiation area of 4 cm x 6 cm with 15% radiation dose uniformity, with a flux of 3.8×10^9 p/cm/s^2. The final setup which will be constructed and commissioned at the end of 2018, will have a adjustable collimator and 3 quadropole magnets, providing users with an irradiation area conforming to the ESA-ESCC 25100 standard, with 10% radiation dose uniformity and a flux menu selectable between 10^6-10^{10} [2].

The first Single Event Test (SEE) at the preliminary setup were performed using 30 MeV protons with a collaboration of TUBITAK Space Technologies Research Institute. A test card was designed around two units of buffers and the readout was performed using an oscilloscope with frame capture. Two rounds of 25 seconds DAQ windows were acquired. In this poster, we first present the METU DBL project and then the results of the SEE tests performed at this new facility.

I. The Preliminary Setup

METU-Defocusing Beam Line (METU-DBL) is an extension of TAEA-SANAEM R&D Beam Line. METU-DBL construction will start after the installation of 5-port switching magnet so that 4 other experiments can be installed in this room. This magnet was delivered only in May 2018, later than planned and this allowed for the construction of a preliminary test setup, that has now been disassembled. The preliminary setup was constructed in 2017 and preliminary tests were performed from December 2017 to March 2018. Figure 1 shows the schematic of the preliminary setup of METU-DBL. This setup starts with moveable beam stopper and a vacuum shutter for emergencies and then is followed by one collimator that proceeds two quadrupole magnets, followed by a long (2.5 m) flight path for enlarging the beam [2]. The collimator prevents protons from hitting the magnets. There is 2 mm-thick graphite layer on the magnet side of the collimator. The graphite moderates some of particles scattered from the collimator.

The preliminary setup provides 4 cm x 6 cm irradiation area after a thin (50 µm) titanium vacuum window. Vacuum inside the beam pipe stays below 10^{-6} Torr. With this irradiation area, the first SEE test campaign in Turkey was performed.

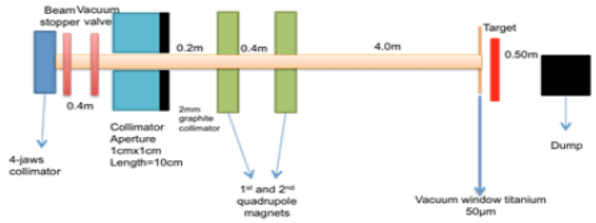

Figure 1: Schematic of METU-DBL preliminary setup

At the end of the METU-DBL preliminary setup, there is test desk between the vacuum window and a cooled beam dump. Magnets, beam stopper and several of the measurement elements of the test desk, as well as the beam dump, are cooled with a cooling system with a total capacity of 50 kW. Figure 2 shows a photograph of the preliminary setup that was used for the first SEE test campaign in Turkey.

A control system written in Labview communicates with all other subsystems: cooling, vacuum, beam optics and the test desk. The operator can monitor and control all the subsystems through a user interface while sitting in the control room across the R&D room.

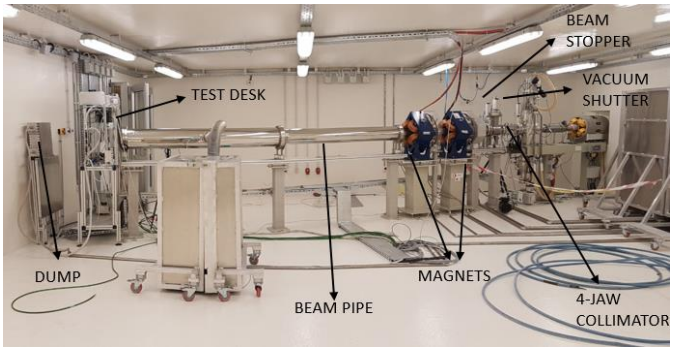

Figure 2: A photo of the METU-DBL preliminary setup, in December 2017.

II. Test Desk

The purpose of using a test desk is to measure the flux and uniformity of the proton beam that the device under test

(DUT) exposed to. Three different detectors and the DUT are attached to different sliding X-Y stages, which can move them in and out of the irradiation area, according to the commands from the control system, which has two modes: measurement of the beam by scanning and irradiation of the DUT. The fiber scintillator detector, the Timepix3 and the diamond detector are shown mounted on their respective X-Y stages on the test desk in Figure 3 [4, 5, 6].

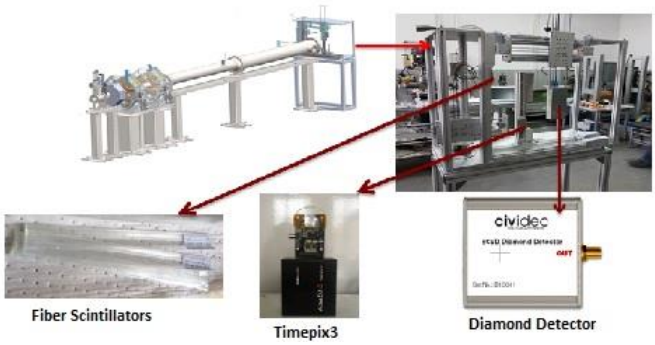

Figure 3: Fiber scintillators, the Timepix3 and the diamond detector as mounted on their respective X-Y stages on the test desk

A. Fiber Scintillators and Photo Diode Detector

3mm-thick fiber scintillators, made of polymers, produce photons when a proton passes through it. 4 of these fiber scintillators coupled to a four-channel photodiode constitute a module, seen in Figure 4. There are two such modules, one that scans the beam horizontally and one that scans vertically.

Figure 4: A module consisting of 4 fiber scintillators wrapped in black tape and the shielded photodiode and electronics box below it. This module scans the beam horizontally.

In order to increase the number of captured photons, scintillators are coated with silver and light-proofed with black tape. Photons emitted from the scintillators are converted to analogue electrical signals by the photodiode. These analogue signals are pre-amplified using Operational Amplifiers (LT1055) before being digitized by a microcontroller (Arduino UNO R3). Digitized photodiode signals are then transmitted to the control computer located in the control room via Ethernet for logging and monitoring in Labview. The photodiode and readout electronics shielded from protons, in a box made of polyethylene sandwiched in Al 6082, to decrease the radiation dose they receive.

B. Diamond Detector

A synthetic 5 mm x 5 mm diamond between gold electrodes biased with 400V provides a fast proton detection signal. The ns-duration signal is first amplified with a broadband amplifier. These signals are then sampled using a high speed 16-bit resolution A/D converter (TI ADS54J60EVM) and then fed into an FPGA Board (TI TSW1456EVM). A single board computer (SBC) records the frames, each containing $2x10^5$ triggers, coming from the FPGA Board using its USB 3.0 port. As the final step, the SBC transmits the frames via Ethernet to the control computer for further signal processing. A Matlab code, which is embedded into Labview, counts the protons in frame and calculates the flux. The readout electronics of the diamond detector is also shielded against radiation using aluminium and polyethylene.

C. Timepix3 Pixel Detector

Timepix3 is silicon detector, with a 255 x 255 silicon diode pixel array with 55 µm edges. The measurements with Timepix3 is performed using Pixet Software [7]. The Pixet Program works on another SBC connected to an AdvaDAQ readout card on the test desk. The control computer communicates with the SBC through the Ethernet.

During the flux measurements in METU-DBL tests, Timepix3 detector records time of arrival (TOA) and time of threshold (TOT) information in frame based mode. When a particle, whose energy is higher than pre-defined threshold (TOT), hits a pixel, the hit time is recorded (TOA). Neighbouring pixels that have very close TOA information count as one particle in order to increase measurement accuracy.

Again, a Matlab code, which is embedded into Labview, is used for counting protons and calculating flux.

The Timepix3 readout electronics are again shielded against radiation.

III. SEE TEST

A. Test Preparation

Two generic 3-state buffer gates (TI SN74LVC1G125-EP) are used as a DUT. The SEE test request from TUBITAK Space Technologies Research Institute required some customizations of the test desk. First, a sandwich shield was designed and built to protect sensitive electronic components on the test card, that should receive minimal radiation dose. This sandwich shield took the place of the Timepix3 detector on its X-Y stage, which meant that flux measurement could only be performed using the other two detectors. Second, custom-made holder for the test card, that allows for several cables to be routed, was designed and produced to attached the test card to the X-Y stage.

B. Test Procedure

The tests starts with TAEA delivering the proton beam to the METU beamline, while the beam stopper is closed. The beam stopper, which can open or close in 1 second, is used to control the duration of the DUT irradiation carefully. The beam stopper is only opened when a detector is ready for scanning the beam or the DUT is ready in its test position for irradiation. Flux was measured with the diamond detector, which is similar in size to the buffer DUT, at the point where DUT would be located. The scan of the scintillator fibers gives a flux integrated over one axis, is shown in Figure 5, and is consistent with the measurement from the diamond detector.

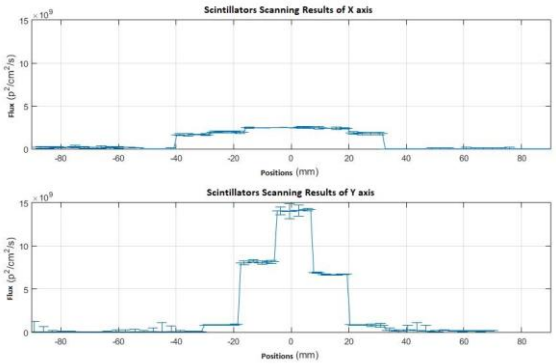

Figure 5: Scanning results of scintillators on both axis

Table 1: SEE Test Condition

Energy	30 MeV
Fluence	0.1 µA
Flux	3.80 x 10^9 p/cm^2/s
Duration	25 ± 1 s
Total Secondary Particle Dose	Gamma: 0.02 rad Neutron: 0.13 rad

When the flux measurements are completed, the DUT is moved into irradiation area with the help of remotely controlled X-Y stage. At a flux of 3.80 x 10^9 p/cm^2/s, only 25 seconds of irradiation was enough to reach a fluence of 10^{11} protons as prescribed by ESA 25100 standard.

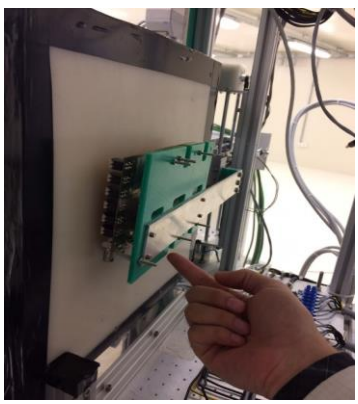

Figure 6: Customization on the test desk: The white polyethylene shield replaces the Timepix3 detector and a new holder for the DUT is attached to the X-Y stage

TUBITAK Space Research Institute recorded the measurements using a 1 GHz sampling oscilloscope. The voltage on the output of the buffer and the current consumption is monitored through the test card whose topology is shown in Figure 7. Measurements are performed three times; before the beginning of the test without radiation, under radiation and after the test without irradiation.

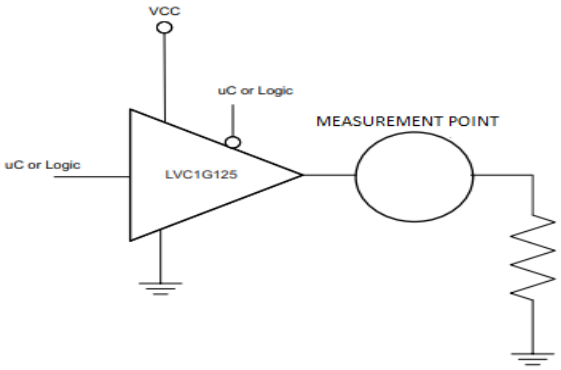

Figure 7: Test card topology for 3-state buffer [8]

IV. Results and Conclusion

TUBITAK Space Research Institute examined the results of their collected data. There are no SEE effect observed during or after the irradiation. Figure 8 shows a part of circuit's output 3.0 V DC signal with noise as recorded on the oscilloscope during the test.

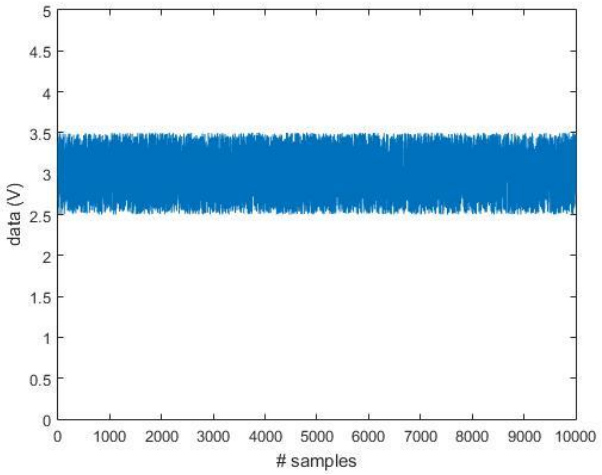

Figure 8: Output of the buffer as recorded on the oscilloscope during the test

Commissioning a new beamline is a challenging task and performing preliminary SEE tests helped achieve two closely related goals: raising awareness of radiation effects in Turkey and building confidence in the METU-DBL project. This collaboration between TUBITAK Space Research Institute and METU was a valuable experience which resulted in some design changes for the final version of METU DBL to be built starting June 2018.

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Heavy Ion Test Results of Different Analog to Digital Converters

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***Abstract* — This paper presents the results of heavy-ion induced single event effect (SEE) tests, performed on analog to digital converters (ADC), which are candidates for usage in spacecraft electronics. The experimental data was obtained at Roscosmos Test Facilities during test campaigns in 2017.**

***Keywords* — SEE, SEL, destructive failures (DF), test facility, LET, ADC.**

I. INTRODUCTION

Analog to digital converters of COTS and industrial production-levels are widely used in the space industry. However, there is very few data on exposing these components to heavy ions. Before using these components in space, they must be tested. The most safety critical type of SEE for analog to digital converters is SEL, which, moreover, often leads to destructive failure.

II. TEST TECHNIQUES AND FCILITIES

The tests of electronic components were conducted from January to December 2017 on the Roscosmos SEE Test Facilities created by JSC Branch of URSC-ISDE and based in Dubna City (Moscow Region, Russia), at the FNRL JINR cyclotrons U-400M and U-400 [1, 2]. The Facilities used during these test campaigns allow the DUTs to be irradiated with different energies ranging from 3 to23 MeV/nucleon of various ion species, in a range of particle fluxes from 10 to 10^5 particles×cm^{-2}×s^{-1}. The DUTs were exposed to different ions, with LETs from 6.34 to 69.2 MeV×cm^2/mg at temperature of 25 °C as it was specified in the requirements. The devices were irradiated at normal incidence with a flux non-uniformity of better than 10 %. The criterion adopted for SEL effect was a hopping increase in the supply current accompanied by a functional test failure, while supply current value and functionality recovered after power reset only. A destructive failure was registered in case of negative result of the functional testing after the power reset. For each type of device, the number of tested samples was not less than 3.

III. TEST RESULTS

The experimental data are listed in Table 1

TABLE 1 TEST RESULTS

Part Number	Manufacturer	Device Function	Test Results*
B7892RH BMTI	Beijing Microelectronics Technology Institute	12-Bit ADC	SEL LET > 69.2 MeV×cm^2/mg (Si). E = 3.9 MeV/nucleon; Range in Si = 42.5 um.
AD7893BRZ-5	Analog Devices	12-Bit ADC	SEL LET > 41.73 MeV×cm^2/mg (Si); E = 20.1 MeV/nucleon; Range in Si = 210.5 um.
ADC08D500CIYB/NOPB	Texas Instruments	Dual 8-Bit, low power ADC	SEL LET > 15.71 MeV×cm^2/mg (Si); E = 3.3 MeV/nucleon; Range in Si = 34.63 um.
* test level – until 30/100 SEE or destructive failure were observed, fluence was 10^7 particles/cm^2 if no effects were observed, unless otherwise specified.			

During irradiation all ADCs were in active electrical mode with the recommended maximum supply voltage.

The Verification of operability of the ADC samples consisted of parametric and functional tests. The ADC sample was considered operable if the parametric and functional tests passed with a positive result.

Before and after irradiation, 10 signal values are fed to the analog input. 10 transformations are made for each of the value of the input voltage; according to the results of the transformations, the maximum and minimum allowable values for the corresponding input voltage are determined, this is done to estimate the noise during measurements on the test facilities. The minimum (DOC_{MIN}) and the maximum (DOC_{MAX}) code for all subsequent ADCs were determined as follows:

$$DOC_{MIN} = DOC - 5 \times \sigma_{ADC},$$

$$DOC_{MAX} = DOC + 5 \times \sigma_{ADC},$$

DOC – average code for sample of 10 values

σ_{ADC} – standard deviation for sample of 10 values.

Functional check during irradiation consisted in comparing the resultant conversion code with the maximum and minimum allowable code values determined before the start of the test. Functional check considered successfully passed in case the output digital code corresponded to the input voltage, taking into account the conversion characteristic. Short-term inconsistencies in the output code of the conversion characteristic arising during irradiation in a single or series of successive transformations were not considered a functional failure.

A. AD7893BRZ-5

During irradiation the AD7893BRZ-5 was in an active electrical mode, the supply voltage V_{DD} = 5.25 V, REF_{IN} = 2.5 V. On input V_{IN} the voltage was set at 3.0 V, the input signal on SCLK was a 8 MHz square wave with amplitude of 5 V. On input #CONVST was fed a signal in accordance with Figure 1. A block diagram of the AD7893BRZ-5 test setup is shown in Figure 2.

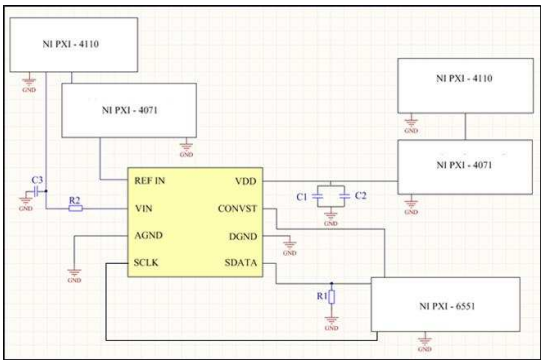
Figure 1 – Time characteristic for specifying control signals

Functional checkout consisted in carrying out the following tests:

- during irradiation the AD7893BRZ-5 was in an

active electrical mode. Resulting output code was compared with DOC_{MIN} and DOC_{MAX}, determined prior to the test. The functional checkout considered successfully passed if the digital output code corresponded to the input voltage;

- before and after irradiation, characteristics of the conversions were evaluated. For this purpose, on input V_{IN} 10 values of voltage ranging from 0 V to 5.0 V in steps of 0.5 V were supplied. After irradiation, for each voltage, conversion and validation whether the output code in a valid range from DOC_{MIN} to DOC_{MAX} were performed. The functional checkout considered successfully passed if the values for each of input voltage fell within the allowable range of codes defined before the start of irradiation.



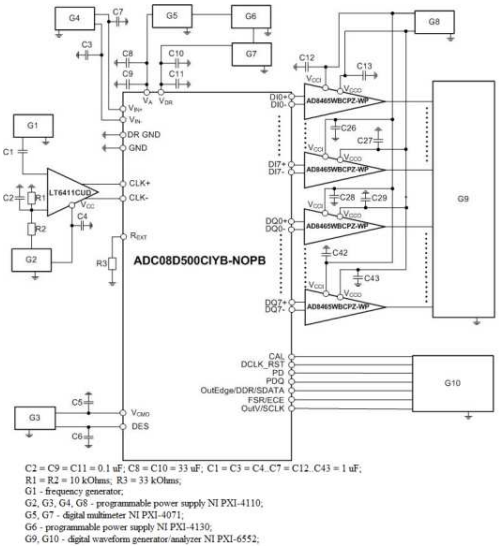
R1 = 50 kOhm, R2 = 10 Ohm, C1 = 1 uF, C2 = 0.1 uF, C3 = 1000 pF.

Figure 2 – Block diagram of the AD7893BRZ-5 test setup during irradiation

B. ADC08D500CIYB-NOPB

Irradiation of the ADC08D500CIYB-NOPB was carried out in an active electrical mode, at a supply voltage V_{DR} = 2.0 V and V_A = 2.0 V. On inputs V_{IN+} and V_{IN-} was supplied voltage of 1.64 V and 0.88 V, respectively. On inputs OutV/SCLK, FSR/ECE was logical level of "1", on DES was supplied 1.0 V voltage, on OutEdge/DDR/SDATA, PDQ, PD – logical level of "0". On CLK+ and CLK- was set the periodic square wave differential signal, V_{CM} = 1.26 V, amplitude of 1.0 V, frequency of 500 MHz Block diagram of the ADC08D500CIYB-NOPB test setup during irradiation is shown in Figure 3.

Functional test was carried out in a similar way to AD7893BRZ-5.



C2 = C9 = C11 = 0.1 uF; C8 = C10 = 33 uF; C1 = C3 = C4..C7 = C12..C43 = 1 uF;
R1 = R2 = 10 kOhms; R3 = 33 kOhms;
G1 - frequency generator;
G2, G3, G4, G8 - programmable power supply NI PXI-4110;
G5, G7 - digital multimeter NI PXI-4071;
G6 - programmable power supply NI PXI-4130;
G9, G10 - digital waveform generator/analyzer NI PXI-6552;

Figure 3 – Block diagram of the ADC08D500CIYB-NOPB test setup during irradiation

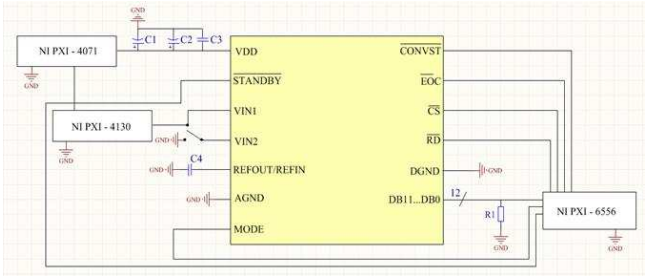
C. B7892RH BMTI

Irradiation of the B7892RH BMTI was performed in an active electrical mode in accordance with Table 2. Block diagram of the B7892RH BMTI test setup is shown in figure 4.

Functional monitoring was carried out in a similar way to AD7893BRZ-5.

TABLE 2 – CONTROLLED SEE AND OPERATION MODE FOR B7892RH BMTI DURING IRRADIATION

Type of SEE	Operation mode during irradiation
SEL	Internal reference voltage REF_{IN} = 2.5 V; Supply voltage V_{DD} = 5.5 V, V_{IN1} = 3 V, V_{IN2} = GND; MODE and #STANDBY – logical high; #CS and #RD – logical low; On input #CONVST - square wave signal with amplitude of 5 V and frequency of 10 kHz.
DF	



R1 = 50 kOhm, C1 = C2 = 10 uF, C3 = C4 = 0.1 uF.

Figure 4 – Block diagram of the B7892RH BMTI test setup during irradiation

V CONCLUSION

The experimental data obtained during the heavy ion tests confirmed the immunity of 11 of 12 devices to DF and SEL effects. But for 1 device we observed SEL and destructive failure. These results of validation tests presented in this work allow designers of spacecraft equipment and systems to draw a conclusion on the conformity of the tested devices to the specified requirements for defined applications. Those components, which do not meet the requirements, should be replaced or additional measures should be taken for hardening if possible.

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Session F

Evaluation and qualification of full custom ICs for space applications

Re-Thinking Reliability Analysis

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Abstract

The rapidly increasing electrical content in automobiles is driving the need for revolution in analogue IC design methodology. Compared to designing for consumer electronics, designing for mission critical applications: industrial, medical, space and automotive, requires re-thinking the approach to analysis of reliability. To improve the results of reliability analysis, we will look at several enhancements to reliability including better modelling of device degradation, accelerate electrical aging with additional phenomena that contribute to shifts in device characteristics, and using realistic use models to better represent the how the devices are used.

I. INTRODUCTION

One of the key challenges for mission critical design is the need to reduce the failure rate across the product lifetime. Traditionally, the failure rate has been expressed as the bathtub curve.

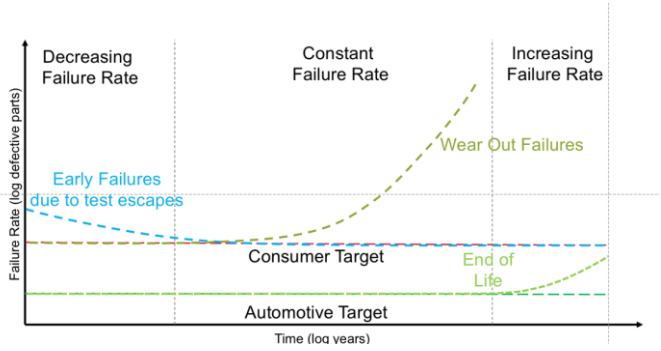

Figure 1: Failure Rate Bathtub Curve

The bathtub curve has three regions: early life, useful operating lifetime, and end of life. The primary source of failures during early life is test escapes. Test escapes are defective devices that are not identified during test. Once these devices reach consumers, they fail resulting in field returns. During the useful operating lifetime, the source of failures, the challenge is to assure that device is constrained to operate within the operating range used for reliability analysis, in particular, design to prevent thermal overstress is critical. At the end of life failures occur due to devices device wear-out, changes of device characteristics due to electrical stress. While engineers may think in terms of the bathtub curve, users, in particular, automotive customers, have a different view. They want the failure rate for an integrated circuit to start out low, ideally, 0 defective parts per million, dppm, and stay at 0 dppm until beyond the useful lifetime of the product. Consider the effect of a 1dppm failure rate for integrated circuits on an automobile. If a typical mid-class car has 80 Electronic Control Units, ECUs, and each ECU contains several integrated circuits, then for every million cars produced about 15,000 cars, 1.5%, of the cars will defect out [1]. Design for automotive applications also place high expectations on reliability, lifetime of integrated circuits compared to the traditional requirements of consumer applications. Typical operating lifetimes for consumer products are from 1~3 years while automotive applications require up to 15 years of lifetime [2].

In this paper we will explore how the reliability analysis is evolving to meet the requirements of mission critical applications like automotive design. First, we will look at how design currently perform reliability analysis, then consider how the needs of mission critical design is forcing the methodology to change. Then we will consider some opportunities to enhance reliability analysis. We will close with considering the impact of these enhancements on simulating the effect of radiation on circuit performance.

II. RELIABILITY ANALYSIS THEN AND NOW

Designers have long recognized the need to be able to analyse the reliability of integrated circuits. There are two commonly used approaches for performing reliability analysis. The first approach is to calculate the change in device characteristics, device degradation, based on the electrical operating conditions and the temperature. The results allow designers to determine if a circuit will still meet specification at the end of life. One early tool for analysing device degradation was the Berkeley Reliability Tools, BERT [3]. The technology is available in Cadence Design Systems, RelXpert Reliability Simulator. The RelXpert Reliability Simulator also introduced one new innovation the AgeMOS model. The AgeMOS model is a compact model for modelling device degradation due to Hot Carrier Injection, HCI, and Bias Temperature Instability, BTI. The AgeMOS model is used with standard compact in RelXpert to enable RelXpert reliability simulation. While tools like RelXpert are powerful, they require special models to predict device aging, e.g., AgeMOS, and additional simulation runs. To address these concerns a second methodology for analysing reliability has been developed. It relies on the availability of safe operating checks in modern circuit simulators, for example, the Spectre® Accelerated Parallel Simulator. A safe operating check monitors a device during circuit simulation and issues a warning if the device leaves the safe operating region. Originally, safe operating checks were developed to assure that device junctions did not exceed their

breakdown voltage. However, by defining an acceptable change in device characteristics, the safe operating checks can be used to perform reliability checks. This approach is sufficient for consumer applications where product lifetime is relatively short. The advantage of using the safe operating area checks is that they are performed while the design is being simulated so for no extra effort designers can verify the electrical performance of their design and the assure that it will meet their reliability criterion. Due to its ease of use, the safe operating region-based approach to reliability analysis has become widely used.

For mission critical applications, like automotive, or use harsh environments like space or particle accelerators, these approaches for analysing reliability are not sufficient. Consider the two cases where both circuits pass the safe operating check. For one design with 100 transistors all the devices have are just below the failure threshold at end of life, versus a design with 100,000 transistors all with a small shift at the end of life. Which part is more likely to become a problem in a system? The approach for analysing these systems is based on calculating failures in time, the failure is calculated using FITs, failures per billion hours [4,5]. Let's look at a simplified example of how to calculate Mean Time to Failure, MTTF, using FIT, suppose we have two components with a failure rate of 100 FITs, a component with a failure rate a failure rate of 300 FITs, the total failure rate is 500 FITs and the MTTF is 2 million hours. While this approach works it requires knowing the failure rate in FITs. This approach works will at the system level but is difficult to apply at the integrated circuit level. So, the problem remains as the product lifetime expectations increase there is a need for more predictive analytical tools for reliability. If using the FITs based method is difficult to apply to integrated circuits, then what can be done? The approach we will use is to go back to device degradation calculations and look at how we can improve the results. In particular, we will focus on three areas: improving the device degradation model, improving the analysis by accounting for factors that accelerate device aging, and introducing the concept of mission profiles.

III. MODELING DEVICE DEGRADATION

The first improvement to the reliability analysis is to improve the model used to calculate the device degradation. Since the original Lucky Electron Model, LEM [6], was developed and implemented in BERT more advanced models have been developed. The AgeMOS has been enhanced to account for these new phenomena and is predictive for planar CMOS designs. Recently other model formulations have been proposed including the electron-electron scattering, EES [7], and multiple vibrational excitation, MVE [8]. These models offer improvement over the LEM approach but are not sufficient now to support the new device structures required for advanced node designs, that is, for designs with FinFET transistors. The three-dimensional, 3D, structure of a FinFET results in changes in how stresses effect the device degradation. So, a new aging model for FinFETs has been developed and demonstrated [9]. The model has been enhanced to provide better prediction of HCI induced degradation including saturation effects under high stress conditions. In addition, modelling of BTI induced degradation and recovery has been improved. This model is extensible allowing for a unified aging for both legacy and advanced node reliability analysis.

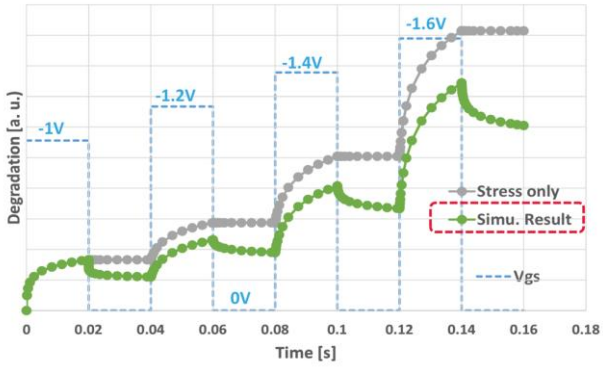

Figure 2: Improved Model for BTI Recovery

Shown in Figure 2 are simulation results for Bias Temperature Recovery using the New Generation Reliability model. The new recovery provides better prediction of degradation and recovery across operating conditions, like varying overdrive and recovery levels and duty cycle.

IV. ACCELERATING RELIABILITY ANALYSIS

The next improvement to reliability analysis is to account for all the phenomena that account for device degradation in the analysis. Instead looking at one factor, phenomena, at a time, we will look at reliability analysis more holistically. So, the analysis will consider for all the phenomena that contribute to device degradation together not in isolation. The phenomena we will consider are electrical stress, temperature, and process variation. In the RelXpert, the effect of the electrical stress on device degradation is calculated. The effect of temperature is included in the analysis, however, there are some limitations to the implementation. For RelXpert, temperature is a global parameter, typically the ambient temperature is used. However, in many cases this description is not sufficient. Device degradation is typically exponentially dependent on temperature and small differences can result in significant differences in device degradation. For example, for advanced node devices the 3D structure results in significant self-heating. Two devices may have identical layouts, one device driving a large load with a high activity rate, e.g., a fast clock, and another driving a light load node and at a low activity rate, e. g., power-on reset, will operate at different temperatures and experience different rates of aging [10]. The simulation is modified, self-heating analysis is performed to calculate the average temperature of each transistor. After back-annotating each device with its temperature, the reliability analysis is performed including the effect of device temperature and electrical stress. At the cost of additional simulation time, much better estimation of device degradation can be achieved. In addition to temperature, the effect of process variation needs to be included in the analysis. We could perform reliability analysis across process corners similar to how we perform other standard PVT verification of a circuit. While this approach accounts for aging due to the effect of process corners on the electrical stress, it misses the effect of process variation on device degradation. Consider Hot Carrier Injection, it occurs because electrons become trapped in the gate oxide and shield

the channel from control by the gate voltage. However, the effect of the trapped electrons is dependent on the gate oxide thickness. Another approach to account the effect of process variation on device aging to perform reliability analysis and use the fresh, before aging, Monte Carlo distribution to estimate the end of life, aged, distribution. This approach has limitations with how to define the variation, sigma, to use, the absolute value or the percent change. In addition, this approach ignores the relationship between process variation and device degradation. The solution to the problem is to analyse the effect of process variation and device degradation together [11]. The approach is to perform a Monte Carlo analysis, then perform aging analysis on each Monte Carlo analysis seed. The cost is an increase from N Monte Carlo runs, to N Monte Carlo runs + N Aging runs, or roughly doubling the simulation time.

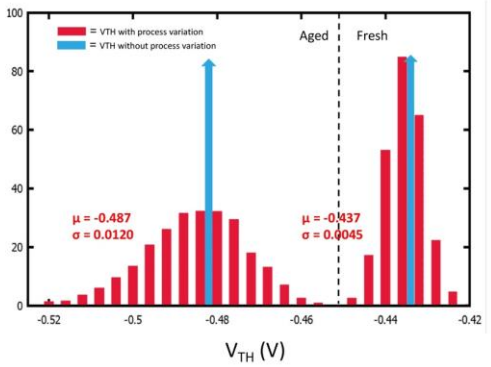

Figure 3: Including the Effect of Process Variation in Reliability Analysis

Shown in Figure 3 is an example of analysing process variation and device degradation together. There is one other consideration the device statistical models also need to be enhanced to account for correlation between process variation and device degradation. As with temperature, at the cost of increased simulation time, we can significantly improve the accuracy of the simulation results.

In order to improve the accuracy of reliability analysis, the reliability analysis needs to account for the phenomena that contribute to device degradation: electrical stress, temperature, and process variation.

IV. MISSION PROFILES

The final improvement to the reliability analysis is to improve the description use model, the mission profile, used to calculate the device degradation. First consider the RelXpert reliability simulation flow, shown in Figure 4.

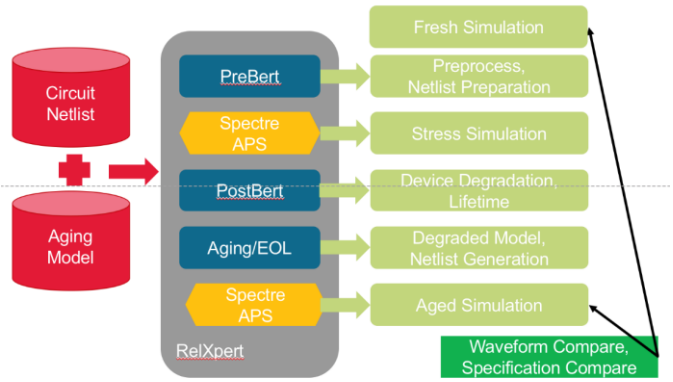

Figure 4: RelXpert Simulation Flow

Typically, there are three simulations performed. The first simulation is the fresh simulation, the simulation without aging, that is used for reference. The second simulation performed is the stress simulation. The stress simulation is performed at the worst case operating conditions, for example, if the ambient temperature is 27C and supply voltage is 3V, used for the fresh simulation, then the temperature will be 80C and the supply voltage will 3.3V, the worst-case conditions. The intent is to calculate the maximum shift due to stress by using the harshest operating conditions. The aged simulation is performed with the same conditions as the fresh simulation so that the overall shift in circuit performance can be measured.

Unfortunately, just using the worst-case conditions results in excessive pessimism, in particular, for applications like automotive design. While the environmental conditions that automobiles operate in can be difficult, automobiles do not operate continuously. Consider how many hours a day an automobile is used, weekdays an automobile is used to commute to and from work and spends most of time idle. While on the week-end, the car might be used for shopping, visiting family, et cetera. Another consideration is the climate, ambient temperature of an automobile experiences in Yellow Knife, Northwest Territories is quite different than an automobile experiences in Paris, France. The result is that we need to change how we apply the stress. The stress simulation needs to account for the how operating conditions vary. This is done by applying different mission profiles based on the different corner conditions in how the automobiles are used. In practice, this means that multiple stress simulations will need to be performed each with differing durations based on the range of operating conditions for each mission. For example, running 10 stress simulations from 0C to 40C each simulation being performed for a different percentage of the product's lifetime.

Using Mission Profiles allows us to explore how the different competing degradation mechanisms impact the design in order to assure that under all conditions, the device lifetime requirements will be satisfied.

V. TOOLS FOR RELIABILITY ANALYSIS

The RelXpert flow is a useful tool for performing reliability analysis. However, it is stand-alone tool and has some limitations, in particular, limited performance and capacity. To address these limitations reliability has been integrated directly

into Spectre APS which allows designers to perform much larger simulations, much faster than they have been able to in the past. Spectre native reliability analysis and RelXpert reliability analysis are supported inside of the Virtuoso® ADE Product Suite. Allowing designers to account for the effect device aging during design and verification.

VI. ANALYZING THE EFFECT OF RADIATION

The final topic will explore is how reliability analysis interacts with analysing the effect of radiation on circuit performance. The first step is how to model the degradation due to radiation, this can be done by a change of variable instead of considering how the device characteristics change as function of time, the change as a function of dose, for total dose, for fluence, for neutron fluence, will allow us to use existing tools to consider the effect of radiation. However, custom models will need to be prepared. In the case of Spectre APS, the Universal Reliability Interface, URI, is provided so customer models can be integrated into the existing flow. In addition, the concept of mission profiles can be applied to the stress due to radiation, that is, the stress can be broken up into multiple stresses each one applied at a dose rate to model the environment that a satellite experiences, continuous exposure to background radiation with stress events due to solar flares.

One other technology to developed to help analyse and reduce the failure rate over product lifetime is analogue fault simulation which is used to simulate analogue test in order to reduce test escapes. Included in the analogue fault simulation is the ability to inject custom faults which can be used for simulating single-event transient upset.

While standard EDA tools may not directly support simulation the effect of radiation on devices, they are becoming more “radiation-hard” friendly.

VII. CONCLUSION

In this paper, we have looked at some recent advances in reliability analysis. These advances have been driven by the need to provide better prediction of product lifetime required to design for mission-critical applications.

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Characterization, Screening and Qualification of the MEDA Wind-Sensor ASIC

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Abstract

This paper describes the final characterization results of the MEDA-WS ASIC, which was described in a previous paper in AMICSA-2016. It describes as well the qualification and the screening processes that have been carried out prior to its integration in the final flying modules of the wind-sensor instrument.

I. Introduction

The paper describes the final steps of characterization, screening and qualification of the MEDA Wind-Sensor ASIC. This ASIC, whose design and preliminary functional measurements were already reported in AMICSA-2016 [1], is a key component of the wind-sensor included in the MEDA instruments set for the upcoming Mars-2020 mission [2].

In the present days, the ASIC has been fully characterized and has gone through a detailed qualification process. Samples have been screened and a selection has been made for the flight modules. The final integration in the instrument printed circuit board (PCB) and the final instrument calibration procedures are underway.

II. The MEDA wind-sensor ASIC

The MEDA Wind-Sensor (WS) ASIC is a mixed signal ASIC designed in a standard 0.35µm CMOS process [3]. This CMOS process had been previously characterized by the authors from IMSE with respect to radiation effects and low temperatures [4], [5], including the assessment and evaluation of typical radiation hardening by design (RHBD) techniques like the use of enclosed layout transistors (ELT) and the use of ward-rings around individual n-mos and p-mos sections. A rad-hard digital cells library and several other previous mixed-signal ASICs have also been designed by the authors from IMSE in the same process [6], [7], [8], [9] as part of a long term effort in the field of space microelectronics initially and mainly promoted by the Payloads Electronic Engineering Laboratory of INTA [10].

The functionality of the MEDA-WS-ASIC together with a description of its circuitry, some design details, and preliminary functional test results were already reported in AMICSA-2016 [1] and will not be detailed again. Essentially, it is that of an analogue front-end for sensor signal acquisition and AD conversion, with a number of multiplexed input channels, and a number of temperature-controlling feedback loops which provide and measure the heat power required to hold the temperatures constant. A digital section is in charge of tasks control and communications with the instruments control unit (ICU). Figure 1: shows a photograph of the MEDA wind sensor die.

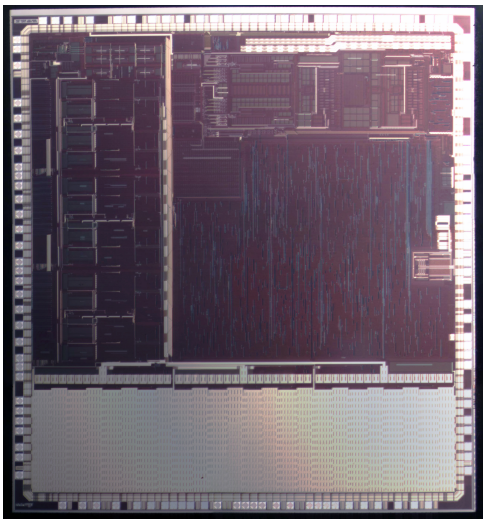

Figure 1: Photograph of the MEDA wind sensor ASIC die.

The wind sensor concept is based on previous work by Universidad Politécnica de Cataluña [11], [12]. The digital control and communication finite state machine (FSM) of the ASIC was designed at high level by CRISA [13]. CRISA was also in charge of the quality assurance control during the design of the ASIC. The design of the full-custom analogue circuitry, as well as the synthesis and back-end of the digital sections was carried out by IMSE. The development of the MEDA instruments set is being coordinated by Centro de Astrobiología (CAB) [14]. Finally, the screening and qualification processes have been defined and carried out by ALTER [15] with measurement set-ups designed by IMSE.

At the time of describing it for AMICSA-2016 [1], the ASIC samples had been received and some preliminary functional tests had been carried out, showing that it was operative and functional. This paper focuses on the works carried out from there on, in particular, on the final characterization results, final packaging, on the screening and qualification processes, and on the integration in the instrument electronics.

III. Characterization results

The ASIC has been found to be functional in every aspect, within a temperature range that goes from -128ºC to +50ºC. The digital control, the command execution, and the communication circuitry are operative, as well as the power-on-reset (POR) circuit, in the whole temperature range. The 16-bits ADC conversion channel, including the instrumentation amplifier and the ADC, has an equivalent input r.m.s noise in the range of 3 V_{LSBs} and a similar integral nonlinearity (INL). Its behaviour is not affected by temperature, apart from the obvious effect of the variations of the reference voltage. The input multiplexer does not affect the measurements, as expected: all channels have the same static transfer characteristic.

The voltage and current references behave as expected as well. The non-calibrated Vref values dispersion among different samples, at nominal temperature, is in the range of ±10mV. This can be calibrated and therefore reduced to values in the range of ±1mV. In any case, the relevant figure is the variation of Vref with temperature. After calibration, the variation within a temperature range of -135 to 50ºC is about ±3mV. Similar variations are observed in the reference current Iref, with a high correlation between Vref and Iref values among samples and temperature.

The several current sources present in the chip for biasing and heating behave as expected, with actual values very close to their nominal values and with the expected programming ranges. Again, the relevant figures are the dispersion among identical sources in a chip sample, among chip samples, and with temperature. As an overall figure, both dispersion at a given temperature and variations within the temperature range of -135 to 50ºC are in the range of 0.4% or lower. Effects of Vref variation are not accounted in that figure.

Concerning the thermal feedback loops, the auto-zeroed comparators have a residual offset of about 0.1Mv. The DACs used to set the prescribed temperatures of the hot dies have an INL in the range of 1 V_{LSB}. The feedback loops are stable and behave correctly, maintaining the temperatures of the hot dies at the prescribed temperature, and providing the count of heating current pulses applied to each die.

Finally, auxiliary blocks like the over-temperature alarms for the external dies and for the ASIC itself behave as expected as well. The same can be said concerning the proportional-to-absolute-temperature (PTAT) circuit used to monitor the ASIC temperature, and the resistive divider (VDD/3) used to monitor the power supply voltage. The internal reference calibration levels have their expected values and dispersions, and the RS-422 driver circuitry is slew-rate limited to about 1V/ms as required.

Summarizing, the ASIC fulfils the specified functionality and the required accuracy and temperature stability levels.

Although individual devices and primitives of the CMOS process had been characterized previously at very low temperatures, showing that their electrical simulation models were acceptable well below the foundry specified temperature range, it was not completely sure that the ASIC would maintain its functionality down to temperatures as low as -135ºC. Therefore, these results represented a significant milestone.

Measurement set-ups and functional tests have been done at IMSE. Low-temperature functional tests have been carried out at INTA facilities. IMSE has recently acquired the nitrogen cooled equipment required for very low temperature tests.

IV. Radiation tests

As already mentioned, the IC process had been previously characterized for space use. This included very low temperature devices characterization (large signal transfer characteristics, mainly), and the analysis of radiation effects from the perspective of total ionizing dose (TID) and single event effects (SEEs). Those previous analyses showed that the devices (3.3V), with specific ELT layouts, could withstand significant amounts of high energy photons without drastic degradations. Levels reached in that characterization were above 300Krads. The specification for the present ASIC was only of 9Krads. Concerning SEEs previous tests has shown that similar mixed-signal ICs, in the same process, using the same RHBD techniques and the specific rad-hard digital library, had a single-event upset (SEU) linear energy transfer (LET) threshold above ~30 MeV/(mg/cm²) and a single-event latch-up (SEL) threshold above at least 80 MeV/(mg/cm²). Still, tests were required and were carried out for the formal qualification of the ASIC.

TID tests were performed at the Centro Nacional de Aceleradores (CNA) [16], in Sevilla, using a Cobalt 60 gamma radiation source. Six IC samples were irradiated. They were kept biased at their nominal power supply voltage and at room temperature. The accumulated dose after 50H approx. (in one step) was 10.6Krads at a rate of approximatively 200 [rad(Si)/h]. No appreciable parameters shifts were detected in the subsequent electrical characterization, as expected. Figure 2: shows the TID test PCB.

Figure 2: Photograph of the TID test PCB in the irradiation area.

SEEs teste were performed at the Cyclotron Resource Centre [17] of the Université Catholique de Louvain (UCL). In order to fulfill the required test conditions, the device temperature had to be about 50ºC or larger. This was achieved exploiting the self-heating of the ASIC while in operation, taking temperature lectures from its internal PTAT, and modifying the amount of the heating currents in a controlled loop implemented in the test-set up software. The effective die temperature during the tests was about 65ºC. Two IC samples were tested, each using seven ion and incidence angle

combinations, with effective LET levels ranging from 16 to 81.6 MeV/(mg/cm²). Fluence for each specific ion/angle combination ranged from 1.2M ions/cm² for the higher energy combinations to 3.8M ions/cm² for the less energetic ones.

No latch-up was recorded up to the maximum effective LET available at the facility: 81,6 MeV/(mg/cm²)) using $^{124}Xe^{35+}$ ions with an incident angle of 40º. Figure 3: shows the SEEs test board with its latch-up detection circuitry, and the vacuum chamber at the UCL cyclotron facility.

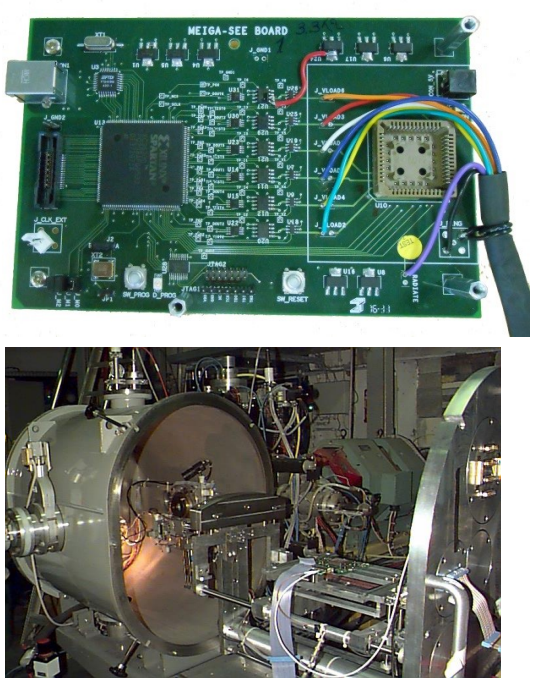

Figure 3: SEEs test board & vacuum chamber at the UCL cyclotron.

Concerning SEUs and single-event failure interrupts (SEFIs), no errors were detected up to a LET of 20.4 MeV/(mg/cm²) with $^{58}Ni^{18+}$. First few errors were observed with a LET of 32.4 MeV/(mg/cm²) with $^{84}Kr^{25+}$. Detailed estimations of upset rates under a geosynchronous orbit condition have been obtained using the procedures described in [18] and [19], resulting in figures lower than 1.5E-9 upsets/bit-day.

Displacement damages (DD) tests using some neutrons irradiation facilities were initially considered as well, but finally considered unnecessary, for a CMOS device, after the TID and SEEs results.

V. Packaging

The development of the MEDA instruments set relies, to a significant extent, on the results of a previous similar mission, REMS, [20], which contained a similar wind-sensor instrument. Much of the reliability issues and qualification processes take advantage of previous experience in REMS. The selected ASIC package, like in REMS, is a ceramic, 100 pins quad-flat package CQFP100. However, at the time of packaging the first ASIC-die samples, for the first functional tests, there were some procurement difficulties concerning the exact same package used in REMS. A CQFP100 from a similar manufacturer was then used for the initial samples, in order to proceed with the functional tests.

After the ASIC was found to be functional and within specs, an additional die lot was ordered from the foundry. These samples were then packaged in the same CQFP package used in REMS, which had been located by that time. This allowed us to skip a long and costly packaging qualification process. Furthermore, this avoided the significant cost of purchasing ASIC carriers and sockets, required for the screening and qualifications processes, since they were available at Alter facilities from the previous REMS ASIC qualification works.

The new dies lot was then packaged under space-use conditions by Optocap [21], and the screening and qualification processes begun on these flight-oriented ASIC lot. Figure 4: one of the final-packaged ASICs.

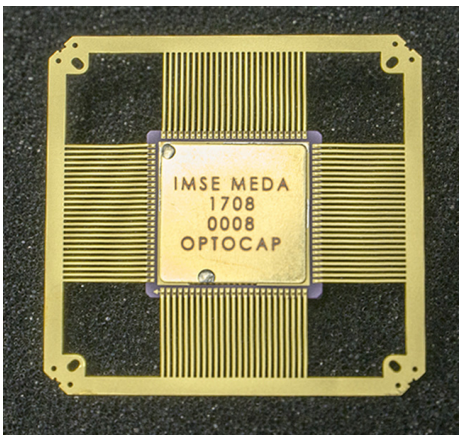

Figure 4: ASIC sample in its final package.

The ASIC function includes heating external silicon dies employed in the wind sensor set-up. The amount of heating power required, which is programmable due to the variable environmental conditions expected along the mission, poses eventual problems with ASIC operating temperature, since part of the “external dies heating power” is dissipated within the ASIC. This is increased by the low density Mars atmosphere, which reduces the heat dissipation capability as compared to that on Earth. Measurements of the junction-to-case thermal resistance θ_{jc} of the packaged samples have been carried out, again exploiting the programmable self-heating capability of the ASIC. The values obtained is in the range of 20ºC/W, which does not represent a problem. An evaluation of the case-to-ambient thermal resistance θ_{ca}, which depends on the final PCB design and the Mars atmosphere conditions, will be carried out for final assessment.

VI. Qualification and Screening

The formal qualification of the ASIC and the screening of the samples for flying-modules (FM) selection have been carried out by Alter TÜV Nord, with the assistance of IMSE concerning the functional electronic measurement set-ups.

The sampled lot consisted of 81 units. After a packaging evaluation test which required five samples, a few samples were dedicated to measurements set-ups development, leads forming validation, and other miscellaneous issues. Finally, 69 samples entered the screening process, which consisted on a sequence of different tests with intermediate functional measurements at room temperature. Specific tests included

constant acceleration, particles impact noise detection (PIND), temperature cycling (-135 to +125ºC), power burn-in (160 hours), and detailed functional and parametric measurements in the operating temperature range (-128 to 50ºC) temperature range for FM units selection. Finally, a seal (fine and gross) test and an external visual inspection were performed. After defining the acceptance limits, 64 samples passed the screening tests. Also, 25 samples were selected as FM samples according to the predefined selection criteria. All tests were made according to their corresponding MIL-STD-883 rules, and/or the previously defined ASIC validation acceptance limits.

The qualification process has consisted in three test groups: environmental, mechanical, and endurance, followed by a destructive physical analysis (DPA) on a few samples. All tests have been performed according to their corresponding MIL-STD-883 methods.

The environmental tests, performed on 15 samples, consisted in a thermal cycling (100 cycles from -135 to +125ºC), and a moisture resistance test. It was followed by electrical measurements at room temperature, a seal test (gross and fine leaks), and an external visual inspection. All samples passed the tests.

The mechanical tests, also performed on 15 samples, begun with a dimensions and lead integrity test, and a seal (fine and gross leaks) test. This was followed by a mechanical shock test (shock response spectrum), random vibration with several variable frequencies, and constant acceleration test. Intermediate electrical measurements were performed. Finally, a seal after mechanical shock test and a final external visual inspection were performed. All samples passed the tests.

The endurance test group was performed on 8 samples. It consisted on an operating life test at a temperature of +70ºC, during 1000 hours, with intermediate electrical measurements after 168 and 500 hours. Again, a seal test followed. All samples passed the tests.

Finally, 5 samples went through a destructive physical analysis. Three of those samples were taken from those that had gone through the endurance test, and one each from the environmental and mechanical tests samples. These DPA consisted in external visual inspection, seal test, radiography, residual gas analysis (RGA), terminal strength, internal inspection, destructive pull test, scanning electron microscopy (SEM) inspection, and die shear test. All DPA tests were successful (the 5 sampled passed) except for the RGA which all samples failed. Excessive moisture was found inside the cavity, possibly due to insufficiently cured epoxy. However, after a specific test was designed and executed to evaluate the possibility of dendrites formation among adjacent pads, the results have been satisfactory and the manufactured lot has been considered qualified.

VII. Conclusions and Summary

The MEDA wind-sensor mixed-signal ASIC [1], designed in a standard 0.35µm CMOS process using RHBD techniques, has been functionally and parametrically characterized, and the manufactured lot has been qualified for space use under the specifications of the Mars2020 mission, including radiation and very-low-temperature effects. A screening process has been used to select the best samples. The ASIC is presently being integrated in the final instrument PCBs. Instrument calibration procedures will follow.

Acknowledgment

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Digital Programmable Controller (DPC) : radhard die in low cost plastic package.
Session: Space Applications for analogue and mixed-signal ICs

AMICSA 2018

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Abstract

This presentation covers the lessons learned from introduction of the Digital Programmable Controller ASIC (DPC) into several space products. Full benefit of DPC introduction, like decentralization of equipment management, is currently limited by size and cost of the component, the latter being a key factor for constellations. Alternative packaging trade-off will be discussed: a non-hermetic BGA type package has been prototyped. Pro's and con's of the hermeticand non-hermetic options will be discussed including the associated TRL levels.

I. DPC STATUS

Started in 2012 in the frame of an Artes 5.2 contract, the development of the Digital Programmable Controller DPC has reached major milestones in 2017. The DPC successfully passed the formal qualification process: industrial qualification for space applications, as per ESCC 9000.

The DPC system on chip is a major breakthrough in the availability of radiation hardened highly integrated European micro-controller. This component uses the IMEC RHBD DARE on UMC 0.18µ library [1] [4] and custom analog IPs designed by ICsense [4] (ADCs, DACs, PLL, …).

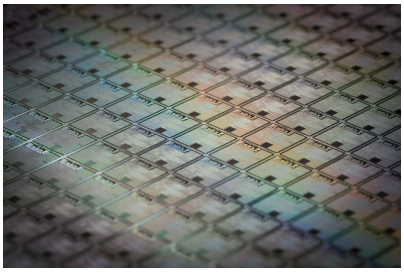

Figure 1: DPC wafer.

Since March 2014 (1st DPC ASIC's assembled [3]), the device has successfully been integrated into a large range of applications. The DPC is an essential building block for the development of intelligent avionics modules that for the first time allows implementing space grade-1 decentralized control such as promoted in the ESA-SAVOIR reference architecture for RTU. DPC is now the core controller of next generation avionics product from Thales Alenia Space where it is used to control power distribution, motor, thrusters, pyros for LEO and GEO satellites.

In order to support the DPC dissemination, a DPC reference kit (DRK) has been built. This board (industrial quality) allows the partner to take-over the DPC features and to start programming in a convenient environment. The DRK is made available with a GNU based SW development toolkit including compiler (gcc), debugger (gdb), boot loader, …

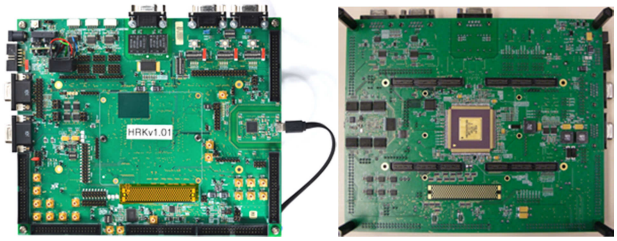

Figure 2: The qualified DPC reference kit.

The board is a rich self-contained prototyping tool (i.e. no other device needed than an USB plug on the SW development PC). It contains a large set of analog peripherals together with classical interfaces used in space applications such as mil-1553, dual CAN, RS4xx … Hence external designers start developing with the DPC in an space system context within less than 2 working days [8], including learning curve of the associated software development tools.

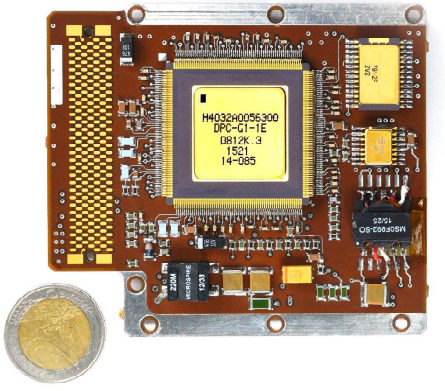

Figure 3: The DPC plugin module.

The DPC plugin module is a small space grade board containing the DPC, drivers, power supply and protection circuits. The designer of a new avionic module for specific scientific missions can easily plug it onto its customized mother board and has only to take care of high voltage or power interfaces.

Papers on DPC applications were presented during different workshop : CCT @ CNES [5] , ADCSS @ ESTEC [6], CAN in Space @ ESTEC [7], AMICSA 2016 [8] [9] [10]

II. THE DILEMMA OF THE NUMBER OF IOS

Micro-controllers are intended to be used in a very broad range of applications & use cases. For terrestrial applications, semiconductor manufacturers are proposing many variants of their micro-controllers with among other small, medium or large number of analogue and digital IOs. This is the ideal situation that also corresponds to needs in space applications.

The problem is that space qualification of a component is not only linked to die but also to package. Going for a 3 variants (large, medium, small) approach would require the 3 qualifications of the 3 component variants. This is clearly not affordable. For DPC, the choice was made of a large package offering more than 120 IOs.

Figure 4: The qualified DPC is packaged into a ceramic quad flat pack 256 pins.

This package choice & associated large number of IO was economically driven from using of the micro-controller in avionics applications. Indeed there are large cost savings of having a single controller per board (without IO extenders) to manage directly a large number of high power interfaces such as heaters, motors, pyro, battery cells.

On the other hand there are other applications where PCB area is limited & hence a large component is not welcome. A good solution to reduce the component footprint while maintaining large pin count is CCGA (Ceramic Column Grid Array). Back five years ago, column grid package was only available from US suppliers, adding export control issues to a design that had intentionally been made completely US free. So that the very classical but bulky CQFP 256 package was the only option affordable at low risk & reasonable costs.

Nowadays, the situation has improved columns are available from European sources. Nevertheless this technology remains used for very large pin-count components like big CPU, ASIC or FPGA. Mostly the reason is cost which remains well above a “simple” CQFP.

Cost is the other major factor that limits the massive introduction of micro-controllers. Where a designer has to optimize the total cost of the bill of material of an equipment, the natural trend is to concentrate a maximum of control functions into a single component.

III. NON HERMETIC

There are multiple options for plastic packaging such as PQFP, PBGA, QFN & CSP. PQFP would have been a simple & straightforward transfer from the ceramic version. However there is no improvement of the density in terms of occupied PCB area. CSP would have offered a significant reduction in occupied PCB area but it is well known [11] to not surviving thermal cycles. Finally PBGA was selected as a solution offering significant footprint reduction & also very good robustness to thermal cycling stress.

Package type	number of cycles -40°C to +125°C before failure
PQFP	>10000
PBGA	3000 to 8000
QFN	1000 to 3000
CSP & flip-chip	<1000

Fig./Table 5: Solder join failure [11] due to thermal cycles

Thanks to the nature of the base substrate used in PBGA (=FR4 instead of ceramic like in CCGA) the thermal expansion coefficient of the application PCB is matching very well to the one of the PBGA component. A JPL study [12] reports that PBGA offers better robustness to thermal cycling that CCGA. Thermal cycling test conducted at TAS on COTS PBGA components confirmed that no degradation of the solder joins is observed after 2000 cycles from -55°C to +125°C. This practically means that standard low cost balls can be used for assembly instead of (space specific) columns, but the carrier has to be made of epoxy: a non hermetic assembly.

IV. PBGA ASSEMBLY FOR SMALL “SPACE” LOTS

After selecting Plastic BGA (non-hermetic) to be the right technical solution, comes the question of finding a assembly house that accepts to take a PO for a small production lot while providing all guaranties of process control. IMEC-services (IC-Link) provided the answer. Package & FR4 substrate was designed in IMEC. A full automotive assembly line (monthly producing millions of pieces) was then made accessible through IMEC’s cooperation schemes. This turned out to be a key element: offering a well mastered & reproducible assembly process.

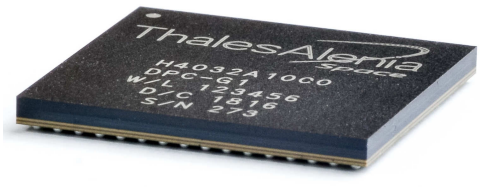

Figure 6: The BGA-256 DPC package designed @ IMEC

The management of this assembly flow (automotive assembly line) strongly differs from classical follow-up of assembly flow used for space components which is based on multiple inspections, destructive tests & material controls to reassess the assembly process stability. The term "high-reliability" or "hi-rel", used almost exclusively for space/military, is based on these intrusive controls. When working with an automotive assembly line, the process stability is permanently checked. Consequently, the reliability issue is addressed by Statistical Process Control (SPC). The process builds reliability into the part.

Nevertheless, lot qualification and up-screening according to ECSS 60-13C will be applied. Similarly each component will be 100 percent tested and screened as for any high-rel parts.

The use of a mass production assembly line leads to more than an order of magnitude difference in recurrent cost of the assembled components. Although there is a non negligible lot fixed charge fee, it still allows to produce large volume of components within affordable investments.

However following steps (lot qualification & individual component testing) are now dominating & defining the component cost breakdown. These costs do not differ from the "standard" approach followed for CQFP variant. Hence final component costs heavily depends on the requested test coverage (number of T° test points, burn-in, …) and finally the lot size considered for the parts qualification.

Obviously this approach nicely addresses the low-cost targets pushed by mega-constellation projects that make use a large component volumes. Furthermore, the fact this µC is based on truly radhard design is a major differentiator with µC based on upscreening automotive components. Indeed introduction of said "COTS" components is generally presented as the method to achieve the low-cost targets of mega-constellation. In practice radiation effects (transients, reboots, corruptions …) onto those said "COTS" components need to be managed somewhere by the equipment. Here the presence on each board of the avionic electronic system of fully thrusted, deterministic, robust & radhard controller turns out to be a key for success.

V. INCREASED DENSITY

PBGA technology clearly brings a significant improvement. The integration of decoupling capacitor inside the package reduces PCB area by a factor >5.

The availability of a low cost compact component opens the door for simple performance up-scaling by simply using 2 or multiple controllers per board. Multiplication is now affordable, pushing away any limits of processing power, memory or even number of IO.

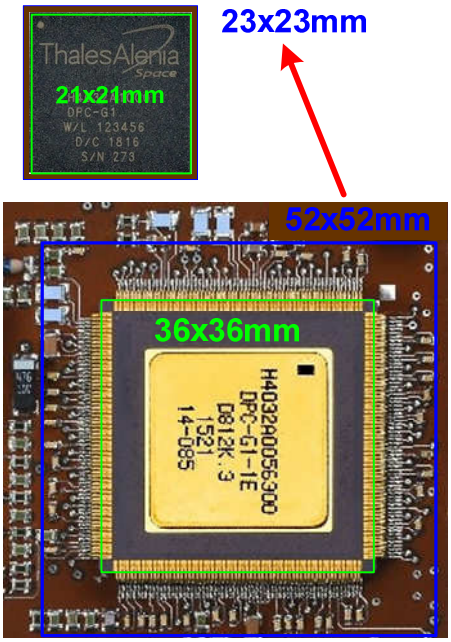

Figure 7: The BGA occupies 6x less area on the PCB.

This breakthrough also makes the DPC affordable to be used in CubeSat both in term of size & cost. The University of Liège had successfully developed & launched on 26 Apr 2016 of the OUFTI-1 educational 1-U CubeSat, with an amateur-radio D-STAR repeater as its primary mission. In its OUFTI-2 project, a DPC with BGA package will be used as OBC leveraging on the full radhard properties of the DPC. Hence delivering a trustable OBC control system. [13]

VI. CONCLUSION

Alternative packaging has been introduced: a non-hermetic PBGA. This allows significant gains in PCB area, solves the dilemma of the number of IOs. It is the step forward to achieve the low-cost targets of mega-constellation: first through the use of an automotive mass production assembly process. Second: it allows to manage "COTS" malfunctions due to radiations by having, on each board of the avionic electronic system, a fully thrusted, deterministic, robust & radhard controller.

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ESCC Single-Phase-Qualification of Space Microcircuits

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Abstract

As announced at previous AMICSA workshops in 2012 and 2016, the European Space Components Coordination (ESCC) system has evolved in recent years in order to improve its Qualification methodologies. In order to save time and efforts and remove any possible duplications o repetitions, an effort is underway to transform the current ESCC scheme, based on the implementation of two independent stages of actual component tests (electrical, environmental, endurance).

This paper describes:

- the principles of implementation of Single Phase Qualification (SPQ) as set in the latest update (up to its issue 10) of ESCC 9000 (Integrated circuits: Monolithic and Multichip Microcircuits, Wire-bonded, Hermetically Sealed and Flip-Chip Monolithic Microcircuits, Solder Ball bonded, Hermetically and Non-hermetically Sealed, and Die)

- the progress in the preparation of the Assembly and Test Houses (ATH) certification scheme.

Both developments will streamline testing requirements and may therefore open opportunities for a fast-track to full ESCC Qualification for Microcircuits.

I. ESCC 9000 ISSUE 10 (FEBRUARY 2018)

A. Scope of insertion of SPQ in ESCC 9000.

The insertion of SPQ is limited to hermetic, wire-bonded, Integrated Circuits. This implies that the formal Qualification of Flip-chip and Die product is still to be achieved through the implementation of two separate stages of test, as defined in ESCC 9000 and ESCC 226900.

B. SPQ in ESCC9000 Iss. 10– A helicopter view.

The insertion of SPQ requires initial assessment activities followed by a Qualification test stage:

(a) Initial assessment

The initial assessment reviews the manufacturer's status of conformance with general ESCC requirements. These include:
- a commitment to maintain the mid-term availability of product in the market,
- a commitment to maintain qualification,
- the implementation of ESCC-specific Quality Assurance requirements and other documentation requirements.

The initial assessment reviews as well the component in question regarding its construction, performances, compatibility with the Space environment and intrinsic reliability. In particular, on the subject of the component's reliability, wafer-level and component-level requirements are developed in the ESCC 9000 specification with the aim to establish satisfactory operation of the qualified microcircuits up to 18 years operating life at Tj ≤ +110°C. In lack of suitable test data evidence, at this assessment stage, in this respect, the duration for Operating Life Test (OLT), to be performed as part of Qualification testing, may have to be doubled up to 4000 hours at Tamb = +125°C.

The initial assessment's requirements have developed policy agreed in general in recent years for the whole ESCC system, with the aim to assess better the qualified components for their compatibility with their use and application. This includes, for example, a more explicit -possibly harder- approach, which has been developed in this update of the specification, to verify by test the component's capabilities with regards to: mission reliability, radiation hardness or its assembly onto a printed circuit board. With the development of SPQ, an assessment of the microcircuit's capability to withstand typical mounting techniques is now required as a prerequisite to advance further into Qualification. Similarly, Radiation evaluation test evidence and Construction Analysis reports, obtained in line with mandatory test method requirements as set in applicable ESCC specifications, have become necessary inputs at the time of this initial assessment.

The initial assessment concludes with a Manufacturer Data Review, an "extended audit", where the ESCC Executive confirms adequacy and completeness of the data. It may be noted therefore that no manufacturer's self-certification is possible in this respect, as this is a general rule for ESCC Qualification. The Manufacturer Data Review in fact substitutes the Evaluation phase specified in general in ESCC for other technologies and opens the door to the only stage of Qualification testing required.

(b) Qualification testing Phase

A revised chart F4A in ESCC 9000 defines Qualification testing through the identification of sequences of tests, test methods and sampling requirements. The various tests are gathered in different branches in the referenced chart, as subgroups (SG). It is really worth mentioning that microcircuits submitted to Qualification testing have to satisfactorily pass first the ESCC 9000 production control inspections and screening tests as applicable, identified in the specification's charts F2A and F3A, respectively.

The main changes introduced in this update of ESCC 9000, compared to its previous issue 9, are described in the rest of

this paragraph, in consideration of the test required for each SG.

- Environmental / Mechanical SG. Test condition letter C (-65°C/+150°C) is now specified for Temperature Cycling in accordance with MIL-STD-883, Test Method 1010 (where it was letter B, -55°C/+125°C).

- Endurance SG. The possibility that the duration of OLT may need to be extended up to 4000 hours has been implemented (where it was 2000 hours). The sampling size has also been increased, up to 45 pieces, for OLT at the time of (initial) Qualification Testing.

- Assembly Capability SG. An Internal Gas Analysis has been added (MIL-STD-883, Test Method 1018).

These changes, introduced in the chart F4A as explained, have resulted in a more demanding set of requirements in some aspects. In exchange of this slightly additional effort, the whole test sequence previously required as a first evaluation test stage in ESCC 2269000, has become obsolete for hermetic, wire-bonded integrated circuits in the ESCC Qualification system. It may be noted as well that the revised chart F4A, supplemented by charts F2A and F3A as explained, requires the implementation of all tests usually required for microcircuits qualification for the most demanding missions (for example, all tests defined in NASA's EEE-INST-002, Section M3, except its SG6, are now required in ESCC 9000 from issue 10).

C. Opportunities and risks.

As highlighted at the time of AMICSA 2016, overlapping the previously specified two stages of test (evaluation as required in ESCC 2269000 + Qualification as required in ESCC 9000) was not really forbidden in the past, but it rarely happened in formal Qualification. It was often understood that proceeding to Qualification testing without the product knowledge and other assurances obtained in the Evaluation stage might introduce too high a risk.

However, experience in many satellite projects, as obtained in the last 20 years, has proven that certain risks do not actually materialise that often if an adequate EEE Parts Engineering approach may be implemented at the level of part's specification, radiation evaluation and procurement inspections. In addition, maturity has been achieved among most established component manufacturers supplying space parts, so their understanding of the space market expectations and needs is usually very complete. This implies that some of these manufacturers are often performing extensive product evaluations before they bring any new space products to the market. This sometimes means that the sort of test evidence that might be obtained from a traditional ESCC evaluation test phase may have actually been gathered already, independently, by the manufacturers, who may then be open to share it with the ESCC Qualifying agencies at the time of an initial assessment, as explained. As a result of all this, confronted with cost and schedule limitations, implementing a "success-oriented" lot qualification in parts procurement is not an infrequent practice. This has not eliminated of course the risk that a flight lot fails tests, or that the component's expected performance and capabilities cannot be obtained from a specific lot. To a certain extent, in the move to SPQ, the ESCC system has started to mirror that space parts procurement approach, and, hence, abandon a nearly absolute aversion to component reliability or workmanship risks. The risk is, as in the case of real life parts procurement, that a formal Qualification project actually fails to achieve its desired target if the specified Qualification test regime is just too demanding for the technology or component in question. In a way, using a SPQ scheme will prove (again) that the certification of an achieved formal Qualification "only happens when it happens".

In a similar fashion, it is acknowledged that advancing to a SPQ approach may imply a higher risk that Qualification testing actually encounters failures, as one of the outputs evaluation testing may be to limit the scope of qualification, or refine specification component ratings or performance characteristics. In addition, experience shows that a (possibly) slower, two-stage Qualification approach actually gives manufacturers and agencies the opportunity and time to develop and stabilise adequate test strategies, methods and means, with a proper level of documentation. With the introduction of SPQ, the risk that a new test set-up actually fails to serve its purpose may therefore become more real if there is less time to design and verify it. This sort of risk becomes obviously more serious in the case of relatively new manufactures or component supply chains, which imply outsourced operations. In these cases, the lack of an adequately developed and stable supply chain may actually lead to a failed Qualification campaign. In this respect, when implementing a SPQ, the manufacturers and qualifying agencies need to perform a solid, detailed and systematic review of the product and test baseline before the Qualification testing starts, as this is a first-time-right approach.

The new SPQ methodology for microcircuits qualification still tries to obtain massive reliability and quality assurance by component testing. However, the revised ESCC 9000 focuses more on setting a suitable minimum acceptance test limit (the revised chart F4A, actually more demanding than it was) while it leaves it to the manufacturer to compile a satisfactory and convincing-enough product file, a data set, his "internal qualification", to be reviewed and approved in an extended audit. The expectation is that this move might increase the number of fully qualified parts and technologies, which would still be supported by sufficient assurance by test and would benefit as well from the well-established set of ESCC Quality Assurance requirements, which have ensured that ESCC Qualified parts have performed reliably for decades in so many missions..

II. ASSEMBLY AND TEST HOUSES CERTIFICATION

At the time of writing, efforts are in progress in order to define ESCC requirements for the certification of the capabilities of Assembly And Test Houses (ATH). The general certification scheme to be used in this case is called

Process Capability Approval (PCA) and is introduced in ESCC 25600 specification. This PCA approach has been developed and implemented already in the case of hermetic and non-hermetic hybrid (typically “chip and wire” on a substrate) manufacturing lines in Europe, in accordance with requirements set in ESCC 2566000 and ESCC 2566001, respectively. In the case of ATH certification, it is expected that an ESCC specification for such process capability approvals may be finished and published before the end of 2018.

REFERENCES AND ACKNOWLEDGEMENTS

General information and the procedures and documentation that describe the ESCC system are publicly available for download at the ESCC website, https://spacecomponents.org

All ESCC specifications mentioned in this paper are publicly available for download at the European Space Components Information Exchange System website, https://escies.org

NASA’s EEE-INST-002 is available for download from NASA Electronic Parts and Packaging (NEPP) Program website, https://nepp.nasa.gov

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A better understanding of the ESCC system can be achieved by checking the information published at the mentioned website (https://escies.org), through the reading of ESCC 20000, by sending specific questions or requests to secretariat@escies.org or by attending an ESCC training session, such as those organised periodically by ESA at its ESTEC establishment, which are free of charge.

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