Digital Programmable Controller (DPC) : radhard die in low cost plastic package.
Session: Space Applications for analogue and mixed-signal ICs

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Abstract

This presentation covers the lessons learned from introduction of the Digital Programmable Controller ASIC (DPC) into several space products. Full benefit of DPC introduction, like decentralization of equipment management, is currently limited by size and cost of the component, the latter being a key factor for constellations. Alternative packaging trade-off will be discussed: a non-hermetic BGA type package has been prototyped. Pro's and con's of the hermeticand non-hermetic options will be discussed including the associated TRL levels.

I. DPC STATUS

Started in 2012 in the frame of an Artes 5.2 contract, the development of the Digital Programmable Controller DPC has reached major milestones in 2017. The DPC successfully passed the formal qualification process: industrial qualification for space applications, as per ESCC 9000.

The DPC system on chip is a major breakthrough in the availability of radiation hardened highly integrated European micro-controller. This component uses the IMEC RHBD DARE on UMC 0.18µ library [1] [4] and custom analog IPs designed by ICsense [4] (ADCs, DACs, PLL, …).

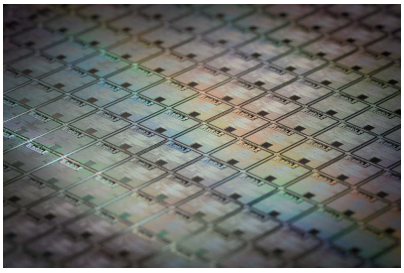

Figure 1: DPC wafer.

Since March 2014 (1st DPC ASIC's assembled [3]), the device has successfully been integrated into a large range of applications. The DPC is an essential building block for the development of intelligent avionics modules that for the first time allows implementing space grade-1 decentralized control such as promoted in the ESA-SAVOIR reference architecture for RTU. DPC is now the core controller of next generation avionics product from Thales Alenia Space where it is used to control power distribution, motor, thrusters, pyros for LEO and GEO satellites.

In order to support the DPC dissemination, a DPC reference kit (DRK) has been built. This board (industrial quality) allows the partner to take-over the DPC features and to start programming in a convenient environment. The DRK is made available with a GNU based SW development toolkit including compiler (gcc), debugger (gdb), boot loader, …

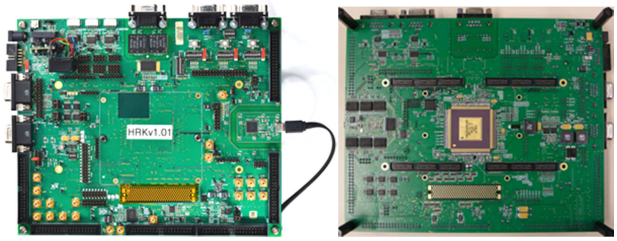

Figure 2: The qualified DPC reference kit.

The board is a rich self-contained prototyping tool (i.e. no other device needed than an USB plug on the SW development PC). It contains a large set of analog peripherals together with classical interfaces used in space applications such as mil-1553, dual CAN, RS4xx … Hence external designers start developing with the DPC in an space system context within less than 2 working days [8], including learning curve of the associated software development tools.

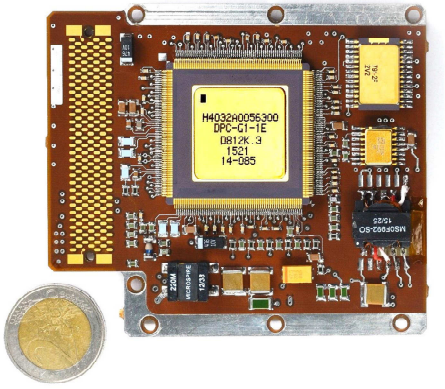

Figure 3: The DPC plugin module.

The DPC plugin module is a small space grade board containing the DPC, drivers, power supply and protection circuits. The designer of a new avionic module for specific scientific missions can easily plug it onto its customized mother board and has only to take care of high voltage or power interfaces.

Papers on DPC applications were presented during different workshop : CCT @ CNES [5] , ADCSS @ ESTEC [6], CAN in Space @ ESTEC [7], AMICSA 2016 [8] [9] [10]

II. THE DILEMMA OF THE NUMBER OF IOS

Micro-controllers are intended to be used in a very broad range of applications & use cases. For terrestrial applications, semiconductor manufacturers are proposing many variants of their micro-controllers with among other small, medium or large number of analogue and digital IOs. This is the ideal situation that also corresponds to needs in space applications.

The problem is that space qualification of a component is not only linked to die but also to package. Going for a 3 variants (large, medium, small) approach would require the 3 qualifications of the 3 component variants. This is clearly not affordable. For DPC, the choice was made of a large package offering more than 120 IOs.

Figure 4: The qualified DPC is packaged into a ceramic quad flat pack 256 pins.

This package choice & associated large number of IO was economically driven from using of the micro-controller in avionics applications. Indeed there are large cost savings of having a single controller per board (without IO extenders) to manage directly a large number of high power interfaces such as heaters, motors, pyro, battery cells.

On the other hand there are other applications where PCB area is limited & hence a large component is not welcome. A good solution to reduce the component footprint while maintaining large pin count is CCGA (Ceramic Column Grid Array). Back five years ago, column grid package was only available from US suppliers, adding export control issues to a design that had intentionally been made completely US free. So that the very classical but bulky CQFP 256 package was the only option affordable at low risk & reasonable costs.

Nowadays, the situation has improved columns are available from European sources. Nevertheless this technology remains used for very large pin-count components like big CPU, ASIC or FPGA. Mostly the reason is cost which remains well above a “simple” CQFP.

Cost is the other major factor that limits the massive introduction of micro-controllers. Where a designer has to optimize the total cost of the bill of material of an equipment, the natural trend is to concentrate a maximum of control functions into a single component.

III. NON HERMETIC

There are multiple options for plastic packaging such as PQFP, PBGA, QFN & CSP. PQFP would have been a simple & straightforward transfer from the ceramic version. However there is no improvement of the density in terms of occupied PCB area. CSP would have offered a significant reduction in occupied PCB area but it is well known [11] to not surviving thermal cycles. Finally PBGA was selected as a solution offering significant footprint reduction & also very good robustness to thermal cycling stress.

Package type	number of cycles -40°C to +125°C before failure
PQFP	>10000
PBGA	3000 to 8000
QFN	1000 to 3000
CSP & flip-chip	<1000

Fig./Table 5: Solder join failure [11] due to thermal cycles

Thanks to the nature of the base substrate used in PBGA (=FR4 instead of ceramic like in CCGA) the thermal expansion coefficient of the application PCB is matching very well to the one of the PBGA component. A JPL study [12] reports that PBGA offers better robustness to thermal cycling that CCGA. Thermal cycling test conducted at TAS on COTS PBGA components confirmed that no degradation of the solder joins is observed after 2000 cycles from -55°C to +125°C. This practically means that standard low cost balls can be used for assembly instead of (space specific) columns, but the carrier has to be made of epoxy: a non hermetic assembly.

IV. PBGA ASSEMBLY FOR SMALL “SPACE” LOTS

After selecting Plastic BGA (non-hermetic) to be the right technical solution, comes the question of finding a assembly house that accepts to take a PO for a small production lot while providing all guaranties of process control. IMEC-services (IC-Link) provided the answer. Package & FR4 substrate was designed in IMEC. A full automotive assembly line (monthly producing millions of pieces) was then made accessible through IMEC’s cooperation schemes. This turned out to be a key element: offering a well mastered & reproducible assembly process.

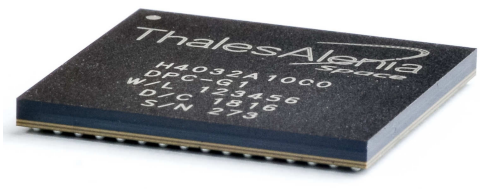

Figure 6: The BGA-256 DPC package designed @ IMEC

The management of this assembly flow (automotive assembly line) strongly differs from classical follow-up of assembly flow used for space components which is based on multiple inspections, destructive tests & material controls to reassess the assembly process stability. The term "high-reliability" or "hi-rel", used almost exclusively for space/military, is based on these intrusive controls. When working with an automotive assembly line, the process stability is permanently checked. Consequently, the reliability issue is addressed by Statistical Process Control (SPC). The process builds reliability into the part.

Nevertheless, lot qualification and up-screening according to ECSS 60-13C will be applied. Similarly each component will be 100 percent tested and screened as for any high-rel parts.

The use of a mass production assembly line leads to more than an order of magnitude difference in recurrent cost of the assembled components. Although there is a non negligible lot fixed charge fee, it still allows to produce large volume of components within affordable investments.

However following steps (lot qualification & individual component testing) are now dominating & defining the component cost breakdown. These costs do not differ from the "standard" approach followed for CQFP variant. Hence final component costs heavily depends on the requested test coverage (number of T° test points, burn-in, …) and finally the lot size considered for the parts qualification.

Obviously this approach nicely addresses the low-cost targets pushed by mega-constellation projects that make use a large component volumes. Furthermore, the fact this µC is based on truly radhard design is a major differentiator with µC based on upscreening automotive components. Indeed introduction of said "COTS" components is generally presented as the method to achieve the low-cost targets of mega-constellation. In practice radiation effects (transients, reboots, corruptions …) onto those said "COTS" components need to be managed somewhere by the equipment. Here the presence on each board of the avionic electronic system of fully thrusted, deterministic, robust & radhard controller turns out to be a key for success.

V. INCREASED DENSITY

PBGA technology clearly brings a significant improvement. The integration of decoupling capacitor inside the package reduces PCB area by a factor >5.

The availability of a low cost compact component opens the door for simple performance up-scaling by simply using 2 or multiple controllers per board. Multiplication is now affordable, pushing away any limits of processing power, memory or even number of IO.

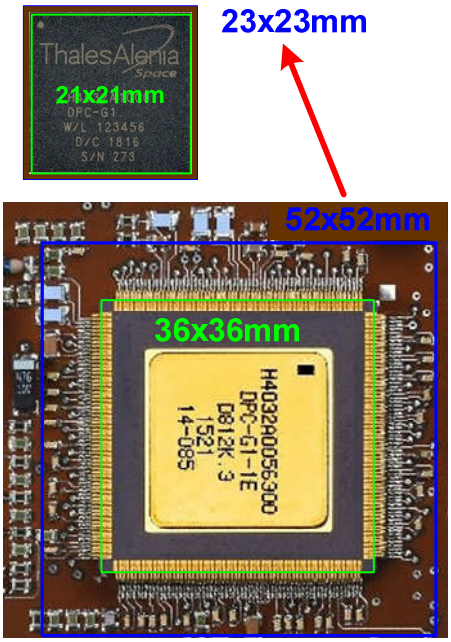

Figure 7: The BGA occupies 6x less area on the PCB.

This breakthrough also makes the DPC affordable to be used in CubeSat both in term of size & cost. The University of Liège had successfully developed & launched on 26 Apr 2016 of the OUFTI-1 educational 1-U CubeSat, with an amateur-radio D-STAR repeater as its primary mission. In its OUFTI-2 project, a DPC with BGA package will be used as OBC leveraging on the full radhard properties of the DPC. Hence delivering a trustable OBC control system. [13]

VI. CONCLUSION

Alternative packaging has been introduced: a non-hermetic PBGA. This allows significant gains in PCB area, solves the dilemma of the number of IOs. It is the step forward to achieve the low-cost targets of mega-constellation: first through the use of an automotive mass production assembly process. Second: it allows to manage "COTS" malfunctions due to radiations by having, on each board of the avionic electronic system, a fully thrusted, deterministic, robust & radhard controller.

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